Piezoelectric CMOS Charger: Highest Output-Power Design

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Abstract

Wireless microsensors and internet of things that add intelligence to the surroundings need ambient energy to extend life and expand functionality. Piezoelectric transducer can turn vibrations into electrical charge, and with the recycling bridge power stage, it can keep the highest voltage across the transducer and output the most power into the battery. This paper examines how to design the optimum recycling bridge power stage. Specifically, this paper theorizes the optimum size of the switches, the optimum inductor, and how to operate the circuit so that it losses the least power. The ohmic loss should equal charge loss to yield the lowest total loss on a MOSFET switch. The loss on the switches and the inductor are co-optimized. The switched inductor charger is optimized for discontinuous conduction mode. The resulting optimized power stage is 92% efficient. **Keywords**

Piezoelectric, charger, CMOS, switched-inductor, synchronous switch harvesting on inductor (SSHI), optimize power switch, lowest loss, powering internet of things.

1. Piezoelectric-Powered Systems

Wireless microsensors and internet of things embedded in factories, vehicles, and human bodies add intelligence to the surroundings to save money, energy, and lives [1]–[4]. To be non-intrusion to the environment, they must be tiny, and the batteries drain quickly. Fortunately, vibration is present in many applications [5]–[6], and recent research shows that piezoelectric transducers [7] can draw power from the vibration to constantly replenish the batteries to extend life for the microsensors [8]–[14].

A piezoelectric powered system, shown in Fig. 1, consists of the transducer, modeled as an alternating current source in parallel with its parasitic capacitor [8], a charger to charge the battery, and power supplies to provide power for the loads. The charger, however, has power loss and adds breakdown constraints to the system. With these constraints, it is important to optimally design the charger to increase drawn power and reduce losses in limited spaces.

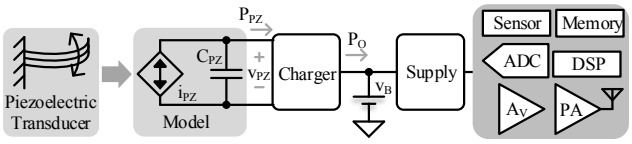

Fig. 1. Piezoelectric transducer powered microsystem.

In this paper, we demonstrate an example optimization process with the following parameters: piezoelectric capacitance C_{PZ} is 15 nF, $i_{PZ(PK)}$ is 20 µA, vibration frequency f_{VIB} is 100 Hz, CMOS breakdown voltage V_{BD} is 3.0 V, and inductor volume L_{VOL} is 3 × 3 × 0.8 mm^3 < 10 mm^3. Section II compares and selects the best power stage. Sections III through V optimize the three segments of the power stage.

2. Highest-P_{PZ} Charger

Piezoelectric transducers have low mechanical to electrical coupling factors [8]–[14]. As a result, the vibration is hardly affected by the electrical power it generates, and the charge, and current i_{PZ} in Fig. 2, also remains the same. Since power is current multiplies voltage, the higher voltage across the transducer, the higher power it generates. Since the transducer interfaces with the CMOS charger, the voltage cannot exceed the breakdown voltage V_{BD}. Therefore, keeping v_{PZ} near V_{BD} across the positive half cycle, and at $-V_{BD}$ across the negative, produces the highest power P_{PZ}.

The recycling bridge power stage, commonly referred to as Synchronous Swith Harvesting on Inductor (SSHI) [8]–[11], in Fig. 3 can achieve exactly that. The maximum power point (MPP) switched inductor (SL) utilizes a buck-boost converter to regulate v_R near V_{BD} and charge the battery v_O. Across the positive half cycle of the vibration, synchronous diodes D_{TR} and D_{BG} direct positive i_{PZ} into rectifying capacitor C_R. After the positive half cycle, at 7.5 ms in Fig. 2, S_X closes so that the inductor L_X receives all the energy from C_{PZ}, and subsequently charges C_{PZ} in the negative direction across t_X. Similarlily, across the negative half cycle, synchronous diodes D_{TG} and D_{BR} direct negative i_{PZ} into rectifying capacitor C_R, after which, at 2.5 ms, S_X closes so that the L_X receives all the energy from C_{PZ}, and subsequently charges C_{PZ} in the positive direction across t_X. The power from the transducer is

$$P_{PZ} = \int v_{PZ} i_{PZ} dt \le V_{BD} \int |\, i_{PZ} \,|\, dt\,. \quad (1)$$

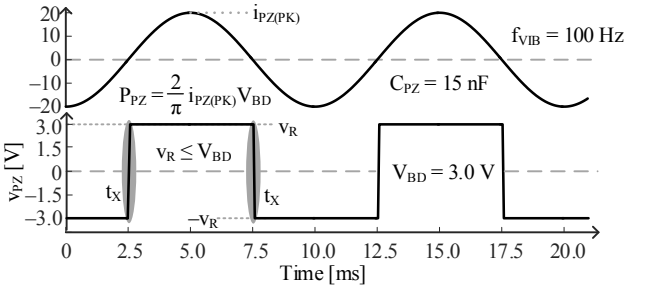

Fig. 2. Voltage and current waveforms for piezoelectric transducer.

Unfortunately, chargers lose ohmic power on the transfers, and charge loss to open and close the switches. As a result, not all the drawn power reaches the battery. The following three sections present the way to design the optimal recycling bridge power stage to maximize the power that reaches the battery.

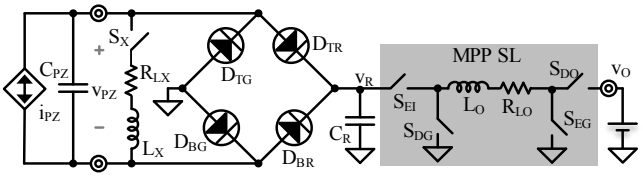

Fig. 3. Recycling bridge power stage.

3. Optimize Power Switches

The power switches employed in the power stage consume ohmic loss when they conduct current. They also require charge provided from the supply to switch them on and off [15]. For a MOSFET switch, we use the minimum length device to reduce the silicon area. The on resistance R_{MOS} decreases with the width of the device W_{MOS}, and the gate capacitance C_G increases with it. Therefore, the wider the switches, the higher the charge loss, but the lower the ohmic loss. Optimizing the power switches comes down to finding the lowest sum of these two losses.

Each power switch consumes ohmic power $P_{R(MOS)}$

$$P_{R(MOS)} = i_{MOS(RMS)}{}^2 R_{MOS}\left(\frac{t_C}{t_{VIB}}\right) = \frac{K_{R(MOS)}}{W_{MOS}} \propto \frac{1}{W_{MOS}}, \quad (2)$$

where $i_{MOS(RMS)}$ is the root-mean-square (RMS) current through the device, t_C is the conduction time, and $K_{R(MOS)}$ is the coefficient. Each switch also requires charge to switch it on and off, and consumes charge loss $P_{C(MOS)}$

$$\begin{aligned} P_{C(MOS)} &= v_{DD} q_C f_{SW} = v_R (C_G v_R) f_{SW} = C_G V_{BD}{}^2 f_{SW}, \\ &= K_{C(MOS)} W_{MOS} \propto W_{MOS} \end{aligned} \quad (3)$$

where q_C is the charge required to turn the switch on, f_{SW} is the switching frequency, v_{DD} is the supply voltage, and $K_{C(MOS)}$ is the coefficient. Since v_R is regulated to near V_{BD}, v_{DD} is also near V_{BD}. To find the lowest total loss, we increase W_{MOS} until the change in $P_{C(MOS)}$ cancels the change in $P_{R(MOS)}$.

$$\begin{aligned} \frac{dP_{MOS}}{dW_{MOS}} &= \frac{dP_{R(MOS)}}{dW_{MOS}} + \frac{dP_{C(MOS)}}{dW_{MOS}} \\ &= -\frac{K_{R(MOS)}}{W_{MOS}{}^2} + K_{C(MOS)} = 0 \end{aligned} \quad (4)$$

The optimum width is therefore

$$W_{MOS}' = \sqrt{\frac{K_{R(MOS)}}{K_{C(MOS)}}}, \quad (5)$$

and the total loss is

$$\begin{aligned} P_{MOS}' &= P_{R(MOS)}' + P_{C(MOS)}' = \frac{K_{R(MOS)}}{W_{MOS}'} + K_{C(MOS)} W_{MOS}' \\ &= \frac{K_{R(MOS)}}{\sqrt{\frac{K_{R(MOS)}}{K_{C(MOS)}}}} + K_{C(MOS)} \sqrt{\frac{K_{R(MOS)}}{K_{C(MOS)}}} \\ &= 2\sqrt{K_{R(MOS)} K_{C(MOS)}} \end{aligned} \quad (6)$$

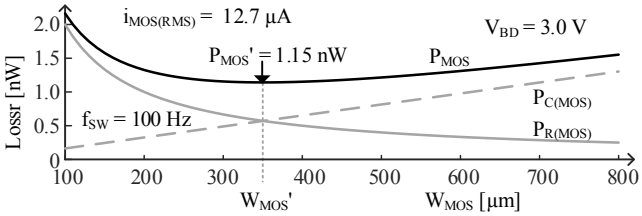

Fig. 4. Ohmic, charge, and total loss on a switch with optimum width.

This occurs when $P_{C(MOS)}$ equals $P_{R(MOS)}$, and it is shown in Fig. 4. As a result, optimized power switches always consume equal ohmic and charge loss.

Bridge: The bridge consists of 4 power switches. Each switch on the bridge conducts half of t_{VIB}, and the current across that conduction time is i_{PZ}, with an RMS of 12.7 µA. Therefore, we can use (2) and (3) to optimize the bridge, and each switch consumes 1.15 nW with and optimized width of 350 nm. Therefore, the loss of bridge P_{BRG} is 4.6 nW.

Recycler/Switched Inductor: The ohmic loss and charge loss on the power switches in the rest of the power stage, i.e. the two switched inductors (SL), is not only a function of the width of the device, but some other design parameters, e.g. inductance and switching frequency. However, the conclusion that the loss on the power switch is the least when charge loss equals the ohmic loss still applies. Therefore, we can use this conclusion to remove device width as a variable in the optimization, and optimize the other design parameters.

4. Optimize Recycler

After the bridge steers current into rectifying capacitor C_R across a half cycle, the recycler, consists of switch S_X and inductor L_X with equivalent series resistance R_{LX}. The inductor receives all the energy from C_{PZ} across a quarter of the LC oscillation cycle, as the current and voltage waveforms in Fig. 5 indicate, and back to the C_{PZ} in the opposite direction across the next quarter cycle. The transition takes a half cycle

$$t_X = 0.5 t_{LC} = 0.5\sqrt{2\pi L_X C_{PZ}}. \quad (7)$$

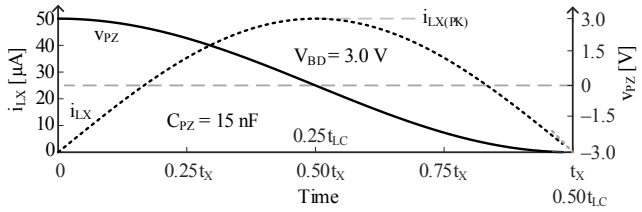

Fig. 5. Current and voltage waveforms for the recycler.

The energy transferred E_X is

$$E_X = E_C = 0.5 C_{PZ} V_{BD}{}^2 \approx E_{LX} = 0.5 L_X i_{LX(PK)}{}^2. \quad (8)$$

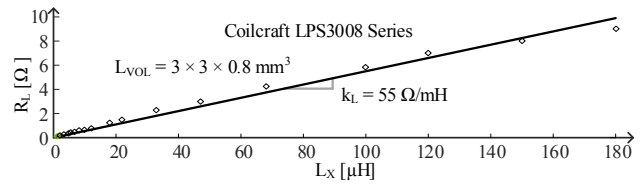

Fig. 6. Inductance and resistance for a 3 × 3 × 0.8 mm^3 inductor.

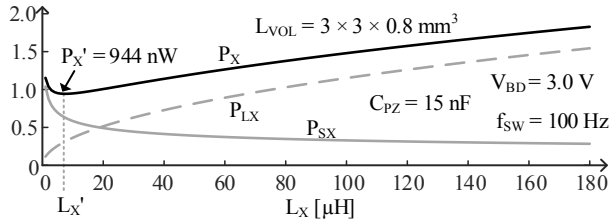

Fig. 7. Power loss on inductor L_X, switch S_X, and total for the recycler.

The period of the LC oscillation is so short compared with a vibration period that the transition looks instantaneous in Fig. 2, as highlighted by the gray region labeled at t_X. The ohmic loss on R_{LX} is

$$\begin{aligned} P_{R(LX)} &= {i_{LX(RMS)}}^2 R_{LX}\left(\frac{t_C}{t_{VIB}}\right) \\ &= \frac{1}{2}\left(\frac{C_{PZ}{V_{BD}}^2}{L_X}\right)(L_X k_L)\left(\frac{0.5\sqrt{2\pi L_X C_{PZ}}}{t_{VIB}}\right), \\ &= K_{R(LX)}\sqrt{L_X} \propto \sqrt{L_X} \end{aligned} \tag{9}$$

where k_L is the ratio of R_{LX} to L_X, and $K_{R(LX)}$ is the coefficient. Since the inductor is limited to a 3 × 3 × 0.8 mm³ box, inductance increases with the number of turns, which leads to higher series resistance. To better demonstrate the optimization, DC resistance values are used for derivations. As shown in Fig. 6, where the solid line is a linear approximation of the values of inductance and resistance, the coefficient $k_L$is 55 Ω/mH. Since L_X is the only variable in the final expression, we can simplify and see that loss of L_X is proportional to square root of L_X.

Similarly, the ohmic loss on S_X is

$$\begin{aligned} P_{R(SX)} &= {i_{LX(RMS)}}^2 R_{SX}\left(\frac{t_C}{t_{VIB}}\right) \\ &= \frac{1}{2}\left(\frac{C_{PZ}{V_{BD}}^2}{L_X}\right)R_{SX}\left(\frac{0.5\sqrt{2\pi L_X C_{PZ}}}{t_{VIB}}\right), \\ &= \frac{K_{R(SX)}}{W_{SX}\sqrt{L_X}} \propto \frac{1}{W_{SX}\sqrt{L_X}} \end{aligned} \tag{10}$$

where $K_{R(SX)}$ is the constant coefficient. Interestingly, the ohmic loss on R_{LX} increases with higher L_X, but the ohmic loss on S_X decreases with higher L_X. That is because although higher L_X means lower peak inductor current, the transfer time increases with L_X, and R_{LX} also increases with L_X, but R_{SX} is completely decoupled with L_X.

From (3), the switch S_X also consumes charge loss that is proportional with W_{SX}, From Section III, the total loss on S_X is at its minimum when $P_{R(SX)} = P_{C(SX)}$, and from (6) the total loss P_{SX} is the least when

$$\begin{aligned} P_{SX}' &= 2\sqrt{K_{R(MOS)}K_{C(MOS)}} = 2\sqrt{\left(\frac{K_{R(SX)}}{\sqrt{L_X}}\right)K_{C(MOS)}} \\ &= \frac{K_{SX}}{{L_X}^{0.25}} \propto \frac{1}{{L_X}^{0.25}} \end{aligned} . \tag{11}$$

where K_{SX} is the coefficient. From (9) and (11), we can see that increasing L_X would result in higher loss on the inductor, but lower loss on the switch. Therefore, we increase L_X until the gain in $P_{R(LX)}$ cancels the reduction in P_{SX}

$$\begin{aligned} \frac{dP_X}{dL_X} &= \frac{dP_{R(LX)}}{dL_X} + \frac{dP_{SX}}{dL_X} \\ &= \frac{0.5K_{R(LX)}}{\sqrt{L_X}} - \frac{K_{SX}}{4{L_X}^{0.25}} = 0 \end{aligned} . \tag{12}$$

As shown in Fig. 7, the total loss on the recycler is 944 nW with an optimum L_X' = 7 μH, and W_{SX}' = 9.8 mm.

5. Optimize MPP Switched Inductor

The last part of the power stage is the MPP switched-inductor (SL) charger that regulates the rectifying voltage at just under V_{BD} and charges the battery v_B. It is needed because P_{PZ} is proportional to the rectifying voltage, so it cannot directly connect to the battery, whose voltage varies from 0 to V_{BD}.

A buck-boost converter is used to lower loss. Switches S_R and S_{GO} close to establish energizing voltage v_E, which is v_R near V_{BD}, to energize the inductor L_O over energizing time t_E:

$$t_E = \left(\frac{\Delta i_{LO}}{v_E}\right)L_O . \tag{13}$$

where Δi_{LO} is the peak to peak inductor current, shown in Fig. 8 and Fig. 10. Similarly, switches S_{GR} and S_O close to drain L_O with draining voltage v_D equals v_O across draining time t_D:

$$t_D = \left(\frac{\Delta i_{LO}}{v_D}\right)L_O . \tag{14}$$

A buck-boost can operate in either continuous conduction mode (CCM) and discontinuous conduction mode (DCM), and they need to be analyzed individually.

a. CCM

In continuous conduction mode [16], the inductor conducts current the entire switching cycle t_O, as shown in Fig. 8. Therefore, the power transferred by the inductor is its maximum energy minus its minimum energy

$$\begin{aligned} P_O &\approx \left(E_{L(MAX)} - E_{L(MIN)}\right)f_O \\ &= 0.5L_O\left({i_{LO(MAX)}}^2 - {i_{LO(MIN)}}^2\right)f_O \\ &= L_O i_{LO(AVG)}\Delta i_{LO} f_O \approx P_{PZ} - P_X - P_B \end{aligned} , \tag{15}$$

where $i_{LO(AVG)}$ is the average inductor current, and $f_O = 1/t_O$ is the switching frequency. The energy transferred is also the drawn power from the piezoelectric transducer minus the losses on the recycler and the bridge.

Again, the transfers are not lossless. The inductors resistance R_{LO} burns ohmic power

$$\begin{aligned} P_{R(LO)} &= {i_{LO(RMS)}}^2 R_{LO} = \left({i_{LO(DC)}}^2 + {i_{LO(AC.RMS)}}^2\right)R_{LO} \\ &= \left[{i_{LO(AVG)}}^2 + \left(\frac{0.5\Delta i_{LO}}{\sqrt{3}}\right)^2\right]L_X k_L \end{aligned} . \tag{16}$$

The energizing switches S_{EI} and S_{EG} burn ohmic power

$$P_{R(EI/G)} = i_{LO(RMS,E)}{}^2 R_{EI/G}\left(\frac{t_E}{t_{SW}}\right) \propto \frac{i_{LO(AVG)}{}^2 + \left(\frac{0.5\Delta i_{LO}}{\sqrt{3}}\right)^2}{W_{EI/G}}, \quad (17)$$

where $i_{LO(RMS,E)}$, $R_{EI/G}$, and $W_{EI/G}$ are the RMS current, resistance, and width of S_{EI} and S_{EG}. Similarly, draining switches S_{DG} and S_{DO} burn

$$P_{R(DG/O)} = i_{LO(RMS,D)}{}^2 R_{DG/O}\left(\frac{t_D}{t_{SW}}\right) \propto \frac{i_{LO(AVG)}{}^2 + \left(\frac{0.5\Delta i_{LO}}{\sqrt{3}}\right)^2}{W_{DG/O}}, \quad (18)$$

where $i_{LO(RMS,D)}$, $R_{DG/O}$, and $W_{DG/O}$ are the RMS current, resistance, and width of S_{DG} and S_{DO}. All four switches require charge loss

$$P_{C(SW)} = q_C v_{DD} f_O \propto W_{E/D} f_O . \quad (19)$$

From (6), the loss on all the switches P_{SW} is

$$P_{SW} = \sum P_{SE/D} \propto \sqrt{\left[i_{LO(AVE)}{}^2 + \left(\frac{0.5\Delta i_{LO}}{\sqrt{3}}\right)^2\right]} f_O \quad (20)$$

The total loss is the sum of (16) and (20), and with the help of (11), it can be reduced to a function of 2 variables, i.e. L_O and f_O. Since L_O is limited to 1 µH to 180 µH, by setting L_O and sweeping f_O, it is shown in Fig. 9 that the optimal CCM charger is with the following settings: L_O' is 180 µH, f_O' is 111 MHz, R_{LO}' is 10 Ω, $i_{LO(AVG)}$ ' is 38.2 µA, Δi_{LO}' is 50 µA. With the operation set, switches can be optimized from Section III, with W_{EI}' at 1.2 µm, W_{EG}' at 860 nm, W_{DG}' at 1.2 µm, W_{DO}' at 1.5 µm, and total loss is 7.5 µW. Note that the width for 2 energizing switches are different, and similarly the width for 2 energizing switches are different, because S_{EI} and S_{DO} are PMOS, and S_{EG} and S_{DG} are NMOS.

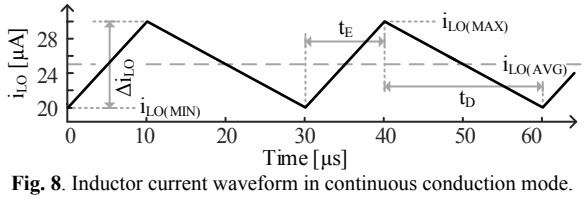

Fig. 8. Inductor current waveform in continuous conduction mode.

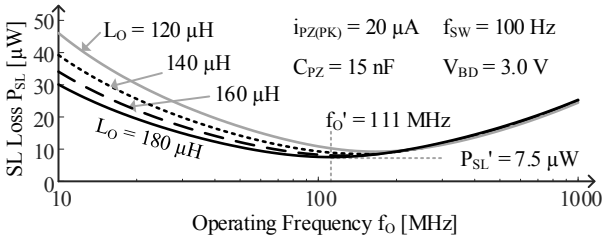

Fig. 9. Total loss on optimized SL in CCM for different inductances.

b. DCM

In discontinuous conduction mode [17], on the other hand, the inductor does not conduct current across the entire switching cycle. Instead, the inductor is energized from 0 to $i_{LO(PK)}$ across t_E, and drained across t_D. After that, it stays at 0 current, until the next switching cycle begins, as Fig. 10 shows. The input power is the power from the piezoelectric transducer minus the losses on the recycler and the bridge, and the energy transferred by the inductor is approximately the peak energy it holds:

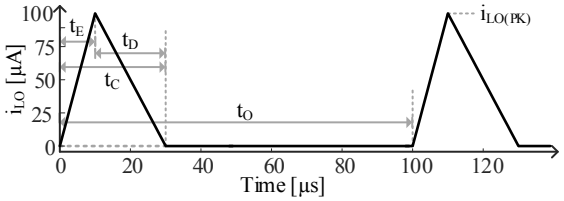

Fig. 10. Inductor current waveform in discontinuous conduction mode.

$$P_O \approx 0.5 L_O i_{LO(PK)}{}^2 f_O - P_{SL} \approx P_{PZ} - P_X - P_B - P_{SL}, \quad (21)$$

where PSL is the loss on the SL. Since drawn power P_{PZ}, loss on the recycler P_X, and loss on the bridge P_{BRG} are all known variables for the SL, the term $L_O i_{LO(PK)}{}^2 f_O$ is a constant

$$L_O i_{LO(PK)}{}^2 f_O \approx 2(P_{PZ} - P_X - P_B). \quad (22)$$

The switched inductor in DCM still consumes ohmic loss on the inductor's resistance:

$$\begin{aligned} P_{R(LO)} &= i_{LO(RMS)}{}^2 R_{LO} = \left(\frac{i_{LO(PK)}}{\sqrt{3}}\right)^2 R_{LO}\left(\frac{t_C}{t_O}\right) \\ &= \left(\frac{i_{LO(PK)}}{\sqrt{3}}\right)^2 (L_O k_L)\left[\left(\frac{L_O}{v_E} + \frac{L_O}{v_D}\right) i_{LO(PK)}\right] f_O . \\ &\propto i_{LO(PK)}{}^3 L_O{}^2 f_O = 2\left(P_{PZ} - P_X - P_B\right) i_{LO(PK)} L_O \\ &\propto i_{LO(PK)} L_O \end{aligned} \quad (23)$$

The last step is because from (21), $L_O i_{LO(PK)}{}^2 f_O$ is constant. It also burns ohmic loss on the energizing switches S_{EI} and S_{EG}

$$\begin{aligned} P_{R(EI/G)} &= i_{LO(RMS,E)}{}^2 R_{EI/G} = \left(\frac{i_{LO(PK)}}{\sqrt{3}}\right)^2 \left(\frac{t_E}{t_O}\right) R_{EI/G} \\ &= \left(\frac{i_{LO(PK)}}{\sqrt{3}}\right)^2 \left(\frac{i_{LO(PK)} L_O}{v_E}\right) f_O R_{EI/G} \\ &\propto \frac{L_O i_{LO(Pk)}{}^3 f_O}{W_{EI/G}} = 2\left(P_{PZ} - P_X - P_B\right) \frac{i_{LO(Pk)}}{W_{EI/G}} \\ &\propto \frac{i_{LO(Pk)}}{W_{EI/G}} \propto \frac{K_{R(MOS)}}{W_{EI/G}} \end{aligned} \quad (24)$$

Therefore, ohmic loss coefficient $K_{R(MOS)}$ is proportional to $i_{LO(PK)}$. Similarly, the draining switches S_{DG} and S_{DO} burn ohmic power

$$P_{R(DG/O)} = i_{LO(RMS,D)}{}^2 R_{DG/O} = \left(\frac{i_{LO(PK)}}{\sqrt{3}}\right)^2 \left(\frac{t_D}{t_O}\right) R_{DG/O}$$
$$= \left(\frac{i_{LO(PK)}}{\sqrt{3}}\right)^2 \left(\frac{i_{LO(PK)} L_O}{v_D}\right) f_O R_{DG/O}$$
$$\propto \frac{L_O i_{LO(Pk)}{}^3 f_O}{W_{DG/O}} \propto 2\left(P_{PZ} - P_X - P_B\right) \frac{i_{LO(Pk)}}{W_{DG/O}}$$
$$\propto \frac{i_{LO(Pk)}}{W_{DG/O}} \propto \frac{K_{R(MOS)}}{W_{DG/O}} \quad . \quad (25)$$

Again, the second to last step of (24) and (25) is because from (22), $L_O i_{LO(PK)}{}^2 f_O$ is a constant. The charge loss is the same as the CCM case in (19), and $K_{C(MOS)}$ is proportional to f_O. Therefore, the balanced ohmic loss and charge loss result in the optimum switch with total loss P_{SW}'

$$P_{SW}' = \sum P_{S(E/D)} = \sum 2\sqrt{K_{R(MOS)} K_{C(MOS)}}$$
$$\propto \sqrt{i_{LO(PK)} f_O} = \frac{\sqrt{L_O i_{LO(PK)}{}^2 f_O}}{\sqrt{i_{LO(PK)} L_O}} \propto \frac{1}{\sqrt{i_{LO(PK)} L_O}} \quad . \quad (26)$$

The total loss on the SL is the sum of (23) and (26), and there is an optimum $i_{LO(PK)}L_O$ that yields the lowest total loss on the SL. In other words, no matter what inductor we choose, we can always modify to switches and controller accordingly such that it is least lossy, shown in the thick solid black trace in Fig. 11. The loss stays flat because for each inductance value, the $i_{LO(PK)}$ is inversely proportional to L_O so that their product stays constant. As a result, from (22), f_O is also proportional to L_O. It consumes P_{SL}' = 2.11 µW in the following optimal settings: L_O' is 130 µH, R_{LO}' is 7.2 Ω, f_O' is 40 kHz, and $i_{LO(PK)}$' is 3.9 mA. With the waveforms set, the optimum switch size can be obtained from Section III: $W_{EI,G}$' is 459 µm and $W_{DG,O}$' is 640 µm. The thin traces in Fig. 11 also show the optimized losses with different inductor volume constraint. Therefore, DCM is less lossy than CCM, while operating at a much lower frequency, so we would operate it at DCM.

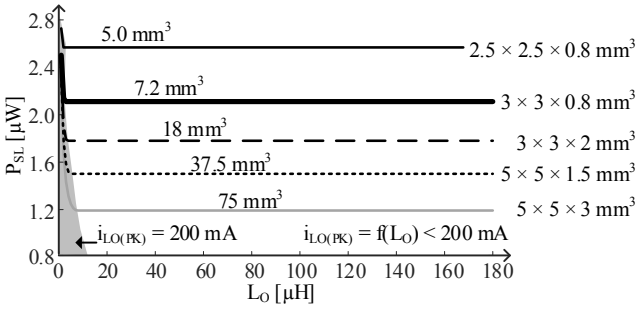

Fig. 11. Total loss on optimized SL in CCM for different inductor volumes.

6. Overall Performance

From the previous three sections, the optimum piezoelectric charger when the vibration provides 20 µA on the transducer is built. The charger draws 38.2 µW from P_{PZ}, and loses 944 nW on the recycler, 4.6 nW on the bridge, and 2.11 µW on the SL, resulting in an overall efficiency of 92%. Simulation of the circuits consumes 990 nW on the recycler, 8.6 nW on the bridge, and 2.35 µW on the SL, resulting in an overall efficiency of 91 %. Repeating the same process for $i_{PZ(PK)}$ from 1 µA to 50 µA, the results are presented in Fig. 12. P_{PZ}, P_{SL}, and P_D all scale linearly with vibration strength, but P_X does not. That is because the recycler operation is the same across all conditions, and the loss also remains the same.

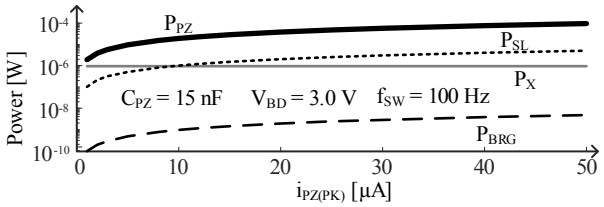

Fig. 12. Drawn power and optimized losses across vibration strength.

Increasing volume of the inductor can reduce the loss on the recycler P_X and switched inductor P_{SL}, as shown in Fig. 13. The efficiency stays above 90% for all inductor sizes and reaches 95% with a 5 × 5 × 3 mm³ inductor. Choosing the largest inductor the application allows yields the highest efficiency.

Table 1 lists and compares the technology used, components, power level, and performance for the design in this paper and several state-of-the-arts. Despite constraint to the smallest inductor, the aforementioned design has the highest efficiency, and the design guideline should be followed for all future recycling bridge designs.

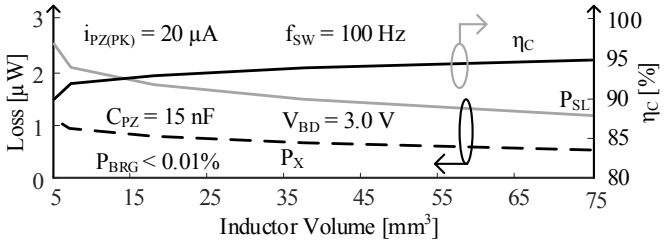

Fig. 13. Total loss on optimized SL in CCM for different inductor volumes.

Table 1. Performance Comparison with the State of the Art.

	JSSC 10' [8]	TPE 19' [11]	ISSCL 20' [12]	This Work
L_{MIN} [nm]	500	350	130	300
V_{BD} [V]	5.0	5.0	3.3	3.0
$\Delta v_{PZ(OC)}$ [V]	4.8	5.0	3.2	4.3
f_{VIB} [Hz]	225	225	143	100
L_X [µH]	22	3300	3300	7; 130
R_L [Ω]	N/A	1.8	N/A	0.9; 6
P_{PZ} [µW]	36	53	31	38.2
η_C	88%	95%	90%	92%

7. Conclusions

The optimized recycling bridge power stage with 92% efficiency has been theorized and designed. To optimize the power switches, width of the device should be selected such that the ohmic loss equal the charge loss. On the recycler, we increase inductance until the gain in the loss on the inductor cancels the reduction on the switch. On the switched inductor, DCM performs better than CCM. In the end, the optimized power stage can be implemented to power internet of things and microsensors to extend life and expand functionality.

ACKNOWLEDGMENT

The authors thank Dr. Lazaro, Dr. Blanco, Dr. Morroni, and Texas Instruments for their sponsorship and support.

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