

Low-output-impedance 0.6 μm CMOS sub-bandgap reference

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A 0.6 μm CMOS sub-bandgap reference circuit, the output voltage of which is, unlike reported in the literature, concurrently low voltage and low output impedance, is presented. Experimental measurements verify that the proposed circuit, which produces a first-order temperature-compensated reference voltage of 890 mV, sources up to 5 mA of load current and rejects noise by a factor of 30.8–8.1 dB at 500 kHz–4 MHz, neither of which feature is achieved by state-of-the-art sub-bandgap circuits.

Introduction: A low-output-impedance reference is desirable for noise-sensitive applications to shunt and steer noise away from sensitive nodes and source DC and AC load currents [1, 2], which is why most of the references used in industry are variations of the regulated references presented in [3]. Reported regulated references, however, only produce the conventional 1.2 V bandgap voltage, or a higher voltage [1–5], which is unsuitable for a growing number of high-end applications that use modern CMOS processes with low breakdown voltages. Alternatively, as shown in Fig. 1, a series linear regulator can buffer the output of a low-voltage high-output-impedance reference [6, 7].

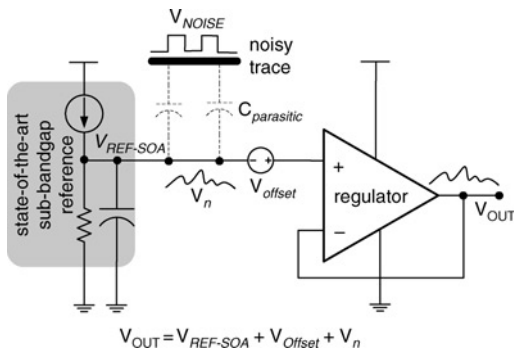


Fig. 1 Reference-regulator low-impedance circuit and its adverse treatment of noise and offset

The buffer, however, introduces additional random and systematic offset components to the reference, significantly degrading the overall accuracy performance of the system; these offsets, for instance, caused an additional ±4 mV error in [2]. This additional error, which monopolises 0.4% of a 1 V reference, leaves little error budget for the reference itself, which is particularly troubling in CMOS technologies because MOS offsets have a nonlinear dependence on temperature and cannot be compensated for with trim. Moreover, a buffer does little to attenuate the noise already present in the high-impedance reference, since it simply propagates the disturbance to the output unabated. Generating a sub-bandgap reference voltage with low-output-impedance characteristics, for which no prior art solution was found to exist, is the objective of this Letter.

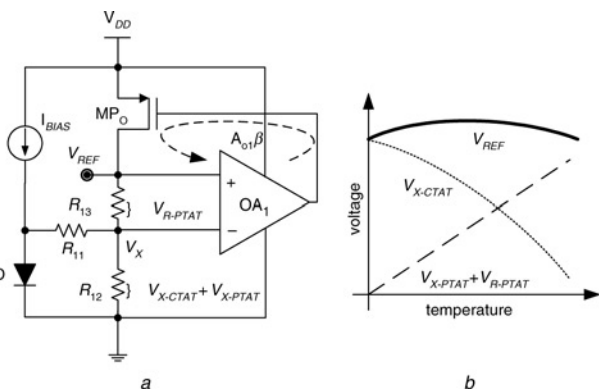


Fig. 2 Concept and temperature behaviour of proposed reference
a Concept
b Temperature behaviour

Proposed topology: For shunt feedback, which is necessary for low output impedance, the reference must be the sum of temperature-dependent voltages (not currents), as shown in the proposed circuit of Fig. 2a, where a proportional-to-absolute temperature (PTAT) voltage is sampled and regulated via amplifier OA₁ and power PMOS MP_O. The forward-biased voltage of diode D decreases, for the most part, linearly with temperature and hence has a complementary-to-absolute-temperature (CTAT) behaviour. This CTAT voltage is attenuated by the potential divider comprised of resistors R₁₁ and R₁₂ to produce CTAT voltage component V_{X-CTAT} at node V_X.

The amplifier has a preset PTAT offset voltage and the loop regulates and impresses this voltage across R₁₃. The temperature-compensated output, shown in Fig. 2b, is the sum of this PTAT voltage (V_{R-PTAT}), the CTAT diode-derived voltage across R₁₂ (V_{X-CTAT}), and the additional PTAT voltage component across R₁₂ (V_{X-PTAT}), that results from running R₁₃ PTAT current through R₁₂ (V_{X-PTAT}) and is given by

$$V_{REF} = V_{R-PTAT} + (V_{X-PTAT} + V_{X-CTAT}) = V_{PTAT} + V_{CTAT} \quad (1)$$

Amplifier OA₁ and pass device MP_O constitute the high loop-gain, shunt-feedback path (A_{ol}β) around V_{REF}. This negative feedback loop regulates the output against variations in input supply and load. Since MP_O is a large PMOS device, the regulated reference can sustain low supply voltages under relatively high load currents, in other words, yield low dropout voltages.

Complete schematic: The complete circuit shown in Fig. 3 comprises a biasing block and the output stage and amplifier shown in Fig. 2. The bias current is defined by a conventional PTAT generator block. The dominant low-frequency pole of the loop is established at the gate of MP_O through the Miller-compensating capacitor C_M.

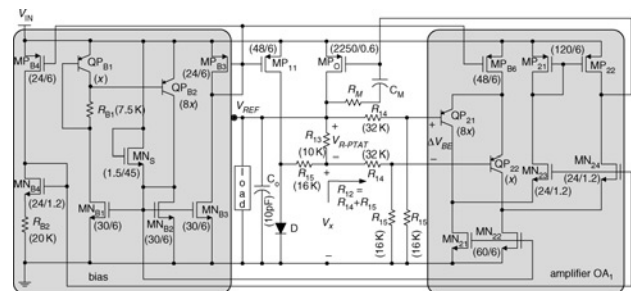


Fig. 3 Complete schematic of proposed low-impedance sub-bandgap reference

Key to this circuit is OA₁'s PTAT offset voltage, which is intrinsically defined by input pair QP_{21–22}, whose emitter areas are 8x and x, respectively, and current mirror MP_{21–22}, which ensures equal currents flow through QP_{21–22}. The result is a PTAT difference across their base-emitter voltages (i.e. ΔV_{BE} = V₇ln(8)). The offset voltage across the bases of QP_{21–22} is the voltage-divided version of the voltage across R₁₃ (V_{R-PTAT}); or equivalently, V_{R-PTAT} is an amplified version of the PTAT voltage present at the bases of QP_{21–22}:

$$V_{R-PTAT} = \left(\frac{R_{14} + R_{15}}{R_{15}} \right) \Delta V_{BE} \quad (2)$$

This voltage defines R₁₃'s PTAT current, which ultimately flows into node V_X. Resistors R₁₄ and R₁₅ therefore implement a voltage divider circuit whose total resistance and series combination is modelled by R₁₂. The first-order temperature-compensated reference voltage is consequently given by

$$V_{REF} = K_1 V_{BE} + K_2 K_3 \Delta V_{BE} = K_1 \left(V_{BE} + \frac{K_2 K_3}{K_1} \Delta V_{BE} \right) \quad (3)$$

where K₁, K₂, and K₃ are given by

$$K_1 = \frac{(R_{14} + R_{15}) \parallel R_{12}}{[(R_{14} + R_{15}) \parallel R_{12}] + R_{11}} \quad (4)$$

$$K_2 = \frac{R_{14} + R_{15}}{R_{15}} \quad (5)$$

$$K_3 = 1 + \frac{R_{11} \parallel R_{12} \parallel (R_{14} + R_{15})}{R_{13}} \quad (6)$$

The lateral *pnp* devices of the process were characterised for parameters like forward beta (BF), early voltage (V_{AF}), and saturation current (I_S), among others. The values of these parameters were found to be 100 A/A, 6 V, and 3 fA, respectively. This high beta allows base currents to be neglected while deriving (2)–(6).

Results: The proposed circuit was fabricated with AMI's 0.6 μm CMOS process technology ($V_{TN} \approx 0.7$ V and $|V_{TP}| \approx 0.9$ V) through the MOSIS design facility. The temperature coefficient of 20 samples, with a sub-bandgap output of 890.5 mV, is shown in Fig. 4a. The transient load-induced variation of the reference when subjected to a load current step of 0–5 mA with 100 ns rise and fall times, shown in Fig. 4b, is a measure of the circuit's ability to suppress load-dump effects. To gauge the noise-shunting capabilities of the proposed circuit against the state-of-the-art, a current-mode 890 mV sub-bandgap reference was built by sourcing 49 μA into an 18 k Ω –10 pF output resistor–capacitor combination, as shown in Fig. 5a. To emulate noise injection through parasitic coupling capacitors, a noise current of roughly 125 μA was injected into the reference (state-of-the-art $V_{REF-SOA}$ and proposed V_{REF}), as shown in Figs. 5a and b. A comparison of the transient response of the two circuits (Fig. 5c) shows how the proposed reference suppresses most of the broadband AC noise injected, quickly recovering its output to the desired level. The frequency spectra of the two waveforms (Fig. 5d) reveal that the proposed circuit (V_{REF}) further rejects noise by a factor of 30.8–8.1 dB ($V_{REF-SOA}$ -to- V_{REF} noise power ratio) at 500 kHz–4 MHz.

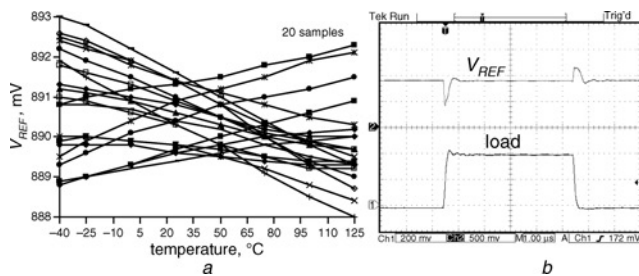


Fig. 4 Temperature dependence of trimmed samples and transient load regulation

a Temperature dependence
b Transient load regulation

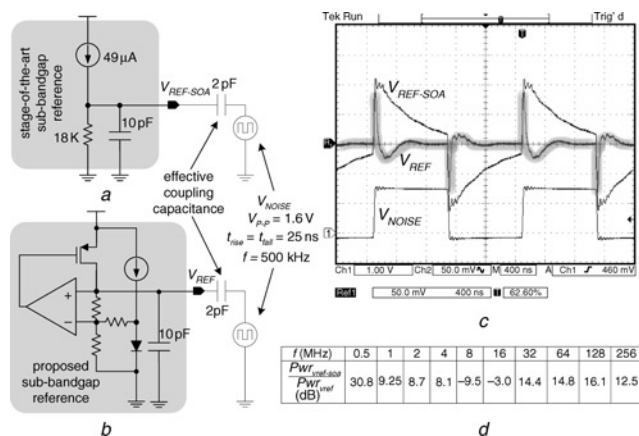


Fig. 5 Noise rejection measurements: setup for state-of-the-art sub-bandgap reference and proposed circuit and corresponding AC-coupled transient and frequency ($V_{REF-SOA}$ -to- V_{REF} noise power ratio) response

a State-of-the-art sub-bandgap reference
b Proposed circuit
c AC-coupled transient
d Frequency response

Conclusions: A 0.9 V, 34.7 ppm/ $^{\circ}\text{C}$, 5 mA, low-output-impedance 0.6 μm CMOS sub-bandgap reference has been designed, fabricated and evaluated. The principal features of the proposed circuit are low impedance and sub-bandgap output voltages, concurrently, the combination of which was not found in the literature, patents or commercial products without the use of series shunt-regulators, which degrade accuracy.

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