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A Low Voltage, Rail-to-Rail, Class AB CMOS Amplifier With High Drive and Low Output Impedance Characteristics

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Abstract-- This paper describes a CMOS rail-to-rail class AB operational amplifier designed to have extremely low output impedance and large current-drive capability. The amplifier uses an innovative output stage, having both source follower and common source stages working simultaneously throughout the output common-mode range. The source follower ensures low output impedance, which enables it to drive relatively large load capacitors, while the common-source gain stage provides high current drive. Furthermore,

the circuit is fully functional with supplies as low as 1.5 V. The amplifier is capable of driving a maximum output current of ± 7 mA with only 140 mA of quiescent current, making it power efficient and, therefore, appropriate for low voltage battery-powered applications.

***Index Terms*-- Class AB, rail-to-rail, low output impedance, low voltage, operational amplifier, power efficient.**

I - INTRODUCTION

Class AB output stages are increasingly popular in today's low voltage battery-powered electronics where amplifier applications demand high efficiency as well as rail-to-rail operation. In the era of portable equipment, low supply voltage and low power consumption are intrinsic traits [1]. Performance requirements are also becoming more stringent, leaving the designer with more difficult specifications to fulfill and less flexibility with which to do it. For instance, low output impedance is generally desired, but classical source-follower configurations are not allowed in low voltage applications. Dynamic range is already limited by low battery voltages and source followers take too much of that range away to be viable solutions. In fact, most low voltage class AB output stages have inherently high output impedance because they necessarily employ common-source configurations [2-4]. On the other hand, amplifiers with source follower output stages typically suffer from output voltage swing limitations, which are severe in low voltage applications. Ideally, though, one would like to combine the characteristics of source-followers and common-source gain stages in the same circuit to achieve low output impedance, rail-to-rail operation, and high current-drive capability. The one previously reported topology that implements this combination is not a low voltage solution and, moreover, has load-range

limitations [5]. The amplifier described in this paper, however, combines common-source gain stages and source-followers to achieve true class AB operation with low output impedance while still producing a rail-to-rail output voltage swing. In light of today's market, the amplifier is designed to operate with low supply voltages and low quiescent current.

The basic circuit topology of the proposed amplifier is presented in Section II. Section III discusses the circuit realization, detailing the input stage, the gain stage, and the output stage. Common-mode feedback, rail-to-rail control, and compensation are also discussed in this section while highlighting optimum operating conditions. In Section IV, simulated results are presented and discussed. The circuit is subsequently compared to other state-of-the-art designs. Finally, conclusions are drawn in Section V.

II - PROPOSED ARCHITECTURE

The basic circuit topology of the class AB amplifier is shown in Fig. 1. The voltage amplifier with gain A_V drives the output stage with separate dual in-phase signals. The output stage consists of a high side driver (HSD) circuit, which is capable of sourcing large amounts of current to load Z_L , and a low side driver (LSD) circuit, capable of sinking large amounts of load current. The high current devices, M_{PD} in the HSD and M_{ND} in the LSD, are connected in a common-source configuration, allowing the output to reach the supply rails as in most low-voltage class AB output stages. In this output stage, however, the output is also connected to source-followers. Both the HSD and the LSD circuits are closed-loop feedback networks. The two feedback loops lower the effective output impedance of the output stage, already the reciprocal of the transconductance, by approximately the loop gain. The Common-Mode Feedback (CMFB) circuit insures that the drivers operate in true class AB mode. It performs this

task by sensing the respective output currents and feeding a control signal back to the main forward loop. The CMFB circuit essentially controls the quiescent biasing conditions of the power transistors.

Fig. 2(a) shows a more detailed circuit diagram of the LSD circuit, without the CMFB portion. Current I_1 is designed to be greater than I_2 . Then, assuming all devices are biased in the saturation region, the current difference, $I_1 - I_2$, flows through source-follower transistor M_{NF} and into driver transistor M_{ND} . Unlike most class AB output stages, the gate of the high current transistor is controlled indirectly through the feedback loop, which is comprised of M_{NF} , M_{PB} , and M_{ND} .

To demonstrate how the feedback loop operates, a fast transient decrease in voltage at V_{IN} is considered. When V_{IN} decreases, more of I_1 is steered into M_{PB} , thereby increasing the voltage at the gate of M_{ND} which, in turn, causes M_{ND} to sink additional current. Subsequently, V_{OUT} is lowered until the gate-source voltage of M_{NF} once again reaches its steady-state value. The overall result, with respect to forward gain, is that the driver circuit behaves similarly to a simple source-follower transistor. One important difference exists, however, in that the output impedance is roughly two orders of magnitude below that of a classical source-follower. Fig. 2(b) shows the ac equivalent circuit used to determine the output resistance, which is given by

$$R_O = \frac{V_t}{I_t} = \frac{V_t}{g_{mF}V_t + g_{mF}V_t r_{o2}g_{mD}} = \frac{1}{g_{mF}(1 + g_{mD}r_{o2})}, \quad (1)$$

where V_t is an ac test voltage applied to the output, I_t is the corresponding test current, g_{mF} is the transconductance of M_{NF} , r_{o2} is the output resistance of current source I_2 , and g_{mD} is the transconductance of M_{ND} . The feedback loop effectively reduces the output impedance of the driver, already $1/g_{mF}$, by a factor of $(1 + g_{mD}r_{o2})$. The ac and dc analysis of the high side driver is analogous to the LSD counterpart.

To drive the HSD and LSD, dual in-phase signals are required. With the help of the CMFB circuit and replication circuits in the input and gain stages, these two signals are generated. The following section describes the circuit operation of each stage.

III - CIRCUIT IMPLEMENTATION

The complete circuit diagram for the class AB amplifier, including the input stage, gain stage, output drivers, and CMFB circuit is shown in Fig. 3. The circuit is biased from a 2 μ A current source, which flows through bias resistor R_{B1} and is mirrored to flow through bias resistor R_{B2} . These resistors provide dc bias voltages for cascode transistors throughout the entire circuit. They are designed to provide enough headroom from either supply rail to insure that all current sources stay in the saturation region, provided that the rail-to-rail supply voltage is greater than about 1.5 V.

A. Input Stage

The input stage of the operational amplifier is similar to the bipolar input stage reported in [6]. It allows rail-to-rail input common-mode range with supply voltages as low as about 1.5 V. Since a detailed analysis of a similar input stage is presented in [6], only a brief intuitive description is offered here. Fig. 4 shows a simplified diagram of the input stage. The PMOS and the NMOS differential input pairs operate in parallel. Three regions of input common-mode operation exist. These include when the input voltage is (1) low enough such that only the PMOS differential pair conducts, (2) high enough such that only the NMOS pair conducts, and (3) in the transition region where both differential pairs conduct current. The PMOS pair accommodates input voltages down to the negative supply, while the NMOS counterpart handles input voltages up to the positive supply.

Both input pairs conduct current in the transition region, so long as the total supply voltage is greater than about 2 V. For supply voltages above 2 V, current I_X in Fig. 4 is zero. The common-mode input signal determines the state of current I_X by turning it on only when both differential pairs approach their common-mode range limits, a state that is determined by the reference voltages impressed on resistors R_{V1} and R_{V2} in Fig. 3. In other words, only when both differential pairs' current sources approach the triode region will current I_X be established. For example, if the supply voltage is 4 V, either or both M_{P013} and M_{N011} would be cut off since both NMOS and PMOS differential pair current source voltages cannot simultaneously approach their triode regions.

For the case of lower supply voltages, level-shift voltages are developed across resistors R_{S1} through R_{S4} . If the supply voltage is 1.5 V and the input voltage is 0.7 V, for example, both M_{P013} and M_{N011} conduct current and I_X is established. For the NMOS pair, the resulting input common-mode voltage is increased thereby insuring proper operation with the given headroom. Similarly, the effective input common-mode voltage of the PMOS pair is decreased. The input resistance of the amplifier remains high because the current sourced into the resistors is simultaneously sunk at the other end. Level shifting the inputs circumvents the condition near the middle of the input range where both input pairs are non-operational, which occurs when

$$V_{CC} - V_{SS} < V_{TN} + V_{TP} + 4V_{DS} . \quad (2)$$

Comparators M_{N011} - M_{N012} and M_{P013} - M_{P014} in Fig. 3 dynamically control the actual magnitude of the level-shift voltage by transferring the appropriate amount of M_{P06} 's current into the level-shift resistors. The input impedance of the input stage, in the end, is only compromised by the mirroring inaccuracies of M_{P08} , M_{P03} , M_{N03} , and M_{N04} , resulting from channel-length modulation effects and transistor mismatches [6].

The input stage also includes circuitry to stabilize transconductance over the common-mode input range. Transistor M_{P09} in Fig. 3 senses the input voltage and functions as a current-steering switch to regulate the amount of tail current in each input pair. At common-mode input voltages near V_{SS} , M_{P09} is off, and all of M_{P02} 's current flows into the PMOS pair. Conversely, at input voltages near V_{CC} , M_{P09} conducts and transfers all of M_{P02} 's current to the NMOS pair via M_{N06} and M_{N07} . This topology is commonly used in bipolar rail-to-rail input stages to achieve constant transconductance over the common-mode input range. In CMOS circuits, however, the resulting transconductance is not constant because of the nonlinear dependence of transconductance upon quiescent current. Instead, the transconductance varies by the square root of two over the entire input range. This is less variation than constant current rail-to-rail CMOS input stages, such as the one reported in [7]. The circuit transconductance is given by

$$g_m = \begin{cases} \sqrt{I\beta} & \uparrow \text{ICMR} \\ \sqrt{2}\sqrt{I\beta} & \text{transition region ,} \\ \sqrt{I\beta} & \downarrow \text{ICMR} \end{cases} \quad (3)$$

where β_N is made to equal β_P ($\beta = k'W/L$).

B. Gain Stage

The amplifier uses a folded-cascode current-summing gain stage with two output branches to provide dual in-phase output voltages for the class AB output stage. The gain stage consists of cascode transistors M_{P12} - M_{P14} and M_{N13} - M_{N15} along with current sources M_{P10} , M_{P11} and M_{N10} - M_{N12} . The output currents from the PMOS and the NMOS input pairs are split by M_{P011} , M_{P012} and M_{P13} , M_{P14} , respectively, and are summed into the gain stage's high impedance output nodes, the dominant high impedance nodes of the main loop.

C. Output Stage with Common Mode Feedback

The inputs to the high side and low side output drivers in Fig. 3 are the gates of M_{PF} and M_{NF} , respectively. Current sources M_{P210} and M_{P211} bias the low side driver while M_{N215} and M_{N216} bias the high side driver, as discussed in Section II. The gates of bias transistors M_{NB} and M_{PB} are tied to the same bias points as the cascode transistors in the amplifier gain stage. The outputs of the drivers share a common connection, which is the output of the operational amplifier.

A simplified diagram of the common-mode feedback circuit is shown in Fig. 5. Current-controlled currents I_{DP} and I_{DN} sink currents proportional to the driver currents, forcing them to flow through resistors R_{CMN} and R_{CMP} . The source follower pair, biased from I_{CM1} , senses the lower of the two currents, in the form of voltages across resistors R_{CMN} and R_{CMP} , and directs the signal to the input of amplifier A_v . The amplifier, in turn, compares this voltage to a reference voltage and feeds back an error signal to the gain stage. In a steady-state no-load condition, the voltage drops across R_{CMN} and R_{CMP} are roughly equal, indicating equal amounts of current through both drivers. In this case, both M_{NCM1} and M_{NCM2} conduct current and insure class AB operation. When the output stage is sourcing or sinking load current, the voltage drops across R_{CMN} and R_{CMP} are not equal. The voltage imbalance causes the source follower corresponding to the larger voltage drop to cut off. The loop then, in essence, regulates to the bwer of the two currents to a point established by I_{CM2} . The magnitude of the steady-state driver quiescent current is thus determined by the current flowing through R_{CMR} and M_{NCMR} . Transistors M_{NCMR} , M_{NCMN} , and M_{NCMP} are designed to nominally have equal gate-source voltages. Consequently, the common-mode feedback circuit forces the voltage across R_{CMN} or R_{CMP} to be equal to the voltage across reference resistor R_{CMR} .

In Fig. 3, dependent current sources I_{DP} and I_{DN} correspond to M_{N26} and M_{NDS} , and are current mirrors designed to reproduce a small fraction of the driver currents (M_{ND} and M_{PD}). Device M_{NDS} mirrors M_{ND} 's current and M_{PDS} mirrors M_{PD} 's current, which is turned around by current mirror M_{N25} - M_{N26} before being applied to R_{CMP} . The CMFB amplifier is made up of input pair M_{P26} and M_{P29} , with common-mode transistors M_{P27} and M_{P28} for biasing. The differential outputs of the error amplifier force a differential current back into the gain stage, thereby modulating the voltage at the inputs of the HSD and LSD circuits and controlling the driver currents.

D. Rail-to-Rail Control

In the HSD, if the output voltage is near the high end of the output voltage range, the HSD functions normally, and the common-mode feedback signal propagates through the source follower and the localized feedback loop to control the driver current. However, as the output voltage decreases, the HSD input p-type source-follower M_{PF} cuts off, breaking the HSD loop. Just before this happens, then, the common-mode error signal must have an alternative path to control the driver current (M_{PD}); otherwise, CMFB control is lost. Transistors M_{N217} - M_{N219} and M_{P23} - M_{P24} provide this alternative path. M_{N217} senses the voltage at the input of the HSD and, when the output voltage is approximately 1.5 V above V_{SS} , the gate-source voltage of M_{N217} is large, M_{P24} is off, and the HSD circuit operates normally, as previously discussed. On the other hand, when the output is within 1.5 V of V_{SS} , M_{N217} starts to conduct less current and, at the point where its current is less than that of M_{P22} , transistors M_{N218} , M_{N219} , M_{P23} , and M_{P24} start conducting current. An alternative signal path is therefore generated and control of M_{PD} is guaranteed throughout the output voltage range. Device M_{N217} is sized such that this condition occurs just before M_{PF} turns off such that the alternative signal path exists before the source

follower path desists. In the end, M_{N217} functions as a linear transconductance amplifier when the output voltage is below 1.5 V. A complementary control circuit is similarly used in the LSD counterpart.

E. Compensation

Since the amplifier topology consists of a single high-impedance gain stage, the dominant low frequency pole must be the high-impedance node. Two of these nodes exist in this case, at the gates of M_{NF} and M_{PF} , but these operate in parallel, so they may be treated as a single node for this analysis. Compensation capacitors C_{C2} and C_{C3} are placed on these nodes to the supplies to insure that these nodes are the dominant poles in the main feedback loop.

The output constitutes the second non-dominant pole. Its frequency is determined by the load capacitor and the effective output impedance, as defined in Equation (1) and given by

$$p_2 \approx \frac{1}{2\pi(Ro_{LSD} \parallel Ro_{HSD})C_L}, \quad (4)$$

where

$$Ro_{LSD} \approx \frac{1}{g_{mNF}g_{mND}r_{ds-N20}} \quad (5)$$

and

$$Ro_{HSD} \approx \frac{1}{g_{mPF}g_{mPD}r_{ds-P20}}. \quad (6)$$

A third, designed to be non-dominant, pole is introduced by the driver loops at the gates of M_{ND} and M_{PD} , high impedance nodes. Intuitively, by inspecting Equations (1) and (5) more carefully, it is evident that the impedance increases at a frequency roughly defined by R_{DS-N20} and C_{GS-ND} . The impedance can be estimated by

$$Ro_{LSD} \approx \frac{[1 + s(r_{ds-N20}C_{GS-ND})]}{g_{mNF}g_{mND}r_{ds-N20}}. \quad (7)$$

In other words, at frequencies greater than the aforementioned pole, R_{OLSD} increases thereby establishing an additional pole in the main forward loop. Resistance R_{OLSD} behaves in a similar fashion. However, to insure stability of the local loops, the pole at this node is made dominant, being the only high impedance node in the loop. Simultaneously, though, to insure stability of the overall loop, this pole cannot be too low, otherwise overall phase margin of the main loop is compromised. Capacitors C_{C1} and C_{C4} were added for this reason. The reason behind resistors R_{C1} and R_{C2} and their connections to the gates of M_{NF} and M_{PF} have to do with the stability of the CMFB circuit.

The CMFB loop has two high impedance nodes, the one shared with the main loop, at the gates of M_{NF} and M_{PF} , and one within the drivers themselves, at the gates of M_{ND} and M_{PD} . For the CMFB circuit, the ac signals propagate through the drivers via source followers M_{NF} and M_{PF} , which lead to the low impedance sources of M_{PB} and M_{NB} and, ultimately, to the high impedance gates of M_{ND} and M_{PD} , before converting it to a current back in the CMFB circuit. Thus, for this loop to be stable, Miller compensation is used to split the two poles, which is why C_{C1} and C_{C4} are connected back to the gates of M_{PF} and M_{NF} . Resistors R_{C1} and R_{C2} were added to bring the Right-Half Plane (RHP) zeros back into the Left-Half Plane (LHP) to help optimize phase margin. The gates of M_{NCMP} and M_{NCMN} constitute the third non-dominant poles of this loop. Since their respective resistances and associated capacitor values are low, they are easily kept at high frequencies. It is noted that when the alternative signal paths in the rail-to-rail control circuit (M_{N217} and M_{P214}) are used, no high impedance poles are added thereby preserving the stability conditions of the CMFB loop.

F. Optimum Operation

The amplifier's closed-loop output impedance can be estimated by dividing the result of Equation (1) by the gain of the main feedback loop,

$$R_{O-CL} \approx \frac{R_{O-LSD} // R_{O-HSD}}{A_V} \leq \frac{1}{g_{mF02} g_{mD} A_V}, \quad (8)$$

where R_{O-LSD} and R_{O-HSD} are the output resistance of the LSD and HSD circuits, respectively. Clearly, for this approximation to be valid over the entire output voltage range, either the HSD or LSD must be functioning regardless of output voltage; otherwise, the output resistance of the drivers degrade since the localized feedback loop is broken. This requires that the supply voltage be large enough to allow the HSD to assume control of the output before the LSD cuts off, and vice versa. Closer inspection of the output stage and rail-to-rail control circuitry reveals this condition is attainable only when the total supply voltage is greater than about 3.2 V. For the HSD to function as described in Section II, V_{OUT} must be at least $V_{TN} + V_{TP}$ greater than V_{SS} , as mandated by M_{PF} and M_{N217} . Similarly, in the LSD, V_{OUT} must be at least $V_{TN} + V_{TP}$ below V_{CC} , as mandated by M_{P214} and M_{NF} . Otherwise the follower would be cut off and the alternate CMFB path would be activated. Thus, to insure that one driver circuit is always on, even in the middle of the range where the limitation is worst, the supply voltage should be roughly greater than 3.2 V,

$$V_{CC} - V_{SS} \geq 2V_{TN} + 2V_{TP} + 4V_{DS}. \quad (9)$$

Coincidentally, when the input voltage is lower than 3.2 V, the circuit still has very low output impedance, since the output node is still part of the CMFB feedback loop through the alternate CMFB path.

IV - SIMULATED RESULTS

The amplifier was simulated and compared with other state-of-the-art class AB amplifiers. A summary of this comparison is given in Table 1. The proposed circuit has the best peak output-current performance as well as the lowest quiescent-current flow, in other words, best efficiency, which is important in battery-operated environments. It is also capable of working down to supply voltages of 1.5 V, the lowest of the competing amplifiers surveyed. Other parameters were similar. Open-loop gain was lower in the proposed circuit, however, since a single gain-stage topology was used.

Fig. 6 shows the current through driver transistors M_{ND} and M_{PD} as a function of common-mode output voltage, with a 1.5 V supply in Fig. 6(a) and a 6 V supply in Fig. 6(b). These plots demonstrate the true class AB behavior of the output stage over the full range of supply voltages. The input stage transconductance is shown in Fig. 7 as a function of the input common-mode voltage. The left side of the hump is the region where the PMOS differential pair is conducting and the right side is where the NMOS pair is conducting. As predicted, transconductance increases when both input pairs conduct and the peak g_m is exhibited. Since the region for which both differential pairs conducted was narrow, the estimated peak transconductance was not attained; instead, a lower, less variable, response was shown.

The ac characteristics of the amplifier are shown in Fig. 8. Fig. 8(a) shows how the circuit gain varies with common-mode input voltage. Since g_m is relatively constant, the gain variations mostly reflect changes in the output impedance of the gain stage, which are present due to modulation of the common-mode feedback signal. Fig. 8(b) shows supply rejection as a function of frequency for several different output voltages.

Fig. 9 shows the amplifier's response to a pulse on the input when configured for unity gain. Fig. 9(a) shows a rail-to-rail input pulse with a 1.5 V supply and the amplifier's rail-to-rail response when loaded with 10 k Ω and 100 pF. The output voltage is limited only by the required drain-source voltages of the driver transistors, M_{ND} and M_{PD} . In Fig. 9(b), the pulse goes from -1 to 1 V and the output is connected to a 350 Ω / 100 pF load to ground to show the circuit's behavior as it is forced to quickly go from sinking to sourcing current. The propagation delay of the circuit was roughly between 2 and 2.5 μ s, showing very stable characteristics.

The circuit's output impedance is shown in Fig. 10 as a function of common-mode output voltage and load current. The DC output resistance is on the order of hundreds of micro-ohms in Figs. 10(a) and (b), for the case of higher supply voltages. These figures are designed to show how the output impedance remains low throughout the operating range of voltages and loads, even when there is little current being sourced or sunk. In Fig 10(c), the output impedance is increased by approximately an order of magnitude when the supply voltage is dropped to 1.5 V.

V - CONCLUSIONS

A CMOS low voltage, rail-to-rail, class AB amplifier with high output drive and low output impedance was presented. Novel high side and low side output drivers, utilizing source followers in conjunction with common source drivers, were shown to significantly lower the output impedance of the amplifier, while still allowing rail-to-rail operation. The amplifier is fully functional with supplies as low as 1.5 V and optimum operation, with regards to output impedance, is achieved at supply voltages greater than 3.2 V. A typical quiescent current of less than 140 μ A was achieved over the full output current range, with a maximum output current of ± 7 mA with a ± 3 V supply. Low voltage rail-to-rail input/output operation with low quiescent

current flow and high output current make it ideal for battery-powered applications where efficiency is paramount for battery life and extended dynamic range is intrinsic for performance.

REFERENCES

- [1] Soundarapandian Karthikeyan, Siamak Morteza pour, Anilkumar Tamineedi, and Edward K. F. Lee, "Low Voltage Analog Circuit Design Based on Biased Inverting Opamp Configuration", *IEEE Trans. Circuits and Systems II*, vol. 47, pp. 176-184, March 2000.
- [2] Satoshi Sakurai and Mohammed Ismail, "Robust Design of Rail-to-Rail CMOS Operational Amplifiers for a Low Power Supply Voltage", *IEEE J. Solid-State Circuits*, vol. 31, pp. 146-156, Feb. 1996.
- [3] Klaas-Jan de Langen, Johan H. Huijsing, "Compact Low-Voltage Power-Efficient Operational Amplifier Cells for VLSI", *IEEE J. Solid-State Circuits*, vol. 33, pp. 1482-1496, Oct. 1998
- [4] Randall L. Geiger, Phillip E. Allen, Noel R. Strader, *VLSI Design Techniques for Analog and Digital Circuits*, pp. 466-473, McGraw-Hill, 1990.
- [5] Joseph N. Babanezhad, "A Low-Output-Impedance Fully Differential Op Amp with Large Output Swing and Continuous-Time Common-Mode Feedback", *IEEE J. Solid-State Circuits*, vol. 26, pp. 1825-1833, Dec. 1991.
- [6] Jeroen Fonderie, Marinus M. Maris, Erik J. Schnitger, and Johan H. Huijsing, "1-V Operational Amplifiers with Rail-to-Rail Input and Output Ranges", *IEEE J. Solid-State Circuits*, vol. 24, pp. 1551-1559, Dec. 1989.
- [7] J. Francisco Duque-Carrillo, Jose L. Ausin, Guido Torelli, Jose M. Valverde, and Miguel A. Dominguez, "1-V Rail-to-Rail Operational Amplifiers in Standard CMOS Technology", *IEEE J. Solid-State Circuits*, vol. 35, pp. 33-44, Jan. 2000.
- [8] Paul R. Gray and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, 1993.

Table 1. Summary of class AB amplifier performance.

Parameter		Proposed Amplifier	[5]	[3]	Units
Minimum supply voltage		1.5	5	1.8	V
Supply current		140	714	230	μ A
Peak output current		± 7.0	± 4.0	1.2	mA
Input offset voltage		5	-0.5	6	mV
CM input range	max	V_{DD}	$V_{DD}-1.2$	V_{DD}	V
	min	V_{SS}	V_{SS}	V_{SS}	V
Output voltage range ($I_{out} = 0$ mA)	max	V_{DD}	V_{DD}	V_{DD}	V
	min	V_{SS}	V_{SS}	V_{SS}	V
Output voltage range ($I_{out} = \pm 4.0$ mA)	max	$V_{DD} - 0.3$	$V_{DD} - 0.3$	<i>N/A</i>	V
	min	$V_{SS} + 0.3$	$V_{SS} + 0.3$	<i>N/A</i>	V
THD (1 kHz, 1 V, $R_L = 10$ k Ω)		-48	<i>N/A</i>	-41	dB
Unity-gain frequency		300	500	4000	kHz
Phase margin		80	70	67	$^\circ$
Open-loop gain		65	95	86	dB
Slew rate		0.4	0.4	4.5	V/ μ s
Power supply rejection		75	100	<i>N/A</i>	dB
Max capacitive load		100	100	<i>N/A</i>	pF

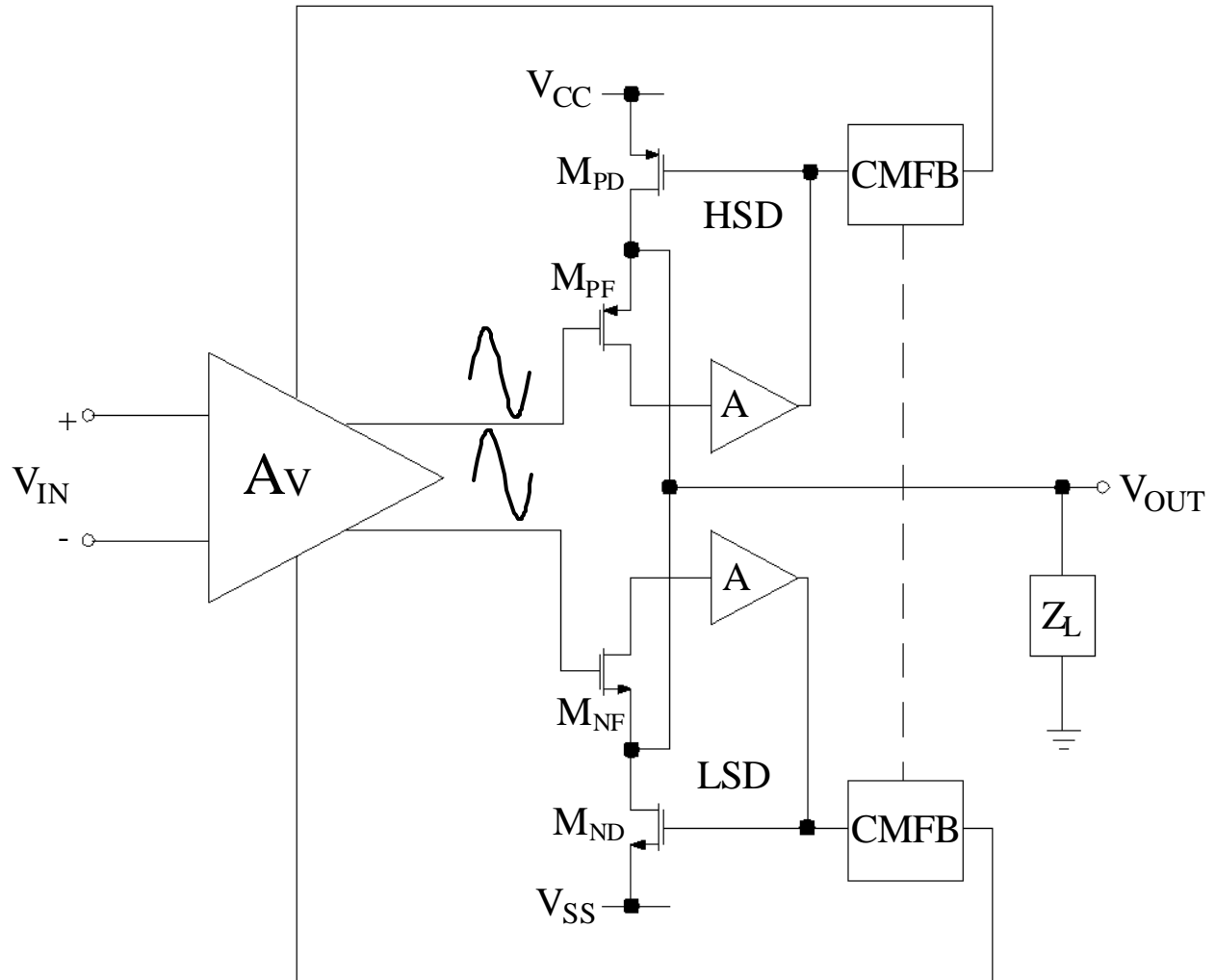


Fig. 1. Circuit topology of the proposed class AB amplifier.

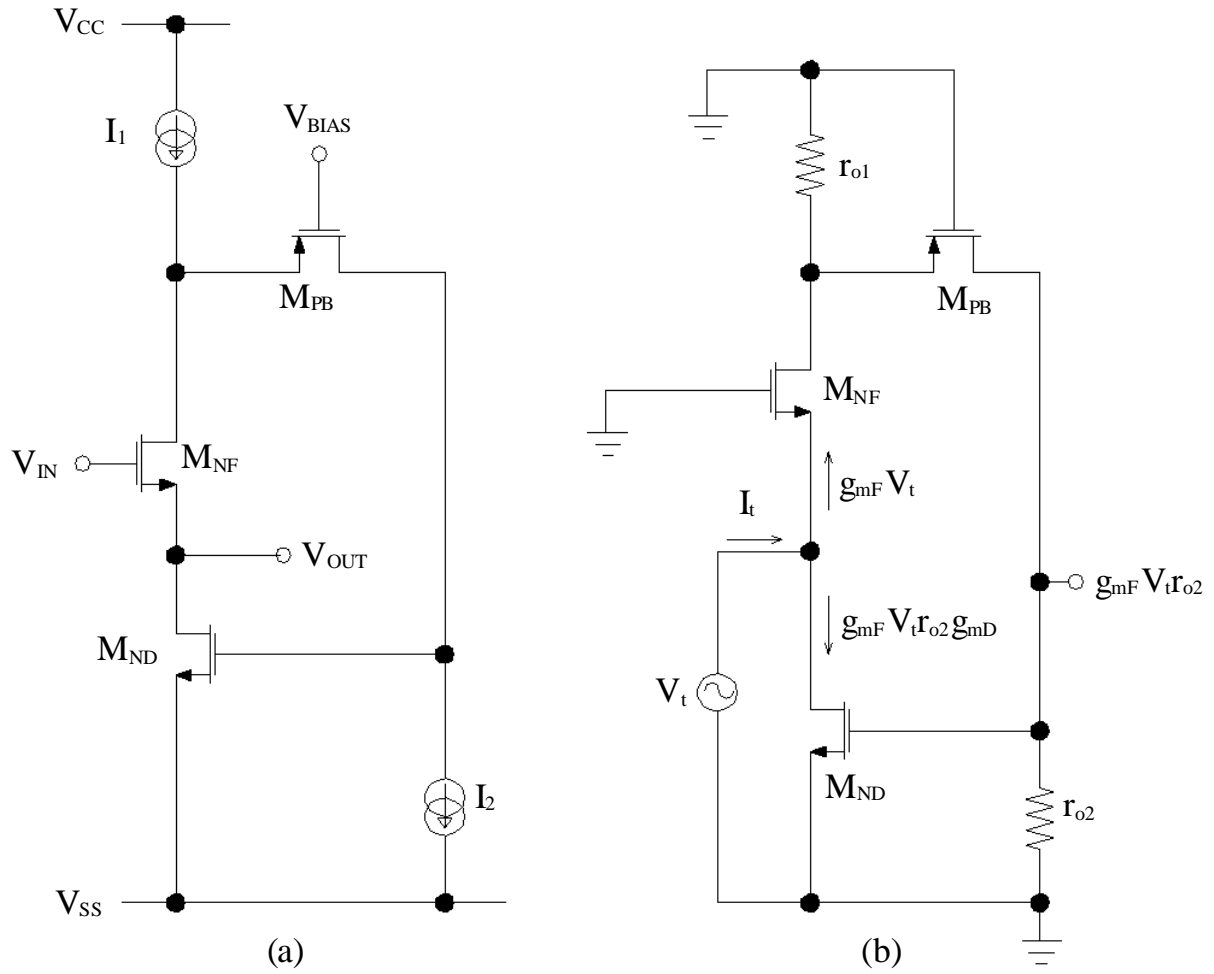


Fig. 2. (a) Simplified circuit diagram of the low side output driver (LSD) and (b) the ac equivalent circuit used to calculate its output impedance.

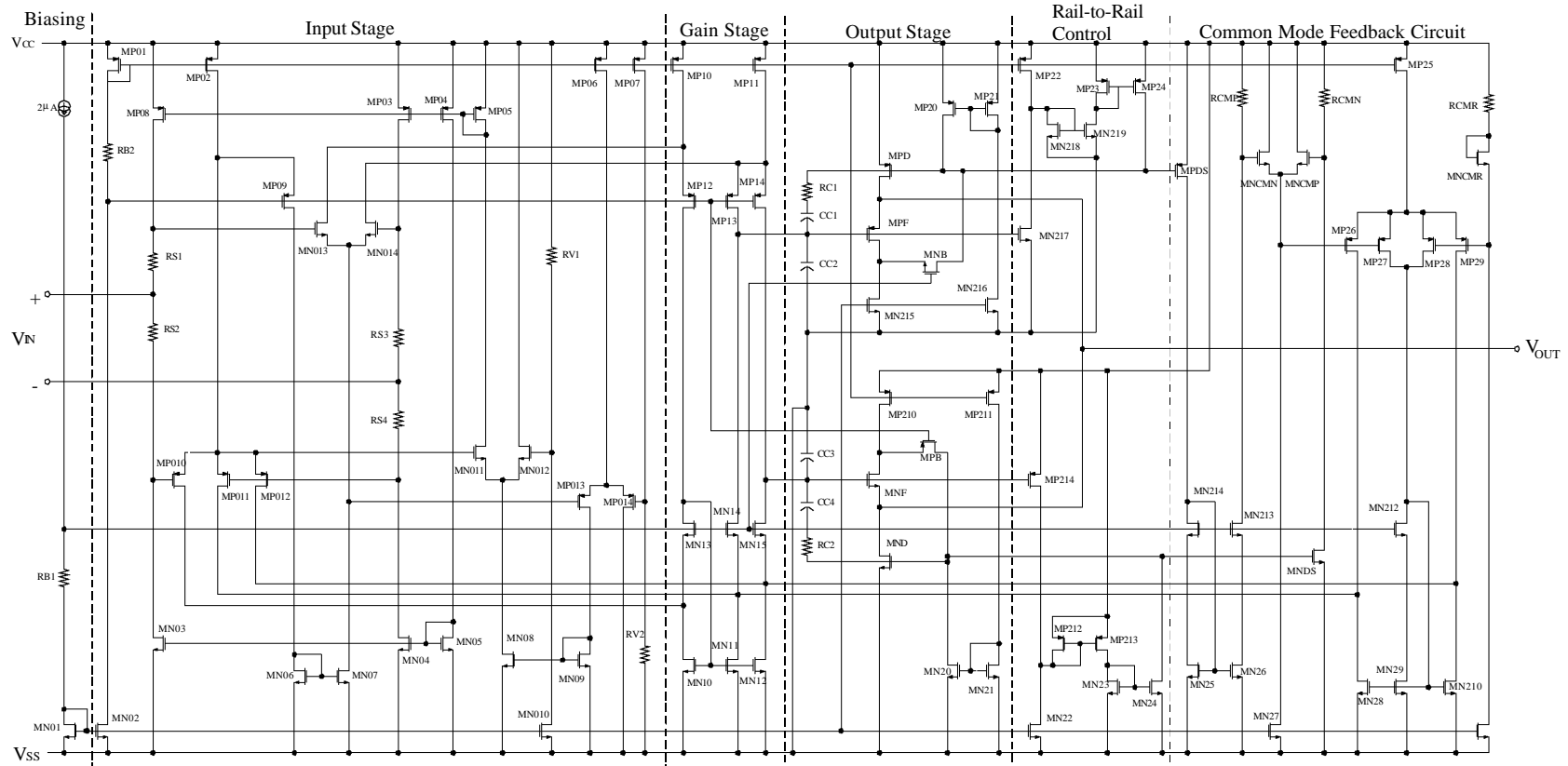


Fig. 3. Complete circuit diagram for the class AB amplifier.

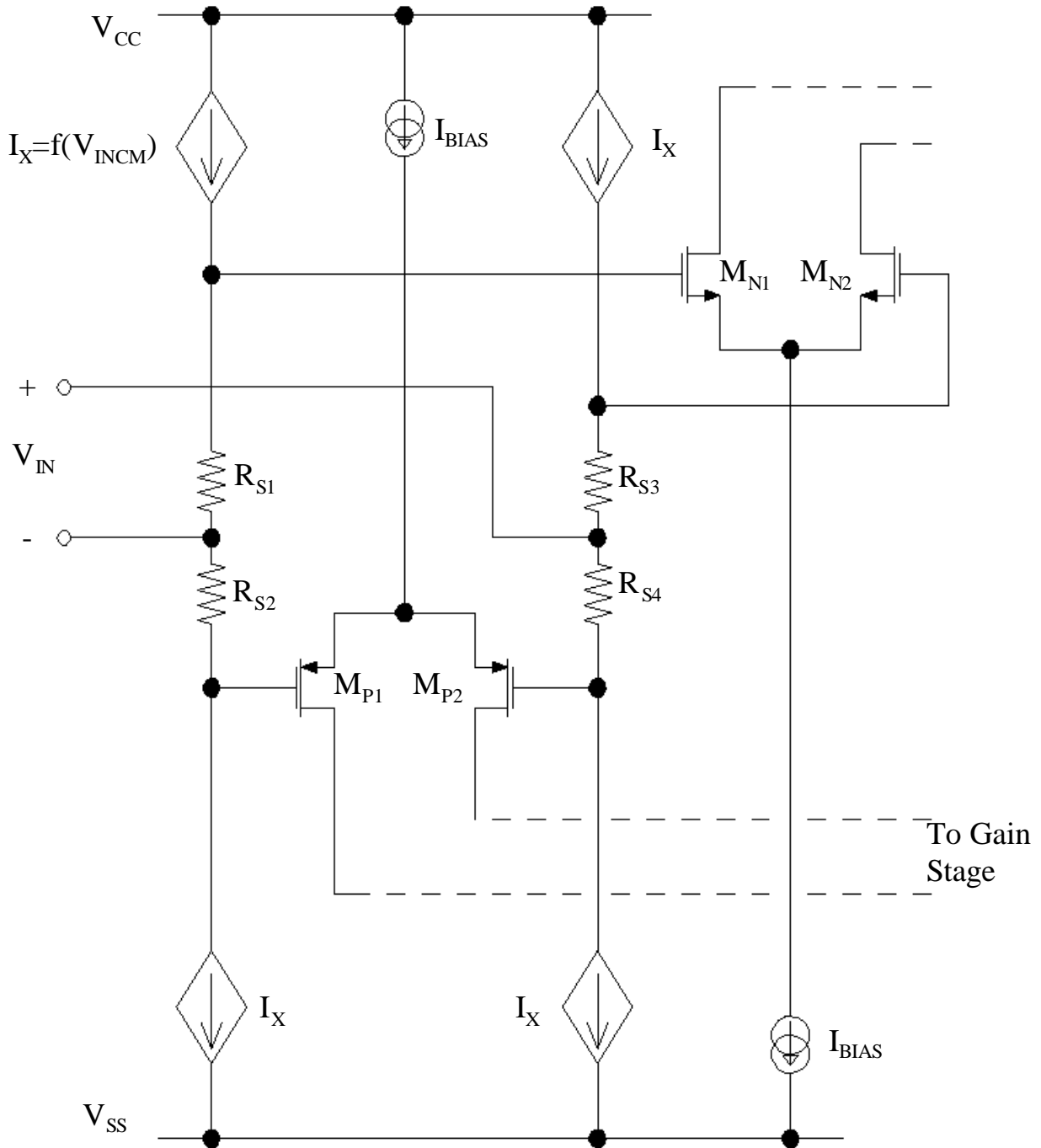


Fig. 4. Simplified schematic diagram of the amplifier input stage.

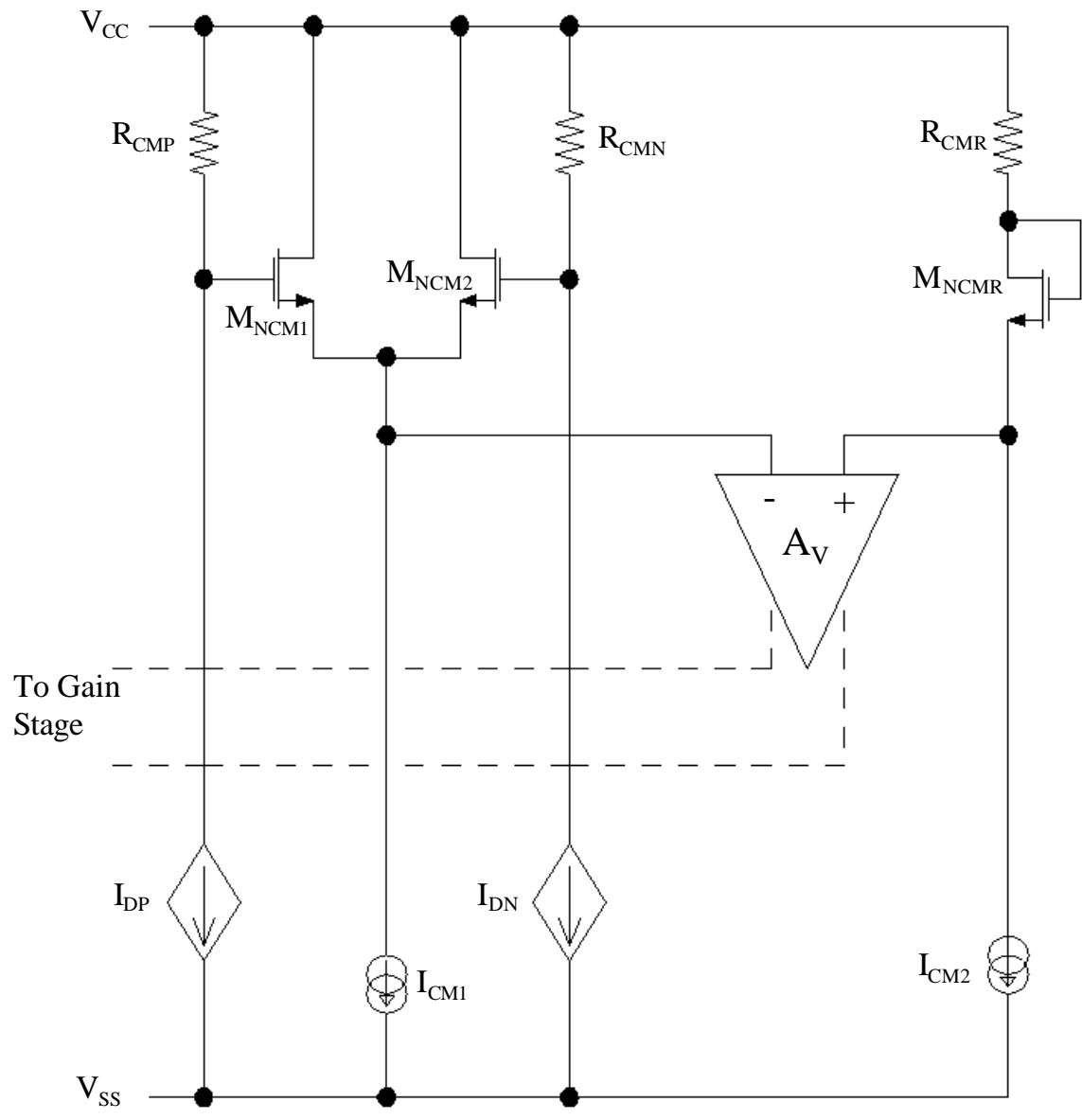
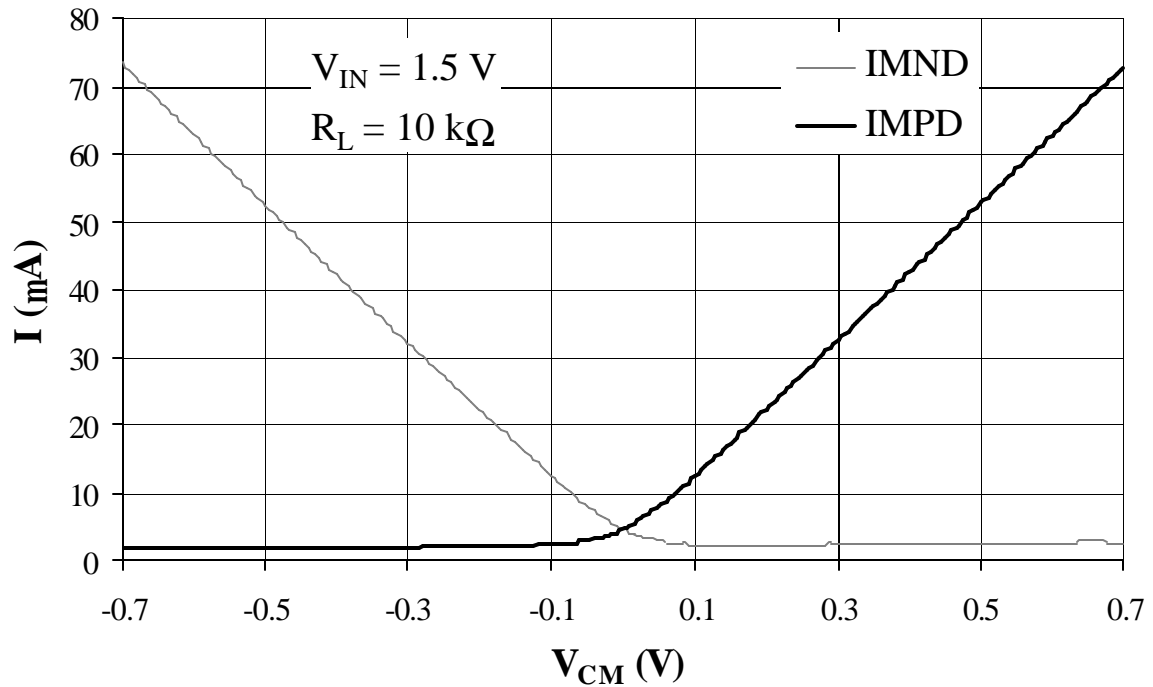
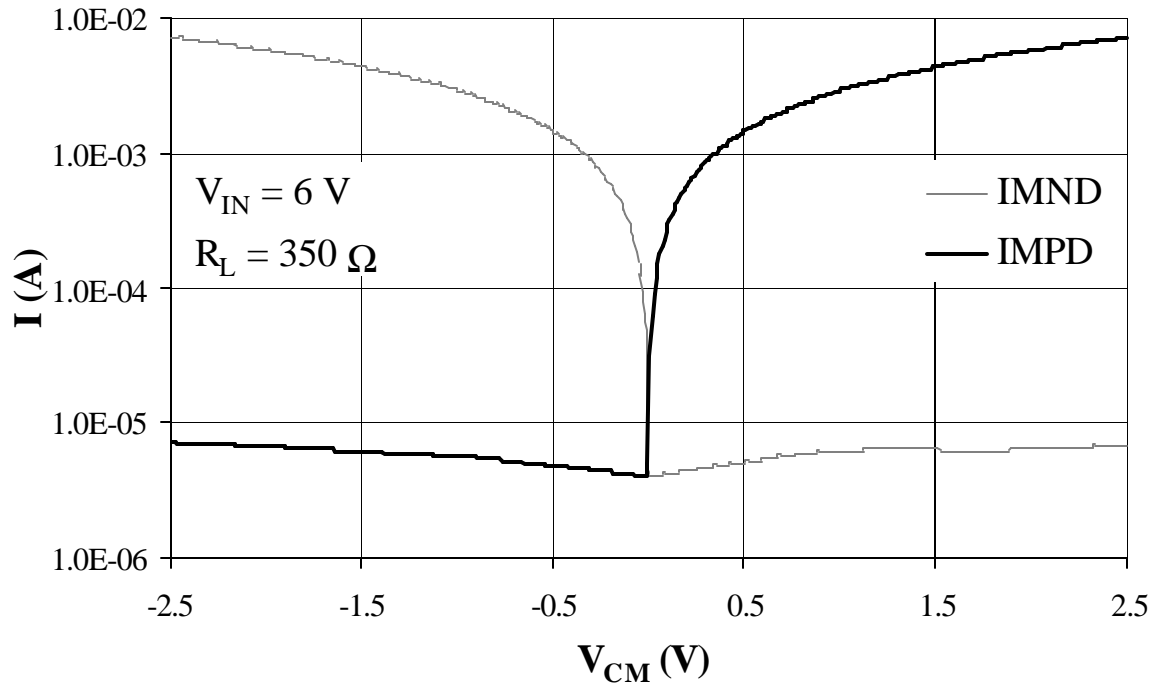


Fig. 5. Simplified schematic diagram of the common-mode feedback circuit.



(a)



(b)

Fig. 6. Class AB output stage driver currents vs. common mode output voltage, (a) $V_{IN} = \pm 0.75$ V and (b) $V_{IN} = \pm 3$ V.

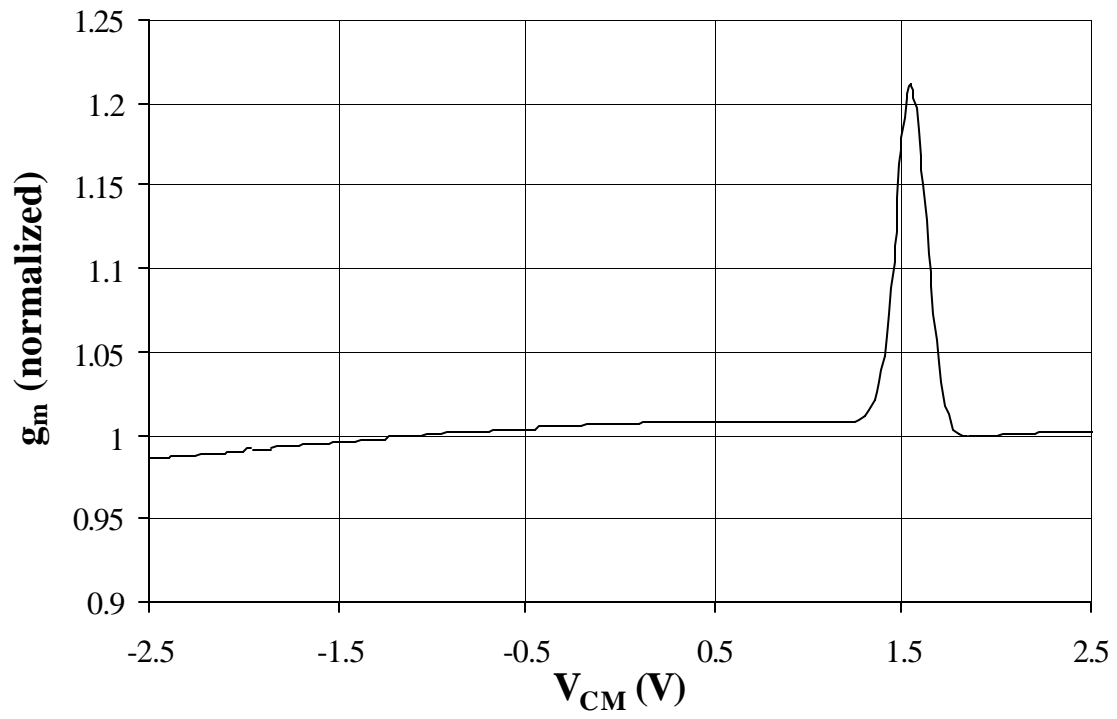
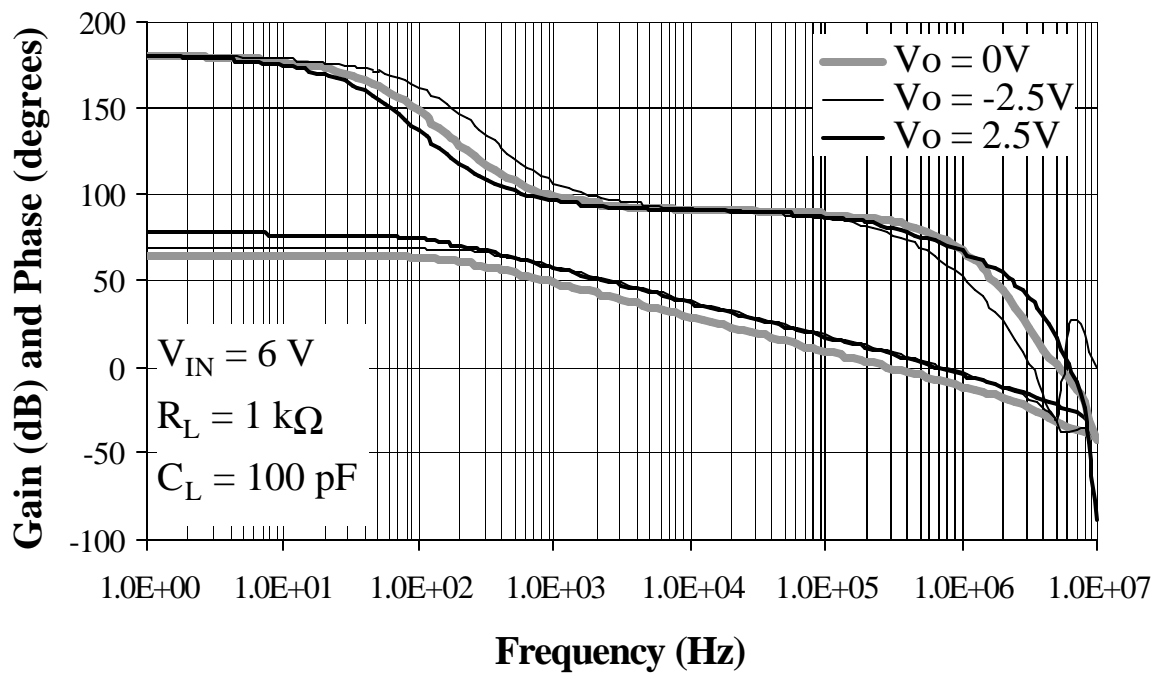
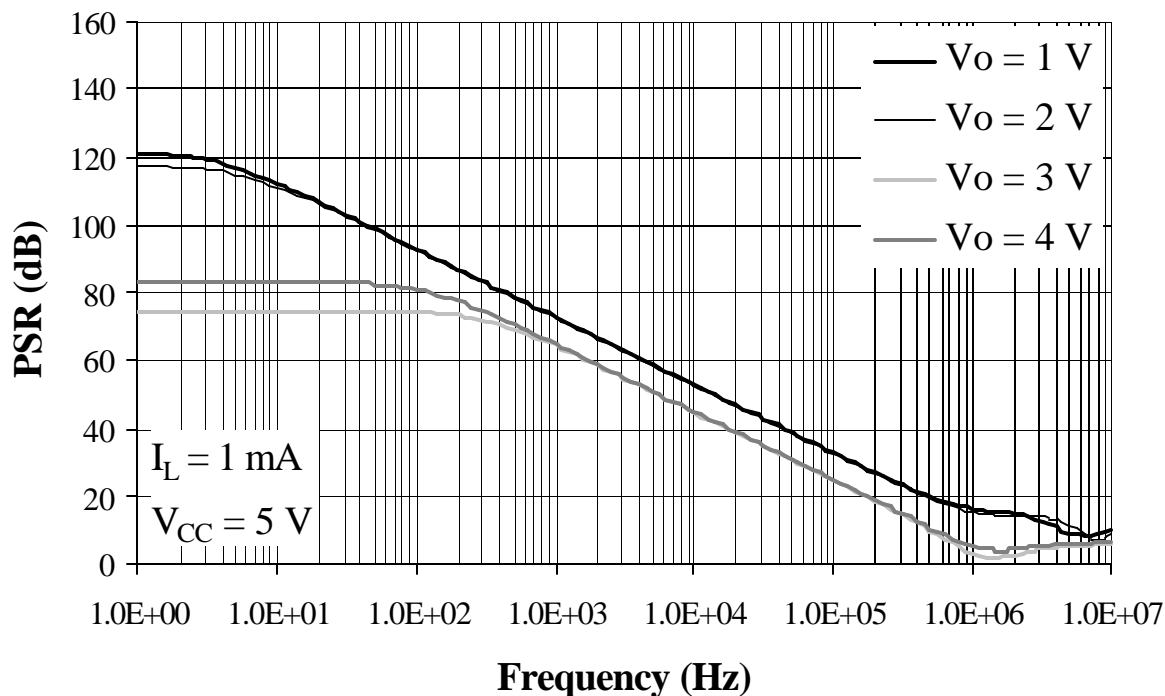


Fig. 7. Input stage transconductance g_m vs. common mode input voltage V_{CM} .

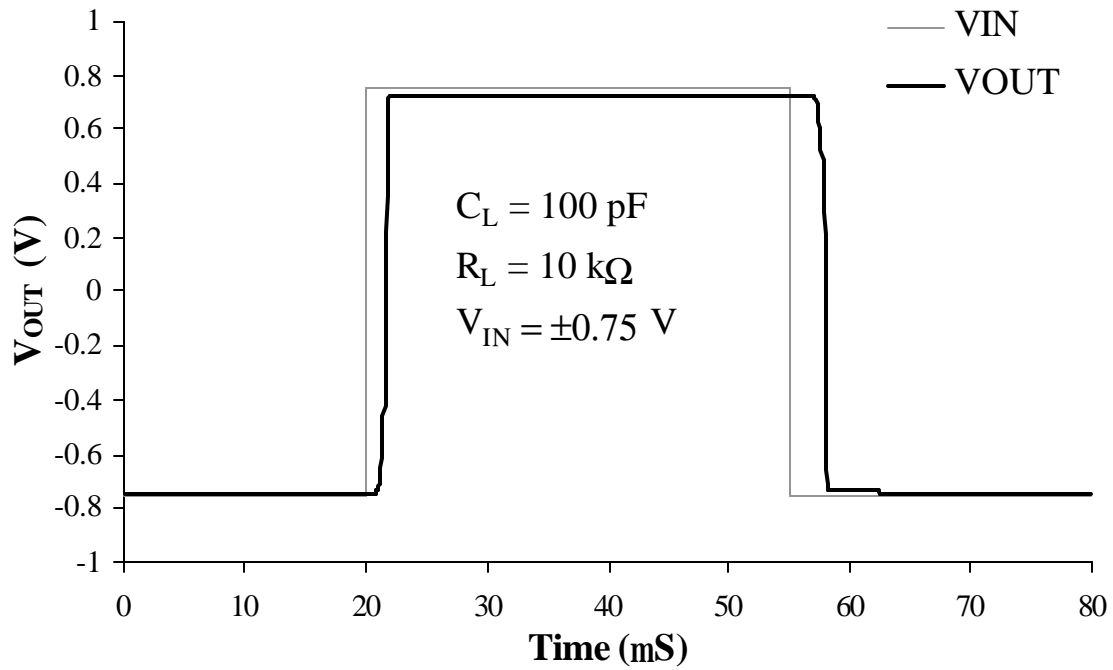


(a)

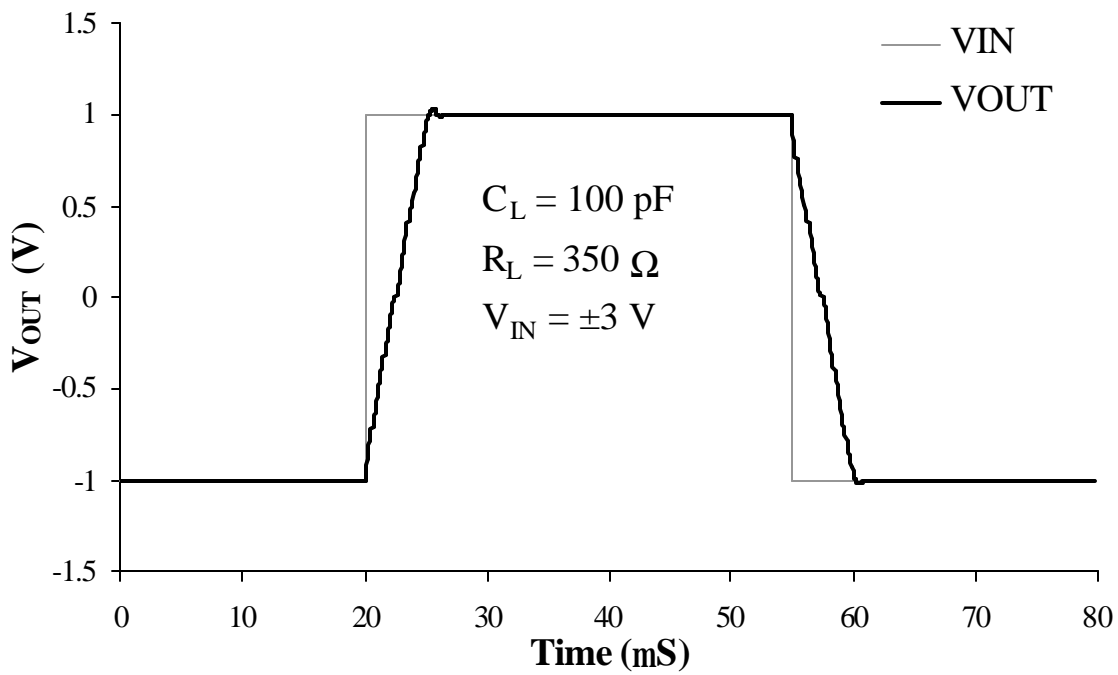


(b)

Fig. 8. (a) AC gain and phase characteristics of the class AB amplifier, and (b) Power supply rejection vs. frequency for several different common mode output voltages.

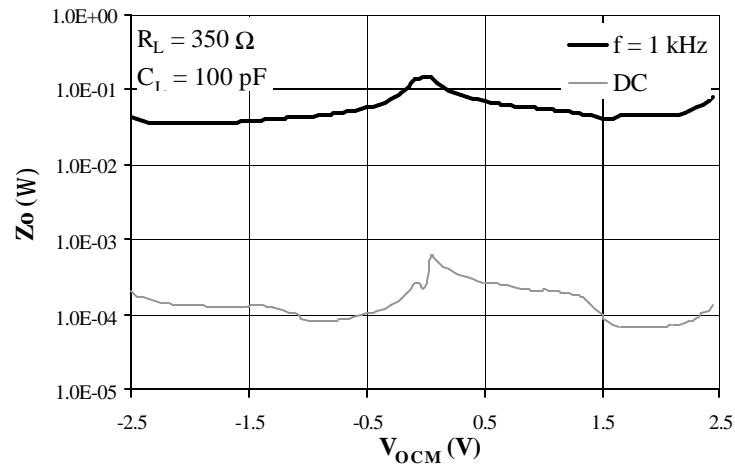


(a)

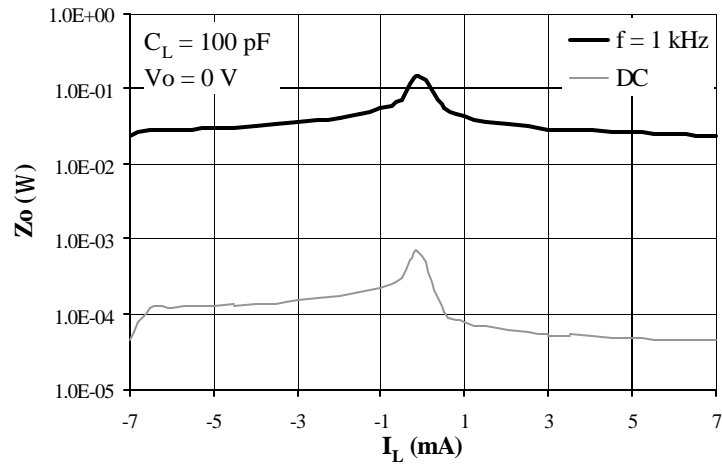


(b)

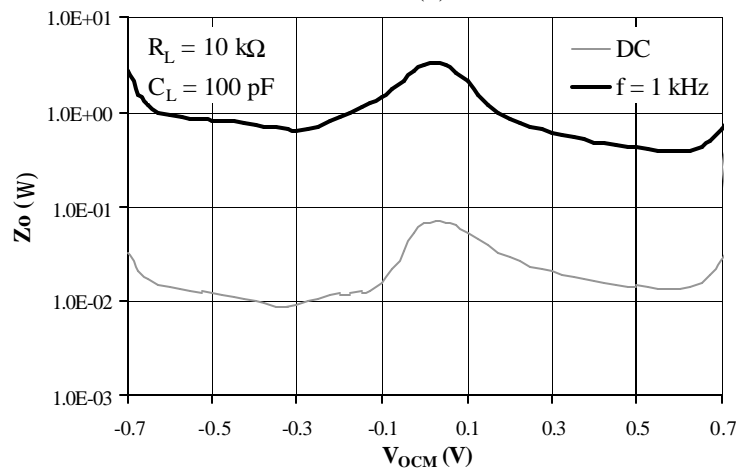
Fig. 9. (a) Unity-gain rail-to-rail step response of the amplifier with minimum supply voltage and (b) step response with maximum supply voltage.



(a)



(b)



(c)

Fig. 10. (a) Amplifier output impedance Z_o vs. common-mode output voltage V_{OCM} for a 350Ω load with ± 3 V supply, (b) output impedance Z_o vs. load current I_L with ± 3 V supply, and (c) output impedance Z_o vs. common mode output voltage V_{OCM} with ± 0.75 V supply.