

An Accurate, Low Voltage, CMOS Switching Power Supply with Adaptive On-Time Pulse-Frequency Modulation (PFM) Control

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Abstract—Integrated switching power supplies with multi-mode control are gaining popularity in state-of-the-art portable applications like cellular phones, personal digital assistants (PDAs), etc. because of their ability to adapt to various loading conditions and therefore achieve high efficiency over a wide load-current range, which is critical for extended battery life. Constant-frequency, pulse-width modulated (PWM) switching converters, for instance, have poor light-load efficiencies because of higher switching losses while pulse-frequency modulation (PFM) control in discontinuous-conduction mode (DCM) is more efficient at light loads because the switching frequency and associated switching losses are scaled down with load current. This paper presents the design and IC prototype results of an 83% power efficient 0.5 V, 50 mA CMOS PFM buck (step-down) dc-dc converter with a novel adaptive on-time scheme that generates a 27 mV output ripple voltage from a 1.4-4.2 V input supply (battery-compatible range). The output ripple voltage variation and steady-state accuracy of the proposed supply was 5 mV (22-27 mV) and 0.6% whereas its constant on-time counterpart was 45 mV (10-55 mV) and 3.6%, respectively. The proposed control scheme provides an accurate power supply while achieving 2-10% higher power efficiency than conventional fixed on-time schemes with little circuit complexity added, which is critical during light-loading conditions, where quiescent current plays a pivotal role in determining efficiency and battery-life performance.

Index Terms— Power supply IC, dc-dc converter, PFM control, adaptive on time

I. INTRODUCTION

THE widespread demand of handheld portable devices with voice, data, imaging, and multimedia all rolled into one requires increasingly efficient power-saving solutions powered from widely variable battery voltages. State-of-the-art power management circuits are therefore used to generate these fixed and dynamic voltage rails in a system from battery supplies (e.g., NiCd and NiMH: 0.9-1.8 V, Li-ion: 2.7-4.2 V) [1]. What is more, fuel-cell technologies, because of their superior energy density [2], are also vigorously pursued in

research for military, space, and possibly consumer electronics. Direct methanol fuel cell (DMFC) systems, for example, exhibit a 0.2-0.7 V terminal voltage variation [3]. All this implies that both currently available and future portable power supplies have a wide variation in input supply voltages, which the power management system must comprehend in its generation of a constant and/or dynamically adaptive output voltage.

Maintaining high efficiency over a wide load range is critical in determining battery life because, on one end, portable devices mostly idle and remain at light loads and, on the other, high performance and high power events have a significant toll on the battery. Unfortunately, when a switching converter designed for high efficiency at a particular peak power level operates in medium-to-light loading conditions, its efficiency and therefore battery life performance degrades. Fixed-frequency, pulse-width modulated (PWM) supplies suffer from this effect because switching losses constitute a major portion of the total power loss when lightly loaded. The key to achieve high efficiency under moderate-to-light loading conditions is to reduce the load independent power losses, most dominant of which are the switching losses [4]. A lower switching frequency in PWM mode reduces switching losses, but results in a higher peak current flowing through the power inductor and power transistors, thereby not only incurring higher conduction losses but also increasing their respective current ratings and die size requirements, that is, increasing cost. Pulse-frequency modulation (PFM) control in discontinuous-conduction mode (DCM) [5] is an attractive alternative for light-to-moderate loads because of lower switching frequencies and therefore reduced switching losses, which is why commercial dc-dc controllers [6]–[8] adopt a combination of PFM and PWM control.

The effective on time of switching converters employing PFM control under DCM conditions is typically set by the inductor's peak current [9]–[11] or fixed (i.e., constant on-time) [12]. In the former, the inductor current is sensed, reconstructed, and controlled with relatively complex and high speed sample and hold analog amplifiers and comparators [9], which often result in additional power losses, silicon real estate requirements, and component count, in other words, higher cost. The high speed requirements of the peak current

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comparator are acute in low duty-cycle conditions, when the input voltage is high and the output is low, because a delay here constitutes a significant fraction of the converter's on time. Although these power losses are often miniscule in moderate-to-high load-current events, they are not so in idle and light loading conditions, the most prevalent and therefore the battery life-determining state of many portable handheld devices. This is why sensing the peak inductor current for over-current protection is often altogether circumvented and simplified by sensing the peak voltage across the synchronous switch, which is not accurate but practical. In constant on-time control, on the other hand, inductor current is neither sensed nor compared, but the cost tradeoff is increased output ripple voltage variations, especially when supplied from a widely variable source. A constant on time under a varying input supply results in a variable peak inductor current, and the subsequent input-to-output energy transferred in one switching cycle also varies [5], producing a widely variable ripple and average output voltages.

This paper proposes a novel technique through which variable energy transfer and output ripple voltage variations are reduced by dynamically adapting the on time of the converter with relatively simple analog electronics, achieving the accuracy performance of peak-current control while retaining the simplicity benefits of constant on-time schemes (i.e., lower silicon real estate) and yielding higher power efficiency (i.e., lower quiescent current flow). The proposed adaptive on-time PFM converter is designed and experimentally validated with a MOSIS 0.5 μm , n-well CMOS prototype IC. To eliminate substrate noise injection, the power switches were integrated separately, on their own IC. The power supply was verified for both functionality and performance over a 1.4-4.2 V input supply voltage range, the lower limit of which was in part limited by the high threshold voltages of the PMOS devices used (0.95 V). Section II of the paper briefly explains the proposed PFM scheme and discusses various system design considerations of adaptive on-time control. In Section III, the key circuit blocks of the controller and their respective designs are discussed. Experimental results of the integrated converter and discussions are then offered in Section IV. Finally, conclusions are drawn in Section V.

II. SYSTEM DESIGN CONSIDERATIONS

A. Basic Converter Operation

The schematic of a synchronous buck converter with PFM control operating in DCM and its key waveforms are shown in Fig. 1. DCM refers to the converter operation where the inductor current remains at zero for part of the switching period, which occurs when the load current is less than half of the peak inductor current [13]. During the on time (T_{PMOS}), transistor MP_1 is on and current in inductor L increases, which decomposes into load and output capacitor charge currents. When MP_1 is turned off, during which time the stored inductor energy is transferred to the output capacitor, the

inductor current is initially freewheeled to zero via the body diode of transistor MN_1 (D_1), then through synchronous

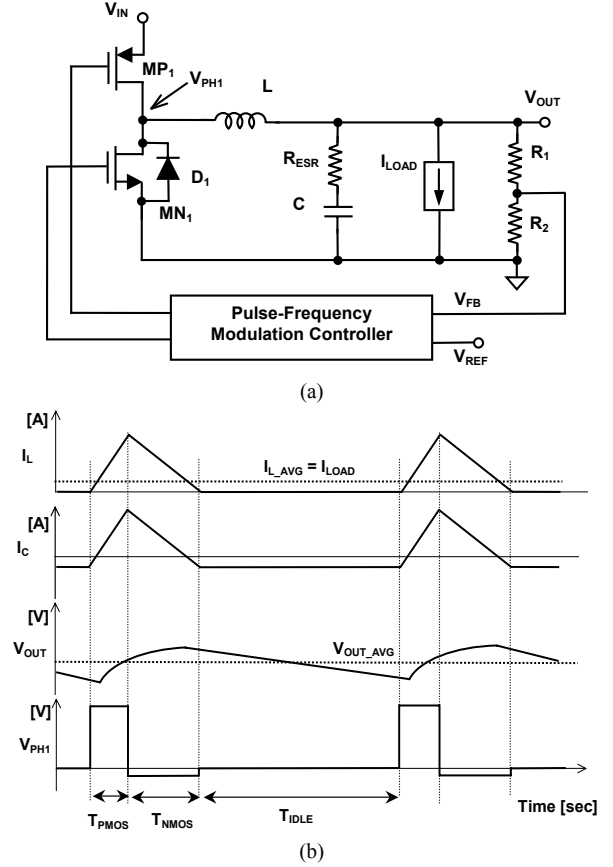


Fig. 1. (a) Schematic of a synchronous buck converter with PFM control and (b) its key waveforms.

switch MN_1 . During T_{IDLE} , both switches remain off and the output capacitor sources the necessary load current.

The total charge stored in the inductor is the area under the inductor current waveform in one switching interval, which is given by

$$Q_L = \frac{1}{2} \frac{T_{\text{PMOS}}^2 (V_{\text{IN}} - V_{\text{OUT}}) V_{\text{IN}}}{V_{\text{OUT}} L}. \quad (1)$$

Ignoring the power losses in the converter to obtain a first-order approximation and assuming the circuit is properly regulating the output, the total charge stored in the inductor is equal to the charge delivered to the load, and given by

$$Q_L = I_{\text{OUT}} T, \quad (2)$$

where T is the sum of switching intervals T_{PMOS} , T_{NMOS} , and T_{IDLE} during PFM operation in DCM. Since the energy demanded by the load is less than the energy stored in the inductor during on time, which is necessary to compensate for the energy loss during the off time, the worst-case output voltage ripple (ΔV) is estimated by assuming the total charge in the inductor is delivered to output capacitor C ,

$$\Delta V = \frac{Q_L}{C}. \quad (3)$$

Consequently, with the power inductor and output capacitor chosen and designed according to PWM control in

continuous-conduction mode (CCM), the peak inductor current value and consequently the on time of pass transistor MP_1 is defined to ensure the output ripple voltage remains within acceptable accuracy limits, as needed by the application.

B. Adaptive On-Time Control

If the on-time is optimally designed for the high end of the input supply range (e.g., 4.2 V), the peak inductor current and therefore energy in the inductor are lower when the converter operates at the low end of the input supply range (e.g., 1.4 V) because the rising rate of the current is linearly proportional to the input voltage. As a result, the converter needs to switch faster to remain in regulation, thereby increasing switching losses and defeating the power-saving advantages of PFM in DCM operation. On the other hand, an on time that is designed for the lower supply voltage range produces higher peak currents and consequently higher output ripple voltages, when operated at the highest input supply voltage. PMOS transistor MP_1 's on time T_{PMOS} (Fig. 1) in PFM control should be a function of input and output voltage V_{IN} and V_{OUT} and peak inductor current I_{L_PEAK} :

$$T_{PMOS} = \frac{I_{L_PEAK}}{V_{IN} - V_{OUT}} L, \quad (4)$$

where for a given input and output voltage, inductor L , capacitor C , and output ripple ΔV combination, peak inductor current I_{L_PEAK} is

$$I_{L_PEAK} = \sqrt{\frac{2C\Delta V}{L} \left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \right) V_{OUT}}. \quad (5)$$

As noted earlier, fixed on-time control under a wide range of input supply voltages produces a variable inductor current, which in turn yields a variable output ripple voltage. To overcome this and maintain a low output ripple voltage, the converter's on-time should be dynamically adjusted when the supply voltage is changed, that is,

$$T_{ON}(T_{PMOS}) = \sqrt{\frac{2LC\Delta V V_{OUT}}{V_{IN}(V_{IN} - V_{OUT})}}. \quad (6)$$

Fig. 2 illustrates the block-level schematic and relevant timing diagram of the proposed adaptive on-time PFM scheme. In essence, variable current source I_{VAR} that is dependant on the input supply and output voltage is used to charge a capacitor from its zero reset state to a pre-determined threshold voltage (a gate-source voltage in this case: V_{CONST}). The time required to reach the threshold voltage (i.e., converter's on time: T_{CHARGE}) is therefore linearly proportional to supply-dependant current source I_{VAR} ,

$$T_{CHARGE} = \frac{V_{CONST} C}{I_{VAR}} = \frac{V_{CONST} RC}{V_{IN} - V_{OUT}}, \quad (7)$$

where R is used to set the magnitude of the current.

To maintain a constant peak inductor current, irrespective of the supply voltage, the required on time of the converter must be equal to the charge time of the capacitor, which is given by

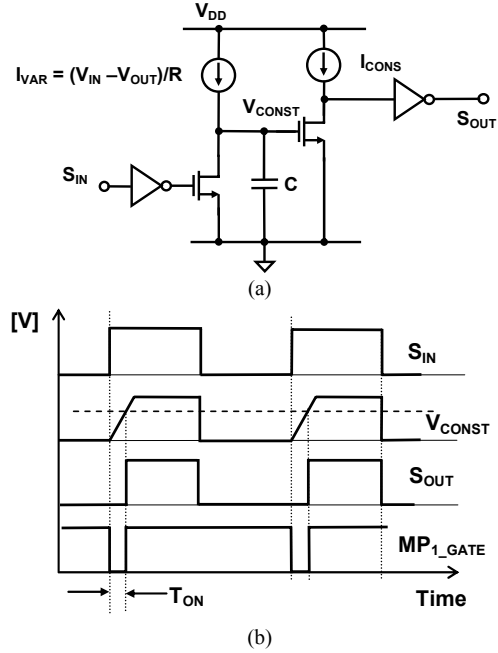


Fig. 2. Block-level schematic and (b) corresponding timing diagram of the adaptive on time generation circuit.

$$T_{ON} = \frac{L I_{L_PEAK}}{V_{IN} - V_{OUT}} = \frac{V_{CONST} RC}{V_{IN} - V_{OUT}}. \quad (8)$$

Therefore, suitable values of V_{CONST} , R , and C define the desired supply-dependant on time, whereby a higher supply voltage causes the circuit to set a shorter converter on time.

C. Asynchronous Versus Synchronous Switching

In PFM control, hopping between asynchronous and synchronous operation could lead to further improvements in efficiency, especially for extreme light loading conditions, where quiescent current has significant impact on converter efficiency and battery life, and knowing where one mode outperforms the other is advantageous. While the inductor current rises at the same rate in both asynchronous and synchronous DCM switching (Fig. 3), it falls faster with asynchronous switching because the additional voltage drop across the free-wheeling diode increases its rate. As a result, the net energy charge transfer from the input supply to the output is lower in asynchronous operation, which is why the asynchronous converter switches more often than the synchronous counterpart, to compensate for the power lost in

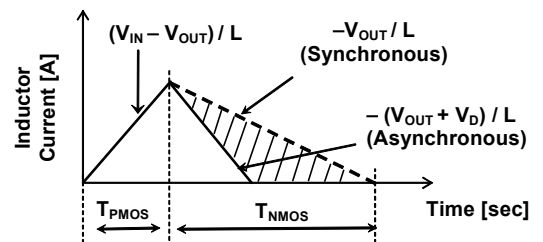


Fig. 3. Inductor current waveform of one switching cycle with asynchronous and synchronous operation in PFM control.

the diode that would have otherwise been delivered to the load, resulting in even more power losses and lower overall power efficiency. To prevent negative current-flow losses in synchronous switching, however, requires additional circuitry to sense the onset of a negative current-flow condition, and this circuitry also incurs additional power losses. Consequently, for a given load current, if the power losses in the free-wheeling diode exceed those of the detection circuit, synchronous operation is warranted; otherwise, the detection circuit can be disabled and its associated power losses avoided.

To quantify this, the charge lost in diode Q_{BD} during one burst of energy transfer is illustrated by the shaded area of Fig. 3, which is equal to the difference in the energy stored in the inductor when switched synchronously and asynchronously,

$$Q_{BD} = \frac{1}{2} \frac{T_{PMOS}^2 (V_{IN} - V_{OUT})}{V_{OUT} L} \left(1 - \frac{1 + \frac{V_D}{V_{IN}}}{1 + \frac{V_D}{V_{OUT}}} \right). \quad (9)$$

The overhead of synchronous switching is the total charge required by the negative inductor current sensing circuitry, which is the product of its quiescent current I_{Q_NCS} and PFM switching period T_S ,

$$Q_{NCS} = I_{Q_NCS} T_S. \quad (10)$$

As a result, the limiting criterion for determining whether asynchronous or synchronous operation is best depends on the switching frequency and the quiescent current of the sensing circuit, the former of which is a function of load current.

D. Adaptive On-Time PFM Controller with Synchronous Switching

Fig. 4 shows the detailed schematic of the PFM controller with the proposed adaptive on-time scheme. The circuit essentially regulates the low peak of the output ripple and sets the high peak when the clock sends a resetting signal. In other words, when feedback sense voltage V_{FB} , which is derived from the output voltage via a feedback resistor divider, decreases below reference voltage V_{REF} (i.e., low peak is regulated against V_{REF}), comparator $COMP_1$'s output transitions from low to high. This event triggers the state of SR latch's complementary output Q_b to transition from high to

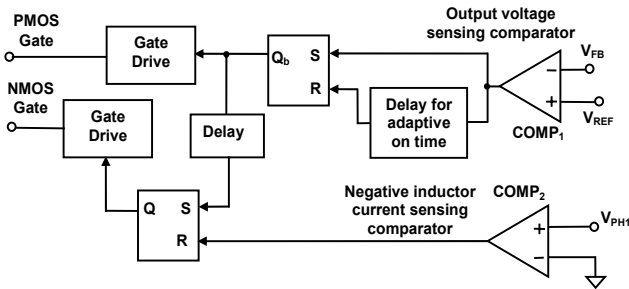


Fig. 4. Adaptive on-time, pulse-frequency modulated (PFM) controller circuit.

low and consequently turn on power PMOS transistor MP_1 (Fig. 1(a)), which causes the output ripple to rise. When a clock-derived resetting signal is engaged, the SR latch is reset and MP_1 's gate-drive signal is therefore raised to the input supply, ultimately turning the device off (and turning MN_1 on) and causing the output voltage to decrease again.

To avoid “shoot-through” current from the input power supply to ground and therefore minimize power losses in the converter, an intentional time delay (i.e., dead time) is introduced between the turn-off event of the buck-stage PMOS pass switch (MP_1) and the turn-on transition of the synchronous NMOS device (MN_1). After MP_1 turns off, after a delay, the output of the second latch goes high, turning MN_1 on and forcing the inductor ripple current to decrease. This current eventually decreases below zero, pushing current back into the circuit, unnecessarily wasting power and discharging output capacitor C , which is why negative current-flow detect comparator $COMP_2$ is inserted, to sense this condition and turn off synchronous switch MN_1 (i.e., operate in asynchronous mode).

Node V_{PHI} is the junction of power transistors MP_1 and MN_1 and inductor L , and its voltage is set by the state of MP_1 and MN_1 and their respective on resistances. As long as the inductor ripple current, which flows through MN_1 when it is decreasing, is positive, V_{PHI} is below ground. However, when the current decreases below zero (i.e., reverses direction), the voltage drop reverses polarity and V_{PHI} becomes higher than ground potential, which is the sensing condition used in Fig. 4 (comparator $COMP_2$ engages with above-ground V_{PHI} voltages) to turn off MN_1 and save the negative current losses alluded to earlier. Once MN_1 is off, since MP_1 is already off and the current in the inductor is exhausted (zero), inductor L and the series combination of output capacitor C and the parasitic capacitance of node V_{PHI} to ground “ring” and tend to converge to the steady-state voltage across capacitor C , until again MP_1 conducts and pulls it high, as later shown in Fig. 9(a), which conforms to typical asynchronous converters’ waveforms. As a side note, ringing in higher power systems causes electro-magnetic interference (EMI), which is not always an issue at low power levels, which is the target application of PFM converters.

Offsets in the comparator (and falsely tripping the comparator) affect the overall efficiency performance of the converter. For instance, if there is a negative offset in the comparator, that is, its threshold is slightly lower than ground, MN_1 may be turned off prematurely, before exhausting the inductor current. Current would therefore be forced to flow through MN_1 's body diode, increasing conduction losses during that time by a factor of V_{DIODE}/V_{DS_ON} (e.g., $0.7\text{ V} / 0.2\text{ V}$). Positive offsets, on the other hand, allow the current to momentarily reverse direction, not entirely avoiding the negative current-flow power losses targeted with this circuit. In practice, the delay across the comparator and drivers constitute a systematic negative offset, which tends to be more power efficient than a positive offset. The delay and effects of falsely tripping the comparator therefore have an impact on

efficiency; however, since the ringing effect of V_{PH1} converges back to its dc value and an intentional hysteresis is added to the sensing comparator, false trip events rarely occur.

III. INTEGRATED CIRCUIT DESIGN

The foregoing PFM mode converter was designed, built, and evaluated within the context of a dynamically adaptive radio-frequency (RF) power amplifier (PA) supply for portable wireless applications. When the PA transmits low power to the antenna, the supply circuit operates in PFM mode, biasing the PA with a supply voltage of 500 mV and supplying relatively low quiescent currents, up to 50 mA. The maximum peak-to-peak supply ripple voltage allowed in this state is 30 mV. The output filter of the converter, which was set by the high load-current requirements of the converter, when operated in pulse-width modulated (PWM) mode, is comprised of a 1 μ H - 20 μ F power inductor and output capacitor combination [14-15].

A. Adaptive On-Time Generation Circuit

The core of the foregoing adaptive on-time scheme is the adaptive on-time signal generator. For low silicon real estate and low power requirements (i.e., low cost and extended battery life), the circuit must be relatively simple (i.e., low component count) and draw minimal quiescent current from the supply, as it will remain active even when the system is in stand-by mode. The basic function of this circuit is to generate the on-time pulse of the converter's pass switch in response to a below-the-reference voltage drop at the output whose width is linearly dependent on supply voltage V_{IN} , not necessarily proportional to $V_{IN} - V_{OUT}$, as V_{OUT} has little variations. Consequently, seeing that the gate-source voltage of an NMOS device (0.7 V) is on the order of the output voltage of the converter (0.5 V), although not exactly equal to it, generating a current that is inversely proportional to $V_{IN} - V_{GS}$ is sufficient to realize the function desired, which is what is implemented in Fig. 5 by impressing $V_{IN} - V_{GS_MN1}$ across R_{BIAS} and using that current (mirrored via MN_2 , MP_1 , and

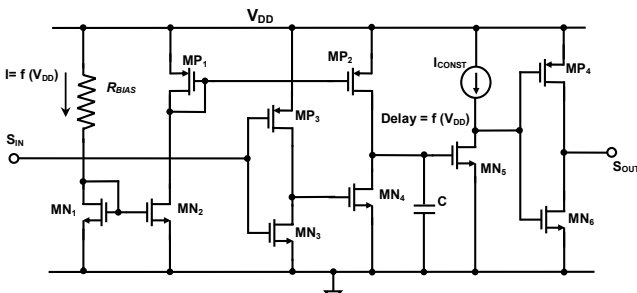


Fig. 5. Adaptive on-time circuit for the proposed PFM controller.

MP_2) to charge capacitor C, and together with $V_{T_MN5} + V_{DSsat_MN5}$, the threshold of the MN_5 class A inverter, set the pulse width and on time of the circuit. As a result, a higher supply voltage produces a larger charge current and therefore a lower charge time, that is, lower on time.

Process and temperature variations will also affect the on

time of the circuit. The root-square sum of the random process-induced variations of R_{BIAS} ($\pm 20\%$), V_{T_NMOS} (± 50 -100 mV), k'_{NMOS} ($\pm 20\%$), C ($\pm 20\%$), $MP_{1,2}$ mirror offset ($\pm 5\%$), and I_{CONST} ($\pm 20\%$) ultimately define the worst-case on-time variation, most of which can be compensated by trimming R_{BIAS} . Temperature variations will also have an adverse effect on tolerance, but this can be mitigated by introducing a temperature coefficient (TC) to I_{CONST} that cancels the systematic tendencies of the circuit or by using a resistor whose TC performance opposes that of V_{GS_NMOS} . For this particular design, however, R_{BIAS} was trimmed and no temperature compensation was performed. Fig. 6 illustrates the simulated and measured on-time performance of the circuit under various supply voltages, where the measured response corresponds to the trimmed R_{BIAS} case and the worst-case corner simulations to resistance and capacitance tolerances of $\pm 20\%$. The measured on-time was slightly longer than its target by 40-200 ns, but its total per cent variation was similar,

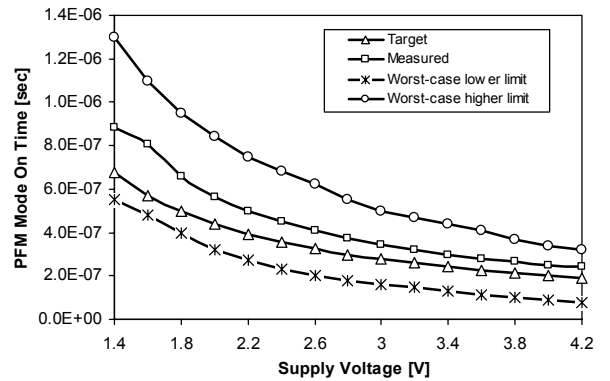


Fig. 6. Simulated and measured on-time performance of the adaptive on-time circuit under various supply voltages, where the measured response corresponds to the resistor-trimmed circuit and simulations to resistor and capacitor tolerances of $\pm 20\%$.

on the order of 50%. The effects of deviating from its targeted variation ultimately affects the overall power efficiency of the converter, by not sufficiently minimizing inductor ripple current variations, but the deviation measured was not significant enough to warrant alarm.

B. Comparator Circuit Design

Both feedback comparator $COMP_1$ and negative inductor current sense comparator $COMP_2$ are designed for an input common-mode range (ICMR) of -50 to 150 mV, to accommodate their combined requirements. The feedback resistor divider gain ratio for $COMP_1$ is set to five (closed-loop gain of the converter) so that its reference is 100 mV (0.5/5 V), around which an ICMR range of 50-150 mV is required. $COMP_2$ senses zero-Volt crossings (V_{PH1}) and its ICMR range limits are therefore set about ground, -50 to 50 mV - a 2-5 mV hysteresis window is added to the comparator to prevent transient glitches when V_{PH1} is in the vicinity of ground. The comparator's dc gain and maximum propagation delay are specified to be greater than 60 dB to resolve 1 mV changes and less than 100 ns with 10 mV overdrive input signals, on one hand, to accurately regulate the feedback loop

with $COMP_1$, and on the other, to prevent the inductor current from reaching large negative values with $COMP_2$, which would otherwise degrade the converter's PFM power efficiency performance. The maximum input-offset voltage specified for the comparators is 10 mV, and this is to limit its impact on the converter's output ripple voltage and overall accuracy performance.

To design for the above ICMR, a PMOS differential input stage was selected. For the lower ICMR of -50 mV, the folded-mirror load configuration shown in Fig. 7(a) can be used; however, since the PMOS devices in the 0.5 μm n-well CMOS process technology used for this design have higher threshold voltages than the NMOS transistors, a simple current-mirror load was used by connecting the input PMOS pairs' bulk to the input power supply. Therefore, the effective threshold voltages of the input pair devices increase under bulk-bias conditions, consequently yielding a lower ICMR limit of less than -50 mV,

$$ICMR_{LOW} = V_{TN} + V_{DS_DSAT} - |V_{TP}|, \quad (11)$$

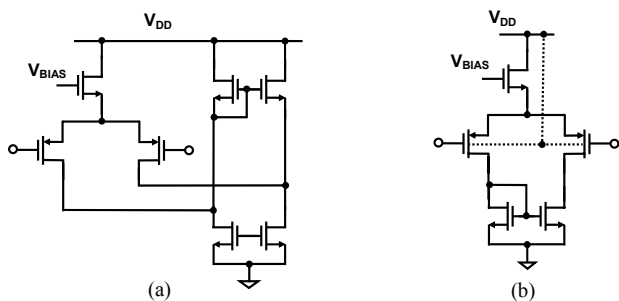


Fig. 7. (a) Folded and (b) non-folded PMOS input differential stage with bulk terminals tied to the supply to extend ICMR limits with bulk-bias effects.

with a nominal value of V_{TN} of 0.75 V and $|V_{TP}|$ of 0.95 V. The use of the folded-mirror architecture is avoided because of its inherently higher quiescent current flow requirements (i.e., higher power dissipation), circuit complexity, and transistor-matching requirements, which are critical for input-offset voltage performance.

C. Power Switches and Other Circuit Blocks

The device dimensions for the power transistors used were selected to achieve high efficiency at higher load currents, when operated in PWM mode, and under low input supply voltages, in other words, low gate-drive conditions (1.4 V). The bias currents and voltages for all the various analog building blocks are generated and derived from on-chip proportional-to-absolute temperature (PTAT) current generator and bandgap reference circuits. Although ultimately necessary for a practical solution, the design details of these circuits bring little value to the foregoing PFM scheme and are therefore excluded in this presentation, but available in [15].

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The fully integrated power supply circuit (i.e., controller with power switches in the same die) was functional for load

currents up to 100 mA at lower input supply voltages. However, as the supply voltage increased, the injected substrate noise from the NMOS power transistor introduced spurious noise to the reference voltage that propagated onto the output of the converter, causing instabilities and unreliable operation, in spite of using triple shallow n+ and p+ and deeper n-well guard-rings to laterally isolate the power switches from the controller and sensitive analog circuits. Process technologies that are more suitable for integrated power switching supply circuits have deep n+ trenches and buried n+ layers that can more effectively isolate the power switches and shunt the noise they generate before they ever reach sensitive analog electronics. A power NMOS transistor, for instance, can be entirely housed within its own isolated p region by extending a deep n+ buried layer to a surrounding deep n+ trench or n-well diffusion “donut” structure. Unfortunately, the n+ buried layer was not available in the process used (0.5 μm CMOS process available through MOSIS), and unlike non-epi wafers, the substrate of the epi-wafer technology used is a noise-conductive medium with a

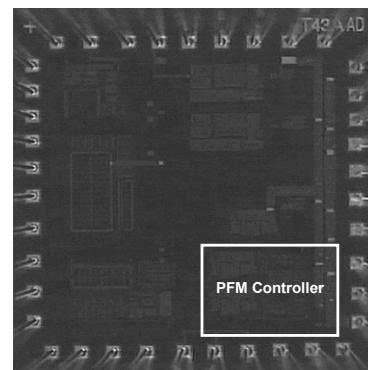
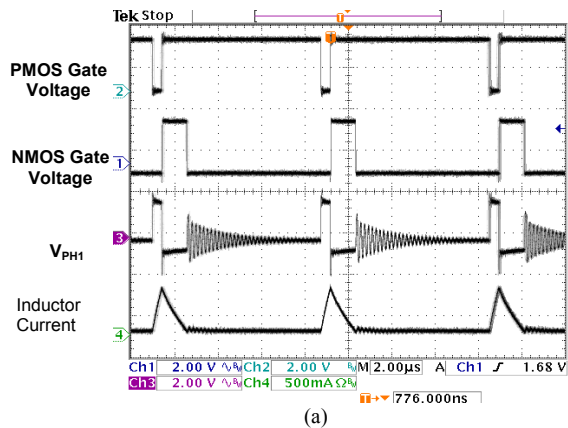


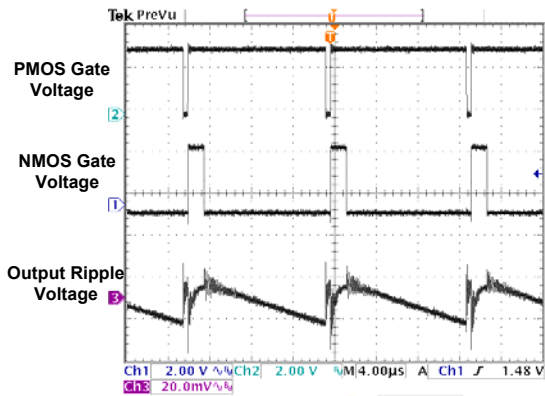
Fig. 8. Die photo of the controller IC.

sheet resistance of 5 Ω/\square . Because of these reasons, and because the objective was to test the proposed PFM scheme, the switching power supply was tested using separate controller and power transistors ICs, just as conventional controllers are normally tested. Fig. 8 illustrates the die photograph of the prototype controller IC.

The experimental power supply with the PFM controller IC in DCM was fully functional, as shown by the experimental gate-drive, switching node, inductor current, and output ripple voltage waveforms presented in Fig. 9. The 0.5 V output was derived from a 3.2 V input supply voltage, producing a 22-27 mV peak-to-peak ripple voltage. The peak-to-peak output ripple voltage variation resulting from input supply changes was 5 mV, whereas its fixed on-time counterpart was 45 mV (10-55 mV), as shown in Fig. 10, which was one of the driving features of the design. As discussed earlier, the peak inductor current and therefore the output ripple voltage of the fixed on-time scheme increase with supply voltage. As a side note, the on-time of the proposed prototype circuit varied from 230 to 850 ns while the fixed on-time circuit was kept at 530 ns. Higher output ripple voltages under PFM control necessarily increase the average output voltage of the



(a)



(b)

Fig. 9. Experimental (a) gate-drive, switching node, inductor current, and (b) output ripple voltage waveforms of the proposed PFM converter in DCM.

converter because its control is fixed and based on the lower limit of the ripple. As a result, a higher ripple variation, as is the case with the fixed on-time scheme when compared with the foregoing adaptive circuit, results in degraded output accuracy – the accuracy of the proposed prototype was 0.6% whereas its fixed on-time counterpart was 3.6%, as shown in Fig. 11.

Since the peak inductor current and consequently the charge and energy per cycle delivered to the output capacitor of fixed on-time control schemes increase with increasing supply voltages, the output capacitor takes more time to discharge to its lower threshold limit, the result of which is a lower switching frequency, as shown in Fig. 12. The energy transferred to the output capacitor in the adaptive scheme, on the other hand, remains relatively fixed, resulting in a low variation of the switching frequency across the entire input voltage range. However, since the PFM circuit was actually applied to a buck-boost converter circuit [14-15], which has a transmission-gate switch in series with the power inductor, the conductance of the additional switch has an adverse impact on efficiency and frequency. When the input supply voltage decreases below 1.5 V with an output voltage set at 0.5 V, for instance, the series PMOS switch shuts off and the gate-drive of the complementary NMOS transistor is low, barely above its threshold, forcing the body diode of the PMOS device to

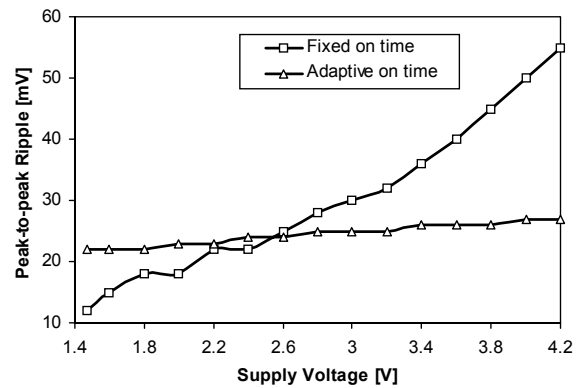


Fig. 10. Experimental peak-to-peak output ripple voltage for fixed and the proposed adaptive on-time prototype.

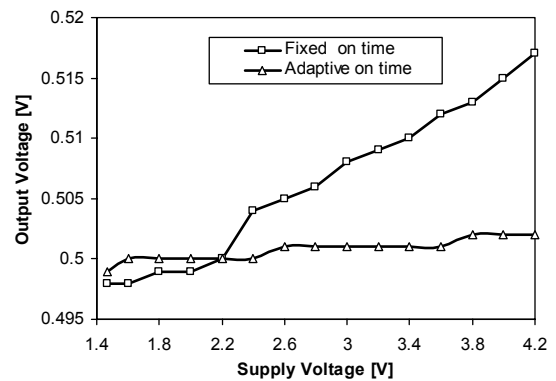


Fig. 11. Experimental average output voltage of the PFM converter for fixed and adaptive on-time control.

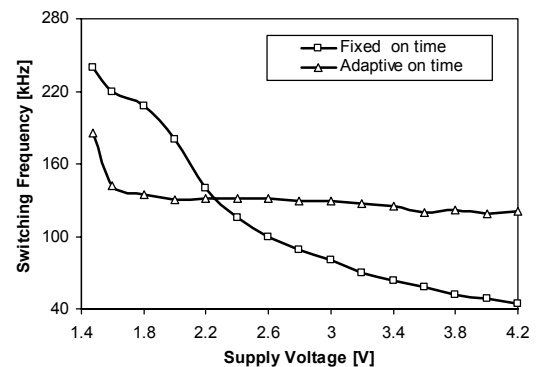


Fig. 12. Measured switching frequency of the converter under fixed and adaptive on-time control.

conduct all the inductor current. The resulting voltage across the switch (i.e., a diode voltage) incurs additional power losses and forces the circuit to compensate for the additional loss of energy, which would have otherwise been transferred to the load, by switching more often (i.e., higher switching frequency).

The power efficiency performance of the adaptive on-time scheme in DCM is 2-10% higher than its fixed on-time counterpart, as shown in Fig. 13. This improvement results because the fixed on-time circuit has larger inductor ripple

currents at higher supply voltages (i.e., higher conduction losses) and higher switching frequencies at lower supply voltages (i.e., higher switching losses). Generally, with respect to itself, the power efficiency of the proposed on-time scheme decreases at higher supply voltages because the gates of the power transistors and relevant gate-drive circuits charge and discharge to and from higher voltages, thereby incurring higher switching losses. However, when gate-drive losses

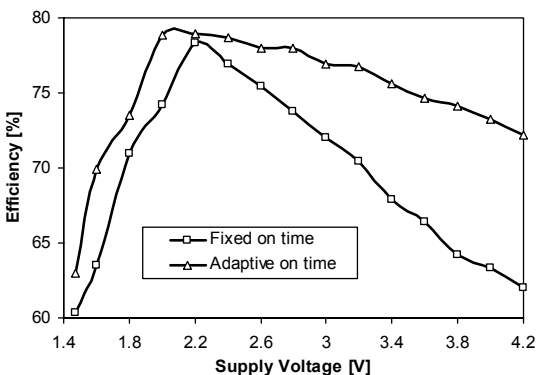


Fig. 13. Measured efficiency performance of the PFM converter under fixed and adaptive on-time control with a 50 mA load.

become smaller than conduction losses, which increase because the switch-on resistances of the buck switches (and series boost transmission gate devices) increase as the supply voltage is decreased, the trend reverses, as shown in Fig. 4. Additionally, as the input supply voltage is reduced further, the body diode of the series boost PMOS transistor conducts and further degrades efficiency performance.

With respect to increasing load currents, because more energy per unit time is demanded by the load, the switching frequency increases under heavier load-current conditions, to offset the energy per cycle deficit, which ultimately results in higher switching and conduction losses (Figure 14), as

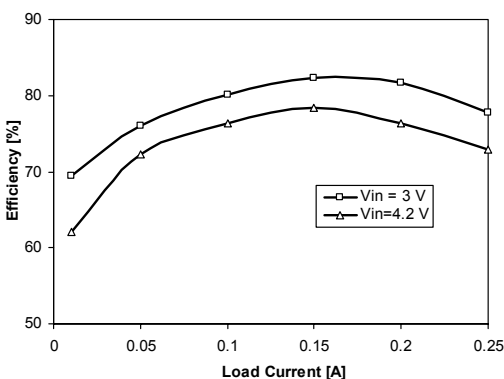


Fig. 14. Measured power efficiency performance of the proposed PFM converter with respect to load current at two input supply voltages.

expected in PFM mode. This increase in frequency also causes the output ripple voltage to decrease because the charge per cycle delivered to the output capacitor is lower. Under extreme light loading conditions, however, quiescent current and switching power losses overwhelm any remaining conduction losses. As before (Fig. 13), higher input supply

voltages incur higher switching losses.

Fig. 15 illustrates the measured load-dump response of the foregoing PFM mode converter, that is, its response to transient load-current changes. As the load is increased from 50 to 300 mA, the average output voltage drops approximately 15 mV from its nominal output voltage of 500 mV, which amounts to its load-regulation performance. The ability of the circuit to settle and converge to its steady-state value after a

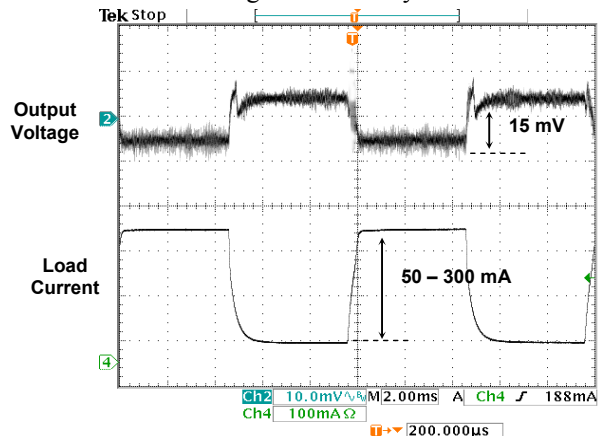


Fig. 15. Experimental transient load-step response of the adaptive on-time PFM converter.

transient load step illustrates the robustness and stability of the circuit's feedback loop. In the application for which this converter was designed, the worst-case negative load-dump step, when entering PFM mode, is 400 μ s, and as shown in the Fig., the circuit responds to this load variation with a settling time that is commensurate with better than 45° of phase margin performance.

The experimental results of the PFM converter are compared with the targeted design values and full-chip simulation results in Table I. The simulated and measured peak-to-peak output ripple voltages and its steady-state values were consistent. Larger on-time variations across the supply voltage range and random input-referred offsets in the feedback comparator account for the slight discrepancies. The measured efficiency was in part lower than simulated because of the conduction power losses associated with the parasitic resistances not present in the simulations, such as those introduced by the traces of the printed-circuit-board, bond wires, and on-chip interconnects. The models of the power switches were also inaccurate, especially as it pertains to parasitic source, gate, and drain resistances and gate-source, gate-drain, and gate-bulk capacitances, all of which are strongly dependent on their layout and resulting three-dimensional physical structure. Underestimating these parasitic devices led to lower conduction and switching power losses and more optimistic simulation results. Correlation between simulation and experimental efficiency results can be improved by extracting the parasitic components of the power devices from an existing layout, but ultimately characterization and custom modeling of already built power devices are needed for accurate results.

The minimum input supply voltage of the fabricated converter was bounded to 1.4 V by the threshold voltage of

the PMOS device and two drain-source saturation voltages. Had it not been for the unusually high threshold voltage of the PMOS transistor, which was 0.95 V, the minimum supply boundary could have been lower. The fact is that many process technologies today offer PMOS devices with threshold voltages of 0.5-0.6 V, which when applied to the

TABLE I
SUMMARY OF THE SIMULATED AND EXPERIMENTAL RESULTS OF THE PFM CONVERTER.

Specification	Unit	Target	Sim.	Exp.
$V_N = 1.4\text{ V}$				
Output voltage	V	0.5	0.508	0.499
Peak-to-peak ripple	mV	≤ 30	20	22
Efficiency (50 mA)	%	≥ 65	69	63
$V_N = 3.0\text{ V}$				
Output voltage	V	0.5	0.508	0.501
Peak-to-peak ripple	mV	≤ 30	22	25
Efficiency (50 mA)	%	≥ 80	83.56	76
$V_N = 4.2\text{ V}$				
Output voltage	V	0.5	0.508	0.502
Peak-to-peak ripple	mV	≤ 30	25	27
Efficiency (50 mA)	%	≥ 80	81.52	72.255

foregoing circuit, lead to minimum input supply limits closer to 1 V. Nevertheless, combining the accuracy performance of adaptive on-time schemes (e.g., low peak-to-peak output ripple voltages and low steady-state output voltage variations) with the simplicity of fixed on-time converters while concurrently improving power efficiency is appealing in its own right.

V. CONCLUSION

A novel adaptive on-time pulse-frequency modulation (PFM) control scheme for buck dc-dc converters is proposed, designed, built, and experimentally validated with an IC prototype from MOSIS' 0.5 μm n-well CMOS process technology. The key features of the design are accuracy performance (on par with conventional peak-current control schemes), simplicity (on par with fixed on-time topologies), and improved power efficiency performance. The prototyped 0.5 V, 50 mA PFM supply circuit exhibited a peak-to-peak output ripple voltage variation of 5 mV (22-27 mV) over an input supply voltage range of 1.4-4.2 V and a steady-state accuracy of 0.6%, whereas its fixed on-time counterpart varied by 45 mV (10-55 mV) and achieved an accuracy of 3.6%, respectively. The proposed IC achieved a peak efficiency of 83%, 2-10% higher efficiency than its fixed on-time counterpart across the entire input supply range. These accuracy and light load efficiency performance enhancements are especially appealing in the ever expanding mobile, hand-held, battery-powered market, where performance is not easily achieved, yet often sacrificed for light load efficiency, that is, for battery life, given the high propensity for portable devices to idle.

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