# Voltage Shift in Plastic-Packaged Bandgap References

Buddhika Abesingha, Gabriel A. Rincón-Mora, and David Briggs

***Abstract*—Bandgap references, packaged in plastic, have been known to shift in voltage, a pre-package to post-package voltage variation. This *package shift* has been analytically discussed and experimentally investigated in this paper. The culprits for such a variation are the package-induced stresses present once the reference is encapsulated. Systematic voltage shifts can range from −3 to −7 mV, and is closely related to package type and processing. Major emphasis has been placed on reducing the random package-shift component, since systematic package shift can be trimmed and its temperature coefficient compensated. The package shift is seen to have a systematic positive temperature coefficient; its effects are mitigated as temperature increases. In summary, results of the study show that die-surface planarization techniques and mechanically elastic compliant layers between the die and the package reduce random as well as systematic package shifts. In particular, systematic variations improved from −5 to −2 mV (0.4% to 0.17% bandgap error) and three-sigma (3$\sigma$) variations improved from 8 to 4 mV (0.67% to 0.33% bandgap error) when adding a 15-$\mu$m mechanically compliant layer between the die and the package.**

***Index Terms*—<AUTHOR: PLEASE SUPPLY YOUR OWN KEYWORDS OR SEND A BLANK E-MAIL TO KEYWORDS@IEEE.ORG TO RECEIVE A LIST OF SUGGESTED KEYWORDS>.**

## I. Introduction

Bandgap references like the Brokaw cell in Fig. 1 are used in a wide variety of integrated systems where accurate and precise voltage references with excellent line regulation and temperature-drift performance are required [1]. Since bandgap references play a pivotal role in determining the accuracy of integrated systems, designers employ different types of trimming techniques and algorithms to compensate for process variations, temperature, and complex second-order and third-order effects [2]. However, bandgap references encapsulated in plastic packages exhibit a characteristic shift in voltage. Once it is packaged in plastic, the bandgap reference's output voltage differs from its original, nonpackaged value. This *package shift,* unfortunately, is not completely consistent from unit to unit, even if the same encapsulant and packaging technique is used. This randomness is detrimental since designers cannot easily account for this variant in the design phase.

This paper reports the investigation of post-package shift in bandgap voltage references, with a discussion of the causes of stress in plastic packages (Section II), effects of such stress on bandgap references (Section III), techniques used to minimize package shifts (Section IV), experimental results (Section V), and finally, drawn conclusions (Section VI).

## II. Stress in Plastic Packages

The main cause for internal stresses in plastic packages, which are relatively inexpensive, compact, and moisture resistant and therefore more popular than the ceramic counterparts, is the difference in coefficient of thermal expansion of the plastic mold and the silicon die. Most of the plastic molding is done at a temperature of 175 °C to lower the viscosity of the plastic mold. The plastic, which has a typical coefficient of thermal expansion greater than ten times that of silicon, transmits an ever-increasing stress to the chip as the package cools from molding to ambient temperature [3]–[5].

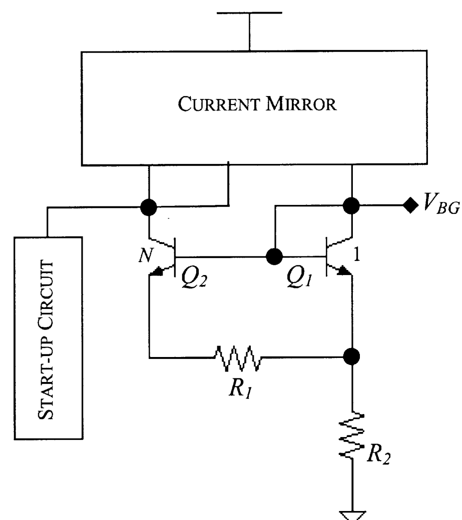


Fig. 1. First-order Brokaw-type bandgap reference.

This differences in thermal expansion coefficients between the plastic and the die results in normal compressive stresses and shear stresses on the die. For most plastic packages, the normal compressive stresses in the $x$ direction ($s_{\rm xx}$) and the $y$ direction ($s_{\rm yy}$) are about an order of magnitude larger than the normal stress in the vertical $z$ direction ($s_{\rm zz}$). This characteristic difference results because the lateral dimensions of the plastic mold are significantly larger than the thin vertical plastic layer on top. Vertical $s_{\rm zz}$, of course, increases with thicker layers of plastic mold. The shear-stress tensor $\langle \tau_{\rm xy}, \tau_{\rm yz}, \tau_{\rm xz} \rangle$ for $x$–$y$, $y$–$z$, and $x$–$z$ planes, respectively, is also about an order of magnitude smaller than normal compressive stresses $s_{\rm xx}$ and $s_{\rm yy}$. Strain gauges placed on chips to identify package stresses have shown that surface compressive stresses $s_{\rm xx}$ and $s_{\rm yy}$ are highest at the center of the die, while $s_{\rm zz}$ is highest at the corners and the edges of the die. All three normal stresses, however, are uniform toward the center of the die while showing large gradients toward the edges and, especially, the corners of the die. All three shear stress components, $\tau_{\rm xy}$, $\tau_{\rm yz}$, and $\tau_{\rm xz}$, are highest at the corners and the edges of the die and lowest toward the center of the die. The shear components show large gradients but they tend to be minimal at the center of the die [6]–[8].

One of the main vertical compressive stress-related failure mechanisms reported in the literature is the filler-induced mechanism [9]. The plastic mold consists of silica fillers that vary in size and shape, as shown in Fig. 2(a). The fillers are used, among other reasons, to reduce the thermal coefficient expansion of the package to prevent destructive effects like corner and passivation layer cracking as well as metal-line shifts. Depending on the size, shape, and orientation of these fillers, they exert intense stress fields on localized regions of the die.

## III. Effects of Mechanical Stress on Bandgap References

Compressive stresses, and the resulting strain, can change several physical characteristics of semiconductors. The most significant of these changes are variations in the energy band structure of the semiconductor, which is manifested by increases in minority carrier concentrations.

Manuscript received March 9, 2001; revised October 17, 2002. This paper was recommended by Associate Editor W. Serdijn.

The authors are with the Georgia Tech Analog Consortium, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA (e-mail: Rincon-mora@ece.gatech.edu).

Digital Object Identifier 10.1109/TCSII.2002.806734

1057-7130/02$17.00 © 2002 IEEE

IEEE Proof

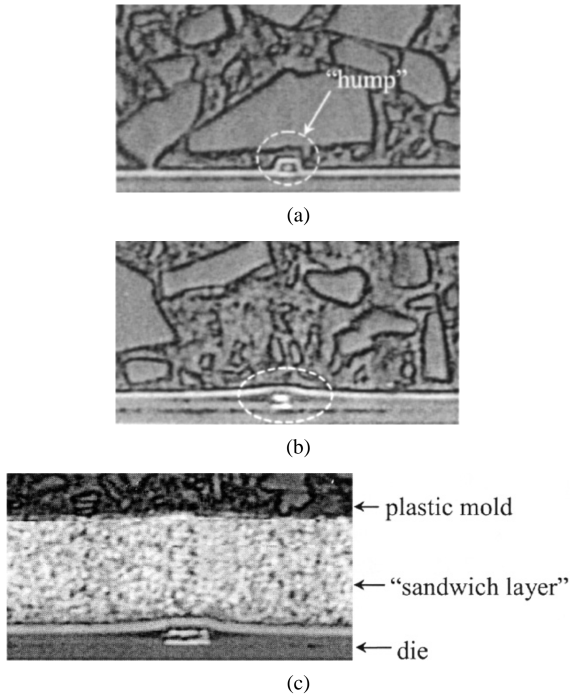


Fig. 2. Cross-sectional images of (a) nonplanarized, (b) planarized, and (c) mechanically compliant layer ("sandwich layer") dies.

### A. Stress Effects in BJTs

Quantum-mechanical studies have shown that changes in the energy band structure results in a decrease in the bandgap energy of semiconductors, like silicon and germanium, and a corresponding increase in minority carrier concentration [10]. Furthermore, these increases in minority carrier concentration depend on the crystalline direction (e.g., [100], [111], or [011]) in which the stress is applied; although, this effect is minimal in silicon. The reverse saturation current $I_s$ of an $n$–$p$–$n$ BJT is proportional to the minority carriers in the base. Therefore, $I_s$ under mechanical stress can be written as

$$I_s \approx I_{\rm so}\gamma(\varepsilon) \tag{1}$$

where $I_{\rm so}$ is the reverse saturation current of the BJT in the unstressed state, $\gamma(\varepsilon)$ is the ratio of base minority carriers under stress to that of minority carriers without stress, and $\varepsilon$ is the magnitude of stress. Compared to increases in minority carrier concentration, stress-related changes in the electron mobility are assumed to be negligible on $I_s$ as [10] points out. Mechanical stress, consequently, tends to cause BJT devices to become stronger, increases its $I_s$.

### B. Stress Effects on Bandgap References

If the BJTs, as well as the resistors in the Brokaw bandgap cell, in Fig. 1 are matched properly (discussed further in Section IV) and the resistors, particularly $R_1$, have negligible stress effects (e.g., polysilicon resistors [11]), then it can be shown that the change in bandgap voltage, $\Delta V_{\rm BG}$, can be given by

$$\Delta V_{\rm BG} \approx V_T \ln\left(\frac{I_{\rm s1o}}{I_{\rm s1}}\right) \approx V_T \ln\left(\frac{1}{\gamma(\varepsilon)}\right) = -V_T \ln[\gamma(\varepsilon)] \tag{2}$$

where $V_T$ is the thermal voltage, and $I_{\rm slo}$ and $I_{s1}$ are un-stressed and stressed reverse saturation currents of $Q_1$ (Fig. 1), respectively. Therefore, the effect of package stress on the bandgap reference is to lower its voltage by an amount approximately given by (2).

### C. Effects on the Bandgap's Package Shift

Theoretically, post package stress is a result of a difference in the thermal expansion coefficients of the plastic mold and the silicon die. It can be approximately shown, as a result, that

$$\varepsilon \propto s \propto (T_{\rm sp} - T); \qquad T < T_{\rm sp} \tag{3}$$

where $\varepsilon$ is the die strain, $s$ is the stress on the die, and $T$ is temperature below the molding set-point $T_{\rm sp}$, which is usually around 175 $^\circ$C [12]. The stress placed on the die by the plastic is directly proportional to the molding set temperature. Consequently, the bandgap voltage shift worsens with higher temperature differentials from the molding set point. Because stress is directly proportional to temperature deviations, and since $\gamma(\varepsilon)$ can be approximated by an exponential relationship (the Appendix), (2) and (3) show that the bandgap voltage shift resembles a parabolic relationship with temperature

$$\begin{aligned}\Delta V_{\rm BG} &\approx -V_T \ln[\gamma(\varepsilon)] \approx -V_T \ln\left[e^{k_1 s + c_2}\right] \\ &= -V_T \ln\left[e^{c_1(T_{\rm sp}-T)+c_2}\right] = -c_0 T[c_1(T_{\rm sp} - T) + c_2]\end{aligned} \tag{4}$$

where $k_1$, $c_0$, $c_1$, and $c_2$ are mathematical representations of combined physical, semiconductor, and package related constants.

## IV. Minimizing Package Shift

Because of the complexity and irregularity of the stress in plastic packages, the bandgap package shift, from unit to unit, is not completely consistent. The package shift can therefore be represented with two components: a systematic mean and a random component. The systematic mean component is largely based on the particular plastic package used and the process used to package it, and is reflective of the stress placed on the die by that package type. Consequently, the systematic component can be compensated in the design phase. The random component of the shift, on the other hand, is the result of unpredictable variations of the stress matrix and is assumed to conform to a Gaussian distribution.

Considering the distribution and magnitudes of the stress components, as discussed earlier, the center of the die provides the greatest safeguard against stress. Precise matching of critical components within the Brokaw cell also alleviates the random component of package shift. Further, if the fabrication process permits, $R_1$ and $R_2$ in Fig. 1 should be designed with a low piezoresistive material. In general, polysilicon resistors exhibit much lower piezoresistivity than diffused resistors.

In minimizing package shift, the effects of overall die aspect ratio, die surface texture, and mechanically compliant layers ("sandwich layers") have been investigated. The aspect ratio of the die can determine the level of strain the die experiences under stress. Deformation of the die, such as structural twisting and bending, which is a function of torque placed on the die, affects all the devices on the die and adds to the effects of localized strain. Rectangular structures with large aspect ratios, length to width, are more prone to such deformations under stress than square structures made of the same material. Therefore, square dies potentially yield better performance than their rectangular counterparts in minimizing the random component of the package shift.

Under normal processing, the surface of the die has an uneven texture, mainly a result of the presence of the top metal layer. The top metal lines yield abrupt topographical "humps" while the pitch between them creates "troughs." The field-oxide and passivation layers on top mimic this incoherent texture. A cross-sectional image of a nonplanarized wafer is shown in Fig. 2(a). As a result of this coarse surface texture

IEEE Proof

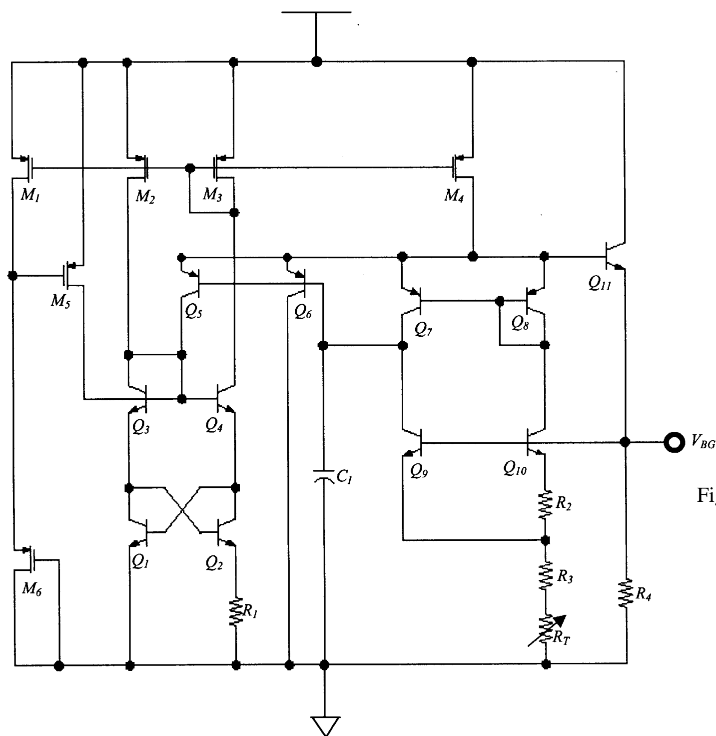


Fig. 3. Practical bandgap circuit used for measuring package shift.

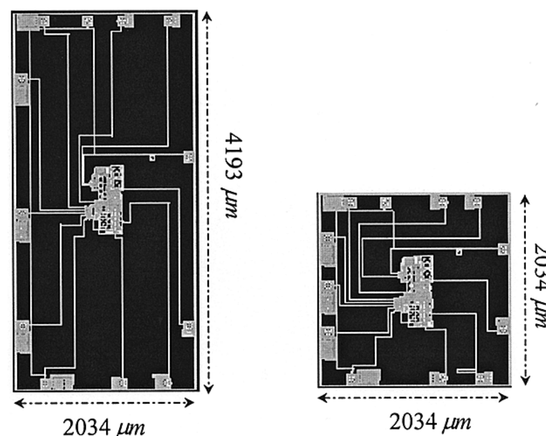


Fig. 4. Rectangular and square die plots.

TABLE I
PACKAGE-SHIFT STATISTICS

| | | SQUARE DIE $\Delta V_{BG}$ | RECTANGULAR DIE $\Delta V_{BG}$ | TRIMMED UNITS $\Delta V_{OFFSET}$ |
|---|---|---|---|---|
| NON-PLANARIZED | $\mu$ [mV] | -5.06 | -5.87 | -5.1 |
| | $3\sigma$ [mV] | 7.92 | 8.25 | 10.8 |
| | # of DUT | 18 | 16 | 27 |
| PLANARIZED | $\mu$ [mV] | -4.26 | | -4.9 |
| | $3\sigma$ [mV] | 6.51 | | 10.34 |
| | # of DUT | 17 | | 32 |
| SANDWICH LAYER | $\mu$ [mV] | -2.26 | | -3.9 |
| | $3\sigma$ [mV] | 4.14 | | 7.05 |
| | # of DUT | 10 | | 31 |

and the fillers in the plastic mold, the stress field from the plastic mold is nonuniform. Such a nonuniform field leads to enhanced random shift behavior. Therefore, planarizing the surface, to flatten it, alleviates the random shift. A cross-sectional image of a planarized wafer is shown in Fig. 2(b).

An elastic thick-film layer in-between the plastic mold and the die surface can absorb some of the stress from the plastic mold and minimize the "filler-induced effects" by distancing the die away from the filler-loaded plastic. Therefore, an elastic "sandwich layer" 15 $\mu$m thick, can minimize the random package shift component by achieving a uniform stress field. Fig. 2(c) shows an image of a chip with a "sandwich layer" placed between the die and the plastic. Note that, before depositing the "sandwich layer" (proprietary stress-relief material), the wafer was planarized. Most other conventional stress-relief layers, such as spin-on coats, are costly and require thick-profile packages. Although planarization techniques and stress-relief layers may not be offered by all process technologies, the concepts discussed above apply universally to all processes.

## V. EXPERIMENTAL SETUP AND RESULTS

A test suite was designed to investigate the effects of aspect ratio, die surface texture, and "sandwich layers" on bandgap package shift. The test suite consisted of a well-characterized Brokaw-type bandgap reference (Fig. 3) placed squarely on the center of both a square die ($W \times L = 2034 \times 2034$ $\mu\text{m}^2$) and a rectangular die ($W \times L = 2034 \times 4193$ $\mu\text{m}^2$), shown in Fig. 4. The wafers were (100) silicon. To ascertain the effects of planarization and the 15 $\mu$m thick "sandwich layer," only the square dies were tested. Non-planarized dies were used to test aspect ratio effects. To simulate and statistically analyze the effects of the planarization and the "sandwich layer" methods in actual production, some of the devices were trimmed to 1.2 V before packaging. As a result, these devices display a narrow rectangular distribution resulting from finite trim resolution. Each die was data logged, for tracking purposes, before and after packaging. Keeping track of each device allowed the individual package shifts to be monitored and statistically analyzed. The square and rectangular dies, as well as the $n$-$p$-$n$ BJT structures were packaged in 16-pin plastic dual-inline-packages (PDIP).

The statistical mean and the standard deviation results of the package shift for the square dies sent through all three processes, the rectangular dies sent through just the normal nonplanarizing process, and post-package voltage variations for the trimmed devices are summarized in Table I. The table also provides the number of devices tested. The measurements were taken at room temperature. The nonplanarized square dies yielded marginally better performance (16%–18%) than rectangular dies. Dies coated with the 15-$\mu$m sandwich layer yielded significantly improved performance (47%–48%), compared to noncoated dies. The temperature dependence of the bandgap package shift was also investigated. Measurements were performed at 15, 25, 50, 75, and 100 °C. Fig. 5 shows the temperature variation of the bandgap package shift for several devices. Note that the empirical data indicates a mostly linear relationship of package shift versus temperature, which are the perceived effects of a small temperature range. Additionally, the temperature coefficient (TC) of the package shift shows variation from unit to unit, just like package shift itself. For this experiment, assuming a mostly linear TC for the package shift, the average TC was about 0.044 mV/°C and its standard deviation was about 0.012 mV/°C. Fig. 6(a) shows a temperature measurement of a bandgap reference before (at probe station) and after packaging, while Fig. 6(b) shows the temperature variation of package shift which is the difference between pre-package and post-package values of Fig. 6(a). Note that the TC of

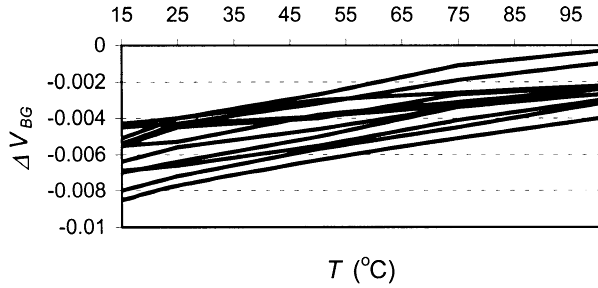


Fig. 5. Measurements of package shift offset ($\Delta V_{BG}$) with temperature.

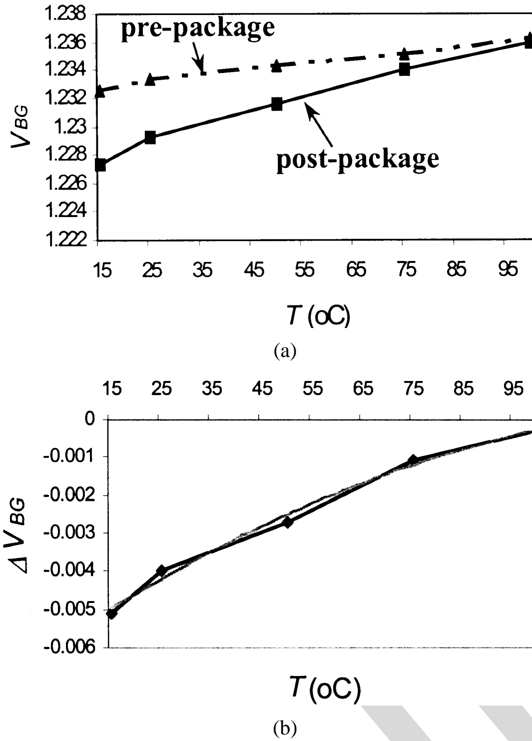


Fig. 6. Temperature variations of (a) $V_{\rm BG}$ before and after packaging, and (b) $\Delta V_{\rm BG}$.

the bandgap reference becomes more positive after packaging. The designer, as a result, can compensate the mean by including the TC of the package shift in the temperature compensation of the circuit.

## VI. Conclusion

Package-induced offsets, unfortunately, vary from unit to unit while roughly conforming to a Gaussian distribution. From a designer's perspective, the problem is addressed in two ways: 1) compensating the mean offset as well as the mean TC and 2) minimizing the effects of the mechanisms that cause random variation. The best approach to compensate for the mean package shift offset and its TC, which turns out to be mostly linearly positive in the temperature range of interest, is to include it in the design of the circuit itself. As a result, characterization of the bandgap circuit within its particular package is required. Additionally, if the process technology permits, adding a moderately thick, yet thin relative to dropper-applied and spin-on overcoats, layer of elastic material between the die and the plastic mold yields significant improvements, a marginal cost that, depending on the application, may be worthwhile.

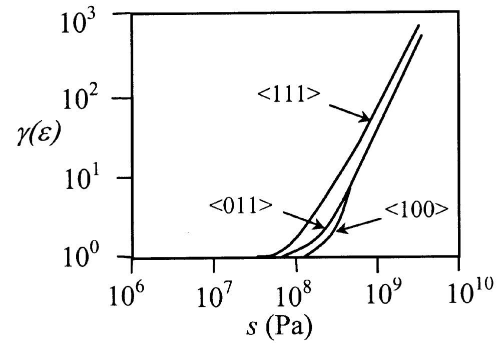


Fig. 7. Ratio of stressed to unstressed minority carrier density as a function of stress in silicon. Values are given for $\langle 000\rangle$, $\langle 111\rangle$, and $\langle 011\rangle$ uniaxial compression stress [10].

## Appendix

### *Derivation*

Ratio of stressed to unstressed minority carrier density

$$\frac{p_n}{p_{\rm no}} \equiv \gamma(\varepsilon_n) \geq 1 \quad \text{and} \quad \frac{n_p}{n_{\rm po}} \equiv \gamma(\varepsilon_p) \geq 1$$

where $p_n$, $n_p$-stressed minority carrier concentrations in $n$-type and $p$-type material, all "o" subscripts denote unstressed values, $\varepsilon_n$, $\varepsilon_p$-position-dependant strains in $n$-type and $p$-type material. $\gamma$ is a function of stress (Fig. 7) and approximated by a single exponential only in the stress region $10^8$–$10^9$ Pa—otherwise, a function of several exponentials—which is the approximate magnitude of stress in plastic packages. Reverse saturation current

$$I_s = \frac{qA\overline{D}_n n_p}{W_B} = \frac{kA\overline{\mu}_n T n_p}{W_B}$$

where $q$—electric charge, $k$—Boltzman's constant, $A$—emitter cross-sectional area, $\overline{D}_n$—average effective electron-diffusion constant ($\overline{D}_n = \overline{\mu}_n V_T$), $\overline{\mu}_n$—average effective electron mobility, $V_T$—thermal voltage ($V_T = kT/q$), $T$—temperature, $W_B$—base width, and $n_p$—base minority carrier density. Thus

$$I_s = \frac{kA\overline{\mu}_n T n_{\rm po}\gamma(\varepsilon)}{W_B} \approx I_{\rm so}\gamma(\varepsilon).$$

Bandgap voltage $V_{\rm BG}$ (first-order Brokaw reference—Fig. 1)

$$V_{\rm BG} = V_{\rm BE1} + 2\frac{R_2}{R_1}V_T \ln(N)$$

where $V_{\rm BE1}$—base–emitter voltage of $Q_1$, $V_T$—thermal voltage, and $N$—emitter area ratio of $Q_2$ and $Q_1$ ($N = I_{s2}/I_{s1}$), and $I_{s1}$, $I_{s2}$ saturation currents of $Q_1$ and $Q_2$. Bandgap voltage shift

$$\begin{aligned}\Delta V_{\rm BG} &= V_{\rm BG} - V_{\rm BGo}\\ &= \left[V_{\rm BE1} + 2\,\frac{R_2}{R_1}\,V_T \ln(N)\right] - \left[V_{\rm BE1o} + 2\,\frac{R_{2o}}{R_{1o}}\,V_T \ln(N_o)\right].\end{aligned}$$

If the circuit is in a uniform stress field (with a proper layout—to match resistors and BJTs)

$$\frac{I_{\rm s2}}{I_{\rm s1}} \approx \frac{I_{\rm s2o}}{I_{\rm s1o}} \Rightarrow N \approx N_o, \qquad \frac{R_2}{R_1} \approx \frac{R_{2o}}{R_{1o}}$$

and

$$\Delta V_{\rm BG} \approx V_{\rm BE1} - V_{\rm BE1o} = V_T \ln\left(\frac{I}{I_{\rm s1}}\right) - V_T \ln\left(\frac{I_o}{I_{\rm s1}}\right)$$

$$= V_T \ln\left(\frac{I I_{s1o}}{I_o I_{s1}}\right)$$

where $I = V_T \ln(N)/R_1$—collector current. Since $N$ is approximately equal to $N_o$—stress effects on resistor $R_1$ are negligible (e.g., polysilicon resistors [11])—$I$ is roughly equal to $I_o$ and

$$\Delta V_{BG} \approx V_T \ln\left(\frac{I_{s1o}}{I_{s1}}\right) \approx V_T \ln\left(\frac{1}{\gamma(\varepsilon)}\right) = -V_T \ln[\gamma(\varepsilon)].$$

## ACKNOWLEDGMENT

The authors would like to thank A. Hastings for his technical advice and feedback as well as T. Dillard for his help in laboratory experiments.

## REFERENCES

[1] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 1993.
[2] G. A. Rincon-Mora, *Voltage References: From Diodes to Precision High-Order Bandgap Circuits*. New York: Wiley, 2001.
[3] H. Ali, "Stress-induced parametric shift in plastic packaged devices," *IEEE Trans. Comp., Packag., Manufact. Technol. C*, vol. CPMTC-20, pp. 458–462, Nov. 1997.
[4] S. Gee, T. Doan, and K. Gilbert, "Stress related offset voltage shift in a precision operational amplifier," in *Proc. 43rd Electronic Components and Technology Conf.*, 1993, pp. 755–764.
[5] R. Pendse and D. Jenning, "Parametric shifts in devices: Role of packaging variables and some novel solutions," in *Proc. 40th Electronic Components and Technology Conf.*, 1990, pp. 322–326.
[6] R. C. Jaeger, J. C. Suhling, R. Ramani, A. T. Bradley, and J. Xu, "CMOS stress sensors on (100) silicon," *IEEE J. Solid-State Circuits*, vol. 35, pp. 85–95, Jan. 2000.
[7] R. E. Thomas, "Stress-induced deformation of aluminum metallization in plastic molded semiconductor devices," *IEEE Trans. Comp. Hybrids, Manufact. Technol.*, vol. CHMT-8, pp. 427–434, Dec. 1985.
[8] K. M. Schlesier, S. A. Keneman, and R. T. Mooney, "Piezoresistivity effects in plastic-encapsulated integrated circuits," *RCA Rev.*, vol. 43, pp. 590–607, Dec. 1982.
[9] H. Matsumoto, M. Yamada, J. Fukushima, T. Kondo, N. Kotani, and M. Tosa, "New filler-induced failure mechanism in plastic encapsulated VLSI dynamic MOS memories," in *Proc. IEEE Int. Reliability Physics Symp.*, 1981, pp. 180–183.
[10] J. J. Wortman, J. R. Hauser, and R. M. Burger, "Effects of mechanical stress on $p$–$n$ junction device characteristics," *J. Appl. Phys.*, vol. 35, pp. 2122–2130, 1964.
[11] A. Hastings, *The Art of Analog Layout*. New York: Wiley, 2000.
[12] H. C. J. M. van Gestel, L. van Gemert, and E. Bagerman, "On-chip piezoresistive stress measurement and 3D finite element simulations of plastic DIL 40 packages using different materials," in *Proc. 44th Electronic Components and Technology Conf.*, 1993, pp. 124–133.

IEEE Proof