A Low-Impedance, Sub-Bandgap 0.6μm CMOS Reference with 0.84% Trimless 3-σ Accuracy and –30dB Worst-Case PSRR up to 50MHz

Vishal Gupta, *Member, IEEE,* and Gabriel A. Rincón-Mora, *Fellow, IET, and Senior Member, IEEE*

Georgia Tech Analog, Power, and Energy ICs Laboratory

School of Electrical and Computer Engineering
Georgia Institute of Technology
777 Atlantic Drive
Atlanta, GA 30332-0250
vishalg@ti.com, rincon-mora@ece.gatech.edu

***Abstract*—Modern mobile applications demand high performance from low supply voltages to reduce power (extend battery life) and survive low breakdown voltages (imposed by sub-micron CMOS technologies), which is why precise low-impedance sub-bandgap references (below 1.2V) that are independent of process, package stress, supply, load, and temperature are critical. However, improving dc accuracy by trimming requires test time (cost) in production and dynamic-element matching (DEM) introduces switching noise. Additionally, improving ac accuracy by rejecting supply ripple with cascodes increases headroom requirements and shunting coupled noise with series low-impedance buffers introduces temperature-sensitive offsets that degrade dc accuracy. This paper presents a prototyped 0-5mA, 890mV, low-impedance, 0.6μm CMOS reference with a trimless 3-σ unloaded dc accuracy of 0.84% across -40°C and 125°C (2.74% when loaded with 0-5mA and supplied from 1.8-3V) and a worst-case power-supply ripple rejection (PSRR) of -30dB up to 50MHz. The design adopts a low-cost, noise-free, self-selecting Survivor scheme to automatically select the best matching pair of devices among a bank of similar pairs during start-up (or power-on reset) and use them**

for critical functions in the circuit. A compact, low-voltage, charge-pumped cascoding strategy and a bandgap-embedded shunt-feedback loop suppress supply and coupled noise.

***Index Terms*—voltage reference, bandgap, mismatch, supply rejection, PSRR**

I. Bandgap References

A bandgap reference is an integral component of any power management system, and in portable applications, attributes like low cost, high integration, and small form-factor are critical [1]. These performance requirements continue to drive system-on-chip (SoC) integration, forcing designers to build critical analog blocks like the reference on the same digital-friendly CMOS die and alongside noisy digital-signal-processing (DSP) and switching power-supply circuits [1]-[5]. While these requirements have an important influence on design decisions, the primary figure of merit for a reference is its overall dc accuracy over temperature, process, component-mismatch, package-stress, supply-voltage, and load variations and ac accuracy over load and line transient events, that is, its ability to recover from load dumps and reject supply ripple noise.

Bandgap references are accurate over temperature because their compensated output is the balanced sum of a proportional-to-absolute-temperature (PTAT) voltage, which increases linearly with temperature, and a complementary-to-absolute-temperature (CTAT) voltage, which decreases with temperature. In conventional CMOS schemes (Fig. 1 [2]-[7]), the CTAT component is derived from the base-emitter (diode) voltage of a substrate PNP transistor and the PTAT counterpart from the difference in the base-emitter (diode) voltages of two substrate PNPs with unequal current densities, the result of which is a *bandgap* voltage (approximately 1.2V):

$$V_{REF} = V_{CTAT} + V_{PTAT} = V_{BE1} + \left(\frac{\Delta V_{BE}}{R}\right) R_{PTAT} = V_{BE1} + \left(\frac{V_T \ln(C)}{R}\right) R_{PTAT} \approx V_{BG} \approx 1.2V, \quad (1)$$

where C is the ratio of current densities in the two PNP transistors.

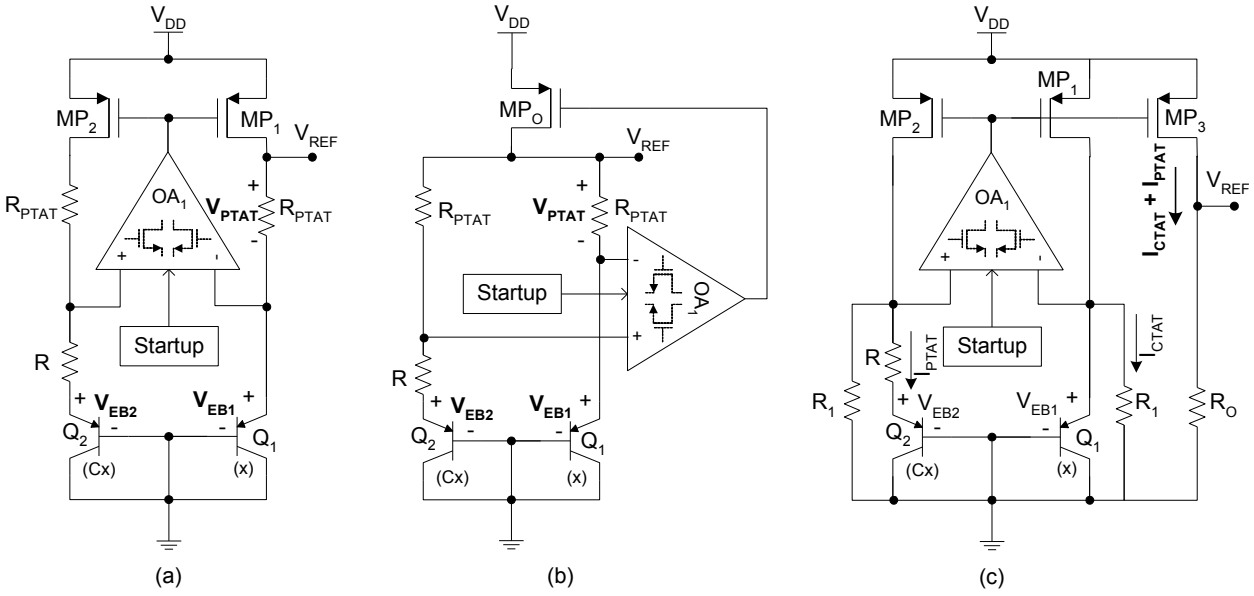


Fig. 1. CMOS (a), (b) bandgap and (c) sub-bandgap references.

With the advent of low-voltage demands for low-power (and extended battery life) and low breakdown voltages, however, 1.2V references are losing their appeal over their sub-bandgap counterparts (below 1.2V) [7]-[10]. Generating sub-bandgap voltages in modern CMOS environments normally require current- [8]-[9] or current-voltage hybrid-mode [10] approaches (Fig. 1(c)), where PTAT and CTAT currents are sourced and summed into resistors to generate a temperature-compensated voltage. The disadvantage of using this approach for generating sub-bandgap references is ac (transient) response, as will be discussed in Section II.

II. Accuracy Performance

A number of factors degrade accuracy in CMOS bandgap circuits, including process tolerance and mismatch [11]-[15], package shift (mismatch induced by the package, which generates localized stress fields on the silicon die that induce parametric variations across adjacent devices) [15]-[17], ac and dc power-supply fluctuations [18]-[19], ac and dc load variations [20]-[22], and temperature changes [5], [7]. Mitigating the effects of this diverse set of variable conditions in a CMOS environment under low power and low voltage constraints is challenging.

Trimming is a well-known strategy to reduce dc variations by tweaking the PTAT component of the reference voltage (typically by changing resistor R_{PTAT} in Eq. (1)) until it compensates for the first-order CTAT dependence of V_{BE} [5], [9]-[10], [20]. Though trimming

eliminates variations that have linear temperature dependence, like mismatch in bipolar transistors and resistors, it is ineffective against variations that are non-linear with respect to temperature, like mismatch in MOS transistors [23], which, given the use of CMOS technologies, are inevitably employed in critical roles. In Fig. 1, for instance, mismatch in MP_1-MP_2 and the offset of OA_1, which is conventionally designed using MOS devices, are particularly important sources of error that cannot be trimmed by conventional strategies. Additionally, since almost every bandgap reference die requires trimming, the process incurs significant manufacturing costs, especially when performed post-package, when few access points (pins) are available [5]. EEPROM can circumvent some of these deficiencies but the associated circuitry adds complexity and programming time (test time). As a result, low-cost, high-volume SoC applications, like portable electronics, demand high accuracy with minimal to no trimming [12].

To avoid trimming, dynamic-element matching (DEM) [12]-[15] was developed. DEM is becoming increasingly popular because the adverse effects of mismatch on accuracy are virtually eliminated without trimming. The idea is to periodically interchange the electrical connectivity of two supposedly matched devices and therefore *average*, over time, their mismatch effects to zero, since each connection sees an equal proportion of the offset. Switching the connectivity of devices inside the reference, however, generates systematic switching noise, which in the context of a practical SoC solution, permeates to critical noise-sensitive blocks, like phase-locked loops (PLLs), voltage-controlled oscillators (VCOs), and analog-digital converters (ADCs).

Large filter capacitors can reduce the glitches produced by DEM and supply ripple, improving the reference's ac accuracy [2], [19]. Integrating these capacitors on-chip with the rest of the SoC, however, is prohibitively expensive because capacitance-per-unit area in modern CMOS technologies is relatively low, resulting in exorbitantly large die areas. Moreover, adding off-chip capacitors negate the principal advantages of SoC integration by increasing the solution's overall footprint. Increasing the effectiveness of smaller capacitors with large series resistors to decrease the -3dB roll-off frequency of the filter to, for instance, better shunt supply ripple [2], is also prohibitive because the series resistor conducts (and dissipates) quiescent power (which decreases battery life) and reduces the voltage headroom under which the circuit must operate.

As mentioned earlier, sub-bandgap voltages are normally realized by summing PTAT and CTAT currents into a resistor (Fig. 1(c)). This approach produces a relatively high-impedance reference, which is unfortunately vulnerable to transient load-current variations and coupled noise. As a result, a series linear regulator is often used to buffer and shunt the noise (Fig. 2), effectively providing a low-impedance output. The buffer, however, introduces additional random- and systematic-offset components to the reference, significantly degrading its overall dc accuracy [22]. This phenomenon is particularly troubling in CMOS technologies because MOS offsets have a non-linear dependence to temperature, which trimming cannot properly cancel.

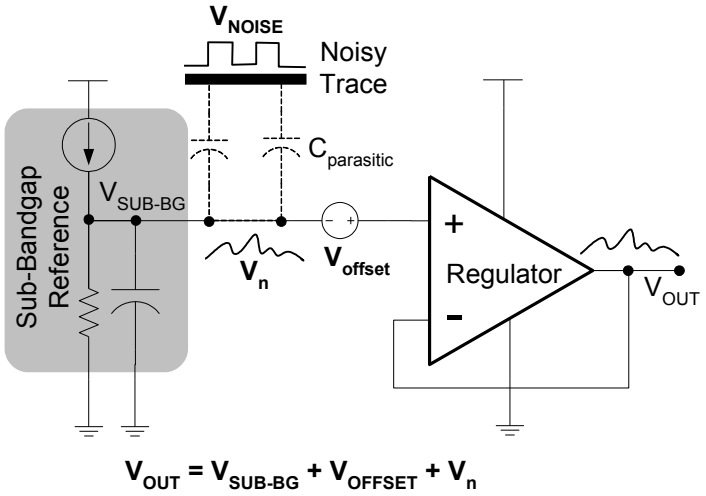


Fig. 2. Reference-regulator low impedance circuit and its adverse treatment of noise and offset.

Instead of inserting a series regulator, or an op amp in unity-gain configuration, to decrease the output impedance, the output of the reference (itself) can be regulated via an integrated shunt-feedback loop (Fig. 1(b)). A low output-impedance reference is especially desirable for noise-sensitive applications like ADCs, VCOs, and PLLs because of its noise-shunting and current-sourcing capabilities [2], [6], [20]-[21], [25]-[27]. For this reason, most of the references used in industry for these types of applications conform to slight variations of the regulated reference presented in Fig. 1(b), producing reference voltages at or above 1.2V [6], [20]-[21], [25], [27], not the sub-bandgap voltage levels now desired by a growing number of sub-micron SoC CMOS solutions intended for battery-powered applications.

III. Proposed Low-Impedance, Sub-Bandgap, Trimless CMOS Reference

The objective of this paper is to present an accurate sub-bandgap, trimless CMOS reference that is immune to process- and package-induced mismatch, temperature, load (static and dynamic), and supply variations (static and dynamic) by using low-cost, noiseless, and SoC techniques with minimal impact on voltage headroom. The proposed system consists of three primary components, as shown in Fig. 3: (1) a low-impedance, sub-bandgap voltage reference immune to variations in temperature (to first order), line, and load [28]; (2) a *Survivor* block that automatically selects the best matched device pair out of a bank of similarly sized pairs during start-up and subsequently uses it in the reference, noiselessly compensating for mismatch and package-stress offsets [29]; and (3) a charge-pumped NMOS cascode to decouple the supply ripple from the output without using large off-chip capacitors or considerably increasing voltage headroom [30]-[31].

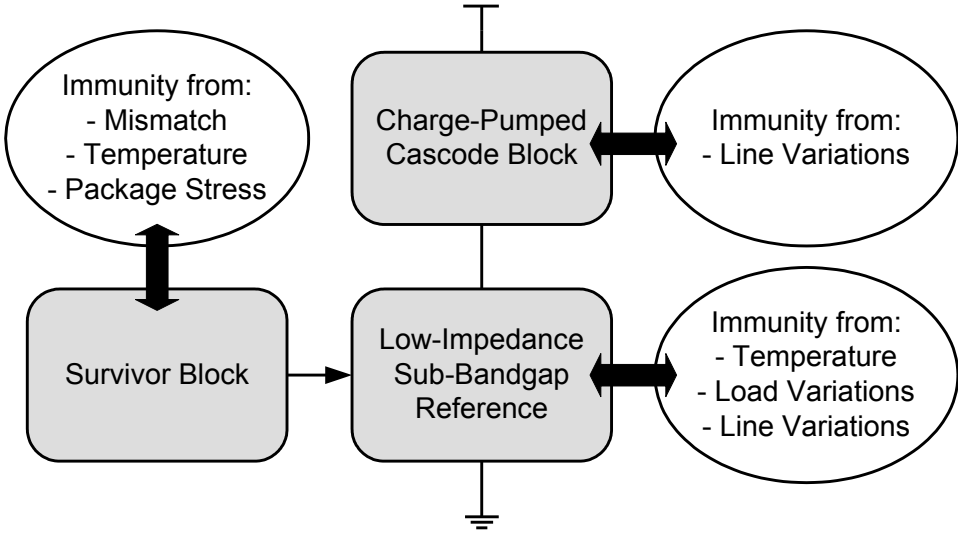


Fig. 3. Conceptual block diagram of trimless reference.

Low-Impedance, Sub-Bandgap Reference

Concept: For shunt feedback, which is necessary for low output impedance and consequently high accuracy in the presence of ac load variations and/or coupled noise, a voltage in the output must be sensed and fed back, which is why the output must be comprised of temperature-dependent voltages (not currents), as illustrated in Figs. 1(a) and 1(b). To produce sub-bandgap voltage levels, however, only a fraction of the diode voltage must be in the output path, as shown in the proposed circuit of Fig. 4, where voltage divider R_{11}-R_{12} defines a fraction of diode voltage V_D across R_{12} and R_{13} a PTAT current – using superposition:

$$V_{REF} = V_D \frac{R_{12}}{R_{11}+R_{12}} + V_{PTAT} \frac{(R_{11} \| R_{12})}{R_{13}} + V_{PTAT} = V_D \frac{R_{12}}{R_{11}+R_{12}} + V_{PTAT}\left[1 + \frac{(R_{11} \| R_{12})}{R_{13}}\right]$$

$$= AV_{CTAT} + BV_{PTAT}, \qquad (2)$$

assuming the impedance across diode D is negligibly small (designed to be more than an order of magnitude lower than R_{11}+R_{12}) and A and B are temperature-independent constants. Since the output is now a series combination of voltages, a voltage can be sensed and shunt-negative feedback applied. In this case, V_{PTAT} is sensed and regulated with op amp OA_1 and power PMOS MP_O. OA_1 has a pre-set PTAT offset voltage and the loop responds to ensure this voltage is impressed across R_{13}. Because series pass device MP_O is a PMOS, as in low-dropout regulators (LDOs), the regulated reference can sustain low supply voltages under relatively high load currents; in other words, it can source high output currents and simultaneously incur low-dropout voltages.

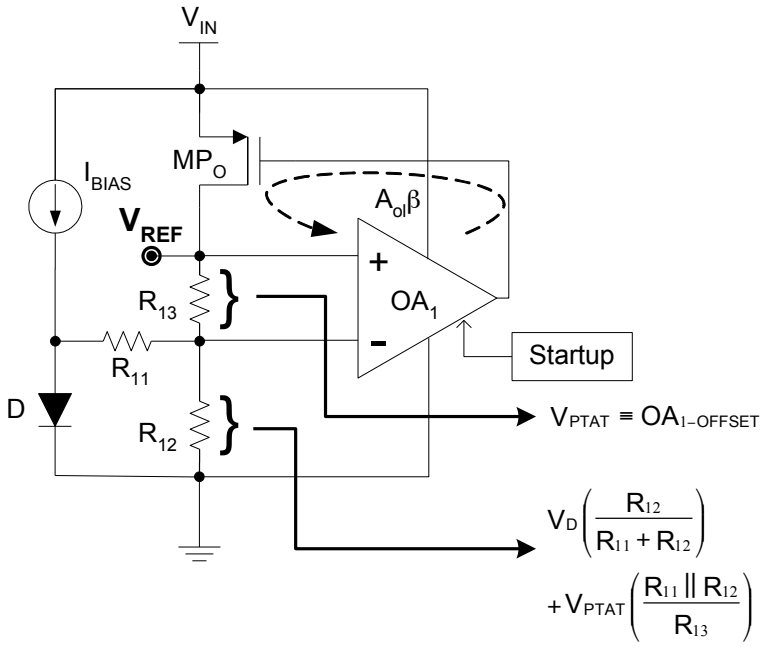


Fig. 4. Block diagram of proposed low-impedance, sub-bandgap reference.

Circuit: The complete circuit comprised of OA_1, a biasing block, and the output stage depicted in Fig. 4, is shown in Fig. 5. Lateral PNP differential-input pair QP_{21}-QP_{22} (available in standard CMOS technologies and used in voltage references in [21], [25], [28]), current mirror MP_{21}-MP_{22}, current sources MN_{21}-MN_{22}, and cascode transistors MN_{23}-MN_{24} constitute amplifier OA_1. Resistors R_{14} and R_{15} implement a voltage divider circuit whose total resistance and series combination is modeled by R_{12}. The bias current is defined by a conventional PTAT

generator block using lateral PNP devices QP_{B1}-QP_{B2} with R_{B1} and a current mirror comprised of MN_{B1} and MN_{B2}, in addition to long-channel start-up device MN_S. The dominant low-frequency pole of the loop is at the gate of MP_O, since the inverting gain stage across compensating capacitor C_M presents a Miller-multiplied capacitance to the gate of MP_O. An asymmetrically sized BJT-input pair is used to define the desired PTAT offset voltage across R_{13}.

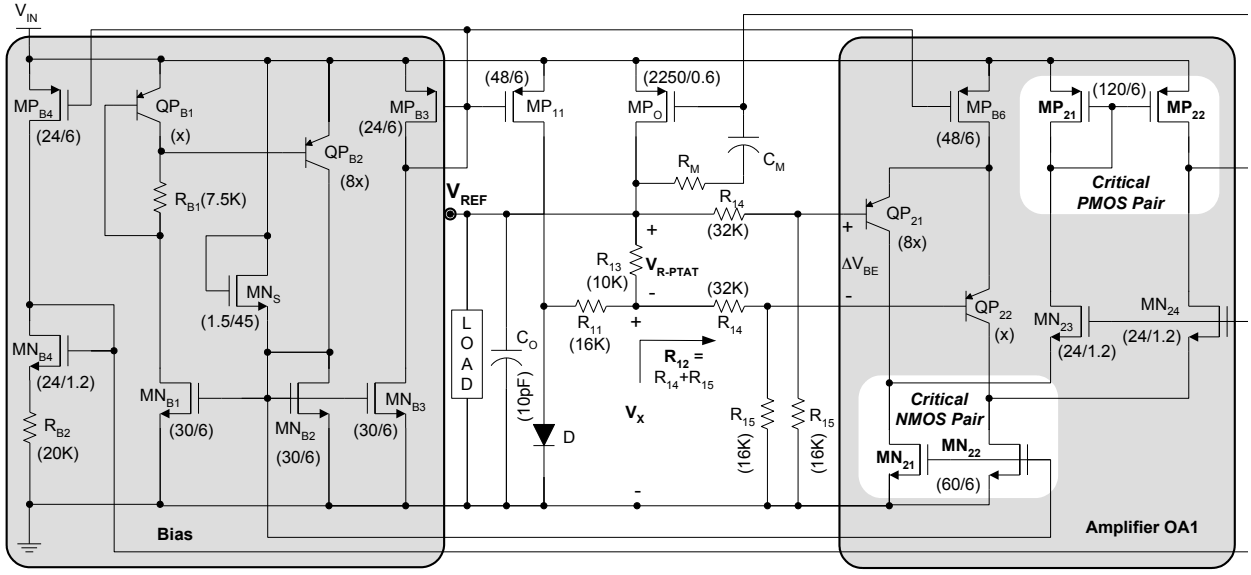


Fig. 5. Complete schematic of proposed low-impedance, sub-bandgap reference.

The lateral PNP devices in this CMOS technology were built with short-channel, source-dotted PMOS transistors (dot-source as the emitter and donut-drain surrounding the gate and source as the collector) and characterized using 15 samples over two fabrication runs from which SPICE-model parameters were extracted and verified. Reverse-saturation current (IS in SPICE's level-2 model), Early voltage (VAF), and β (BF) were measured to be 3fA, 6V, and 100A/A, respectively. Low Early voltages (i.e., low output resistances) are typical for these lateral devices, which is why it is best to buffer their respective currents with common-gate or -base transistors before presenting them high-impedance loads. The folded-cascode topology shown in Fig. 5 does just this: present them low-impedance loads (sources of MN_{22}-MN_{23}) that fold and buffer their currents to a high-impedance load (drain of MP_{22}).

The preset PTAT offset of OA_1 is defined by input pair QP_{21}-QP_{22} and effectively amplified by resistive network R_{14}-R_{15}. MN_{21}-MN_{24} and MP_{21}-MP_{22} force the currents flowing through QP_{21} and QP_{22} to be equal and the difference in their respective emitter areas consequently

introduces a systematic input-referred voltage that is PTAT in nature, much like a traditional PTAT-current generator through a manifestation of the Gilbert principle [32]:

$$V_{OS} = \Delta V_{EB} = V_T \ln\left(\frac{8x}{x}\right) = V_T \ln(8). \tag{3}$$

R_{14} and R_{15} are feedback resistors and a divider network for the voltage across R_{13},

$$V_{R_{13}} = V_{OS}\left(\frac{R_{14} + R_{15}}{R_{15}}\right) = C \cdot V_{OS} = V_{PTAT}, \tag{4}$$

ultimately presenting a PTAT voltage across R_{13}, the same one assumed and used in Eq. 2, where R_{12} is the series combination of R_{14} and R_{15}. In the end, coefficients A, B, and C (i.e., R_{11}-R_{15}) from Eqs. (2) and (4) are designed to cancel and balance the CTAT behavior of diode voltage V_D with the PTAT effects of input-referred offset voltage V_{OS}. Additionally, R_{15} must be considerably smaller than small-signal emitter-base resistance r_π to ensure the voltage-divider ratios presented are independent of r_π, which is not difficult because β is relatively high.

Accuracy: Process variations and mismatch, as noted earlier, have a strong influence on the accuracy of bandgap references. The spread in the base-emitter voltage (V_{BE}) of the bipolar transistor used to generate the CTAT component, for one, which is entirely subject to process variations, can be a considerable source of error because it translates directly into an error in the reference voltage. The substrate PNP-based CMOS references proposed in [12]-[15] employ DEM to eliminate the effect of device mismatch and consequently leave a residual error in V_{REF} of 3-10mV that is primarily due to the spread in V_{BE}. The lower V_{BE} spread these CMOS substrate PNPs exhibit compared to their BiCMOS NPN counterparts is attributed to their wider base width (i.e., n-well base versus a dedicated p-base region), which spatially averages dopant variations in the base, leading to lower current gain but a higher degree of uniformity in base doping and a more stable saturation-current density J_S [15], [35]. Considering the effect of resistor and V_{BE} variations on the proposed topology, a 3-σ variation of 20% in the resistor that sets the bias current of diode D (i.e., R_{B1}) alters the diode voltage by only 3.4mV ($\Delta V_{BE} = V_T \cdot \ln(1.2)$) or 0.4% of the reference.

As in the references shown in Fig. 1, the accuracy of the proposed reference ultimately hinges on the PTAT quality of OA_1's input-referred offset, which depends on resistive network R_{11}-R_{15}, input pair QP_{21}-QP_{22}, current mirror MP_{21}-MP_{22}, and current sources MN_{21}-MN_{22}. Resistors can be matched to 0.1% through careful layout, and the high β of the lateral PNPs

present negligible offset currents [25]. MOS transistors MN_{21}-MN_{22} and MP_{21}-MP_{22}, however, cannot be matched as well as resistors or bipolar transistors because (1) their square-law behavior induces non-linearities in V_T that exacerbate V_T-mismatch effects when biased with lower gate-source voltages and (2) variations in carrier mobility, oxide capacitance, and area produce k' mismatches [23]. While their matching performance can be improved by increasing their active area, this approach lowers the bandwidth of the reference by increasing the parasitic capacitances of the devices that are present in the feedback path, thereby degrading its ability to regulate the output against transient load and supply variations, as will be shown in Section V (buffering the reference with a regulator encounters similar problems because, while small transistors yield higher bandwidth, they introduce larger offset voltages). The proposed Survivor strategy circumvents this accuracy-bandwidth tradeoff by selecting the best matching pair of small-geometry devices out of a bank of similarly sized pairs without introducing noise in the process (as DEM does).

Survivor Strategy

Concept: The heart of the Survivor strategy lies in identifying the best matching pair of devices from a bank of transistor pairs during non-recurring, or infrequent, start-up and/or power-on-reset (PoR) events [29]. The best pair is then used to implement critical devices in the circuit. For the proposed system, one instance of the Survivor strategy chooses the best matched NMOS pair from a bank of similar pairs to implement critical current sources MN_{21}-MN_{22} while another instance chooses the best matched PMOS pair to implement critical current mirror MP_{21}-MP_{22}.Since each start-up sequence activates the Survivor strategy, the bandgap reference is immune to drifts in matching performance resulting from time elapsed and/or packaging conditions. While a prototype of the strategy was used on a simple current-mirror in [29] to improve its matching performance, the strategy is now adapted to the foregoing sub-bandgap reference to improve its (1) initial trimless accuracy performance and (2) temperature coefficient, all without costly trimming and/or noisy DEM techniques.

As shown in Fig. 6, a bank of pairs, each of which is assigned a unique digital code, is fabricated on-chip with the rest of the system, and *every time* the system starts up or resets, a digital engine connects two pairs from this bank to a high-resolution current comparator via a set of switches. The comparator then determines which of the two connected pairs has higher offset (worse mismatch). The digital engine processes the output of the comparator to discard the pair

with the higher offset (the *loser*) and connects another pair from the bank in its place. This new pair is then compared to the *winner* from the previous cycle, and so on. After processing all pairs in the bank, the winner of the last cycle (the *survivor*) is the pair with the least mismatch.

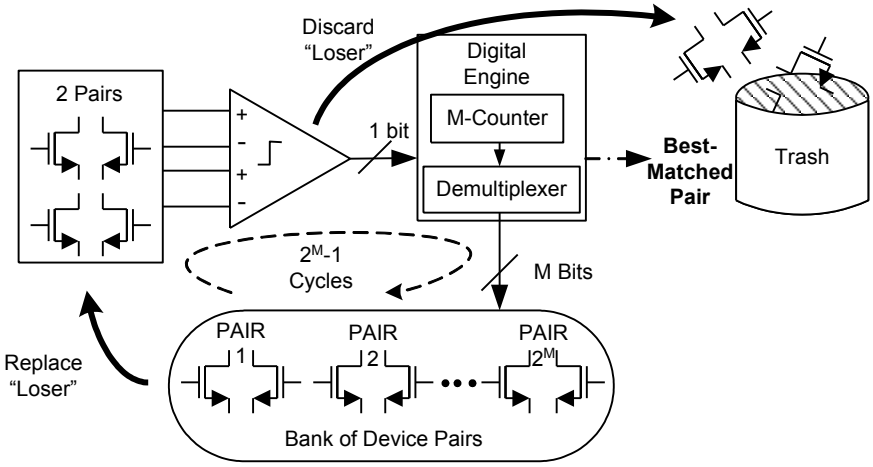


Fig. 6. Block diagram of the Survivor circuit.

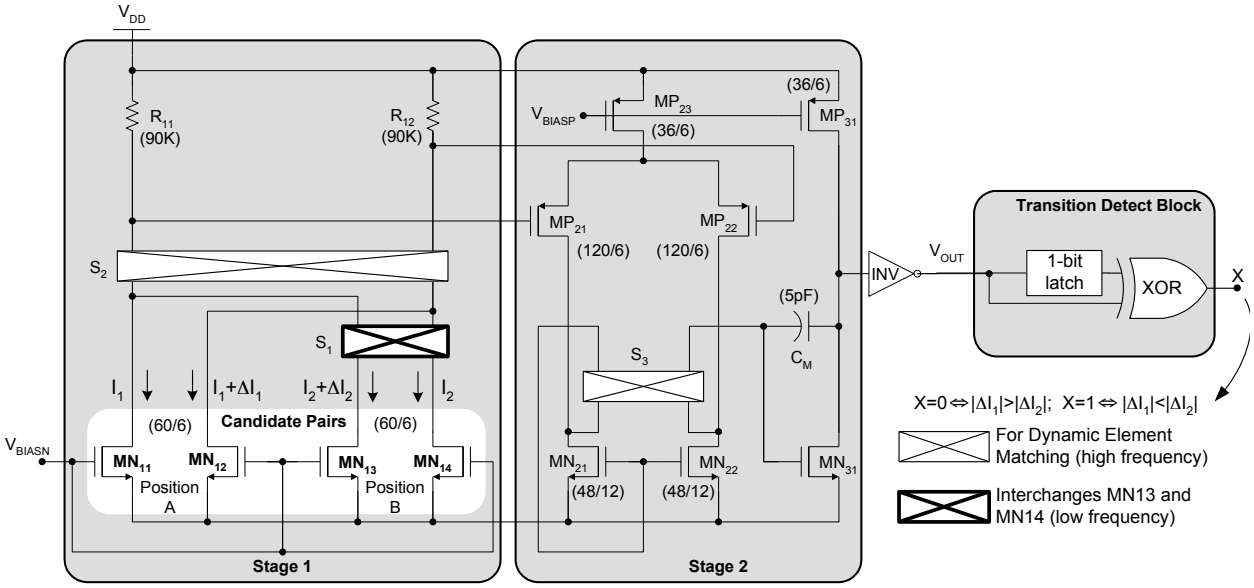


Fig. 7. Schematic of the comparator used to converge on the best matching NMOS pair.

Circuit: The most important component in the Survivor block is the comparator because its resolution determines the matching performance of the winner of every cycle and ultimately the surviving pair. The proposed comparator, shown in Fig. 7, is comprised of four gain stages, including common-source transistor MN_{31} and inverter INV, and a transition-detect block. The two pairs of devices to be tested are first placed in positions A and B and fed to resistors R_{11}-R_{12}. The offsets of these two pairs (ΔI_1 and ΔI_2) determine the state of inverter INV (i.e., V_{OUT} is high if MN_{12} and MN_{14}, when connected together, conduct more current than their respective

counterparts). In the second phase, the connectivity of the pair at position B is reversed and a resulting state change implies the offset of this reversed pair is dominant ($|\Delta I_2| > |\Delta I_1|$); otherwise, no state change occurs. This state-reversal result is then used (via an exclusive OR -XOR- function) to select which pair to discard and to allow the next pair to take the position of the discarded pair, after which point another comparison is processed.

The accuracy of this circuit is key, as it determines the offset of the surviving pair, and is dependent on the matching performance of R_{11}-R_{12}, MP_{21}-MP_{22}, and MN_{21}-MN_{22}. The overall input-referred offset resulting from a current density mismatch in MN_{31}, which is dependent on how well MN_{31} matches MN_{21}-MN_{22} and I_{21} matches I_{31}, is minimal because it is divided by the voltage gain of the first two stages, which is on the order of 50-60dB. Offsets in resistors R_{11}-R_{12} and at the input of the second stage are more critical because they are only divided by the transconductance of the candidate pairs and the gain of the first stage, which is why a dynamic-element-matching (DEM) scheme to match these devices is used. Since DEM only happens during start-up and/or infrequent PoR events, the switching noise it introduces and quiescent power it incurs has minimal impact on system performance. On the other hand, applying DEM by exchanging the connectivity of R_{11}-R_{12}, MP_{21}-MP_{22}, and MN_{21}-MN_{22} several times, with every clock cycle, and therefore, over time, *averaging* their overall effects to zero nearly eliminates all mismatch effects in the comparator. This averaging (low pass filter) function is performed by capacitor C_M, whose Miller effect enhances its filtering capabilities. In simulations, the proposed comparator displayed a worst-case resolution of 90µV with a settling time of 200µs under a 100kHz DEM frequency and 5pF filter capacitor. The transition-detect block the comparator drives detects a change of state by storing the result of the first phase comparison in a 1-bit latch, before the onset of the second phase. The result of the second phase is then compared with that of the first via the XOR gate. If the two states differ, the output of the gate is high, which is the code for a state reversal.

The digital engine uses the output of the transition-detect block to control a switching network that disconnects the loser pair from the comparator and connects the next pair from the bank in its place (while retaining the winning pair). The digital engine consists primarily of counter CTR, demultiplexer DEMUX, and two decoders (DEC_A and DEC_B) that select the pair from the bank to connect to position A or B. CTR generates a digital-code sequence corresponding to each pair in the bank (starting from the third pair, since the first two are

connected to the comparator at the start of the selection process). Based on the output of the transition-detect block, DEMUX routes the code generated by CTR to either DEC_A or DEC_B (for example, if the pair at position B was the loser of the previous cycle, DEMUX routes the next sequential code to DEC_B, thereby changing its output while keeping the output of DEC_A intact). A complete schematic of the digital engine can be found in [29].

Advantages: An important feature of the Survivor strategy is that, if package stresses change the matching performance of the bank of device pairs after the sample is packaged, the Survivor strategy still selects the best matching pair post-package, thereby increasing the immunity of the bandgap reference to package shift and consequently enhancing its accuracy performance. Additionally, by selecting the best matching pair and using it to reduce the offset variations of OA_1 (i.e., V_{PTAT}), the Survivor strategy generates a more robust, predictable, and accurate PTAT voltage, which reduces the untrimmed overall temperature variation of the reference. It is also important to note the relatively simple sequential comparison performed by the proposed circuit circumvents the need for large memory banks that would otherwise be required to measure, digitize, and store offset information.

Enhancing Power-Supply Ripple-Rejection (PSRR) Performance

Block Diagram: To decouple the supply ripple from the output and therefore improve ac accuracy, a charge-pumped NMOS cascode (MN_C) is introduced between the reference and the input-supply voltage, as shown in Fig. 8, which is a variation of [2], [30]-[31], [33], shielding the entire sub-bandgap reference (not shown for simplicity) from any fluctuations in the supply. To mitigate the voltage headroom requirements of the cascode, its gate voltage is boosted with charge-pump CP to an appropriately higher level set by a crude reference to ensure the cascode is in saturation and therefore presents a high-resistance path from the reference to the supply. Since MN_C acts like a voltage follower for any noise present at its gate, it is critical to shield the gate of MN_C from any ripple, which is why a series RC filter is used to shunt the charge-pump noise along with any supply ripple that feeds through to ground. And since no dc current flows to the gate, the series filter resistance can be large without incurring any voltage drops or significant power losses. For the IC prototype built, a 500KΩ resistor and a 15pF capacitor were used to set a filter pole of roughly 20kHz. It is important to note that the shunt-feedback loop attenuates low-frequency ripples because the loop gain is high at low frequencies, unlike at higher frequencies, where loop gain is low, which is why a 20kHz ripple is less problematic than

300kHz-10MHz ripples. In all, while the proposed solution yields a lower PSRR performance (-30dB) than [33] (-40dB), it achieves this using on 65pF of on-chip capacitance, compared to 1.2nF used in [33].

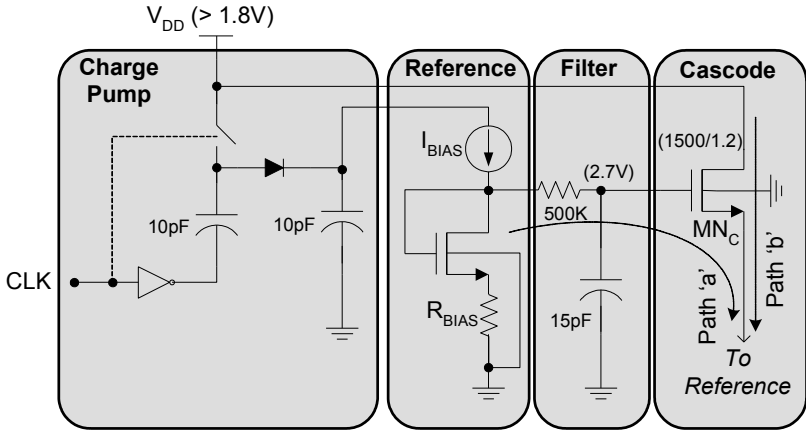


Fig. 8. Block diagram of Cascoding strategy to achieve high PSRR performance.

The minimum supply voltage the system can sustain is now dependent on the minimum voltage required by the core sub-bandgap reference, which is dependent on the output voltage and/or the feedback amplifier OA_1, and the saturation voltage across cascode NMOS MN_C, all of which simplifies to

$$V_{DD(min)} = \max\left\{V_{OUT} + V_{SD.MP_O(sat)} + V_{DS.MN_C(sat)}, V_{TP.MP_O} + 3V_{DS(sat)} + V_{DS.MN_C(sat)}\right\}. \quad (5)$$

More specifically, referring to Fig. 5, $V_{DD(min)}$ is constrained by the headroom voltages associated with MP_O's V_{SG} (i.e., $V_{T.MPo}+V_{SD.MPo(sat)}$) and MN_{23}'s and MN_{21}'s $V_{DS(sat)}$'s. Additionally, given a 0-5mA load-current range, $V_{DD(min)}$ increases considerably with load current, as the saturation voltage of MP_O ($V_{SD.MPo(sat)}$) increases. $V_{DD(min)}$ is consequently lowest at light load currents (e.g., 1.2V with a $V_{T.MPo}$ of 0.6V and $V_{SD(sat)}$'s of 150mV) and highest at maximum load currents (e.g., 300mV higher - 1.5V). Had the load-current requirement been alleviated to maybe 0-250µA, however, which is more compatible with standard references, and a process with a more mainstream PMOS threshold voltage (0.6V) been used, $V_{DD(min)}$ would have been constrained to 1.2V.

IV. Measurement Results

A trimless 0-5mA, 890mV, low-impedance, sub-bandgap 0.6µm CMOS reference prototype (Fig. 9) was designed, fabricated, experimentally tested, and evaluated - the combined measurement results of 30 samples from the same wafer are presented in Figs. 10-14. Overall,

the circuit yielded an untrimmed 3-σ accuracy of 0.84% across -40°C to 125°C. Load-regulation (LDR) effects on the reference were 1.57mV/mA for a 0-5mA load (Fig. 10). Line-regulation (LNR) effects were 0.9mV/V for a 1.8-3V supply. The voltage droops in the reference, which were less than 8mV and 1.5mV over the entire load-current and supply-voltage range in average, respectively, were the result of finite loop gain - including these errors in the overall trimless 3-σ dc-accuracy performance yielded 2.74%. Increasing the loop gain would decrease the effects of these variations, but at the possible cost of compromised stability.

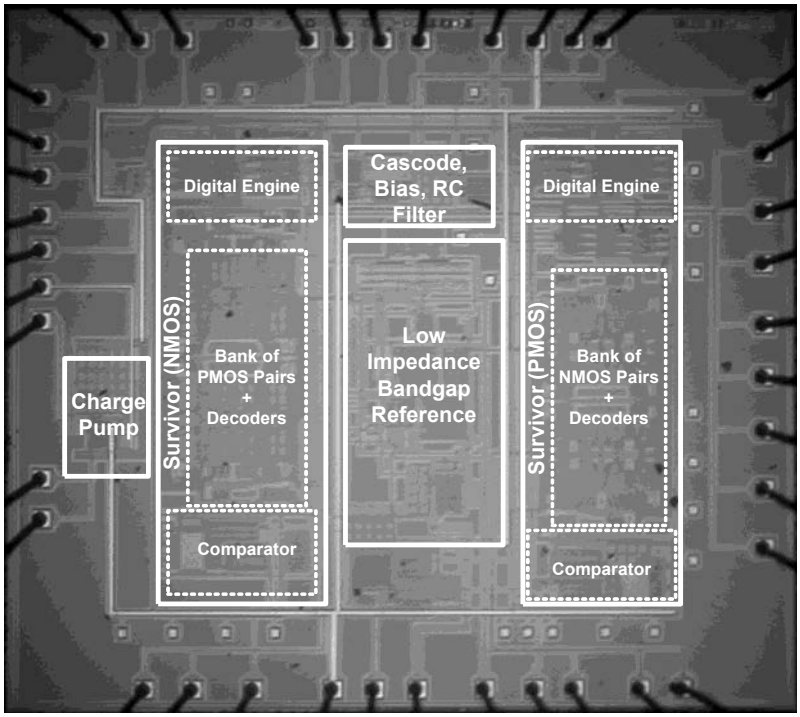


Fig. 9. Die photograph of the trimless low-impedance, sub-bandgap 0.6µm CMOS reference.

A key feature of the design is the Survivor strategy, which is how a trimless 3-σ accuracy of 0.84% was achieved. To verify the functionality of the strategy, that is, whether or not the circuit converged on the best matching pair of devices, the PMOS pairs in the banks of five samples were tested independently, as current mirrors, and their offset results compared against the survivor output (i.e., identity of the surviving pair). The experimental offset measurements of one such bank of devices from a single die sample are presented in Table 1, showing Pair 12 as the best matching pair. Fig. 11 shows the experimental code progression of the Survivor circuit, which converged on Pair 12 as the surviving pair. Similarly, four other banks of devices were tested and the circuit again converged on the best matching pair. To add context to these results,

the 3-σ offset performance of a single PMOS pair, when measured over 30 samples without the Survivor scheme, was 1.95% whereas the Survivor pair was 0.31% (Fig. 12), showing more than a 6× improvement in accuracy with the same geometry dimensions, in other words, achieving the accuracy performance of a larger device with a smaller geometry (higher bandwidth).

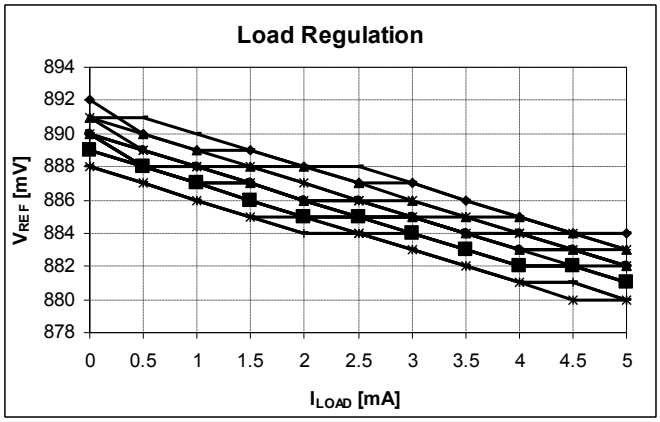


Fig. 10. 0-5mA load-regulation results from 15 samples.

TABLE 1. MEASURED OFFSETS OF PAIRS IN BANK OF 16 DEVICES FOR 1 SAMPLE IC IN 1 LOT.

Pair	Code	Offset [%]	Pair	Code	Offset [%]
0	0000	0.40	8	1000	0.36
1	0001	0.82	9	1001	0.74
2	0010	1.25	10	1010	0.38
3	0011	0.80	11	1011	1.03
4	0100	0.49	12	1100	0.04
5	0101	0.48	13	1101	0.13
6	0110	0.35	14	1110	0.78
7	0111	0.10	15	1111	0.40

The effectiveness of the Survivor strategy in improving the accuracy of the low-impedance, sub-bandgap reference was tested by measuring the output voltage and temperature coefficient (TC) of 30 samples before and after the application of the Survivor strategy. Fig. 13 shows the results of two such samples, where the temperature-induced variation over the span of -40°C to 125°C decreased by approximately 2× when applying the Survivor scheme (from 2mV and 4mV to 0.7mV and 2.2mV, respectively). Specifically, for -40°C, 25°C, and 125°C, the 3-σ accuracy of the output voltage improved from 1.30% to 0.75%, 1.26% to 0.34%, and 1.12% to 0.71%, respectively. The overall spread of the reference is 14.9mV, which corresponds to ±0.84% 3-σ accuracy over temperature and process.

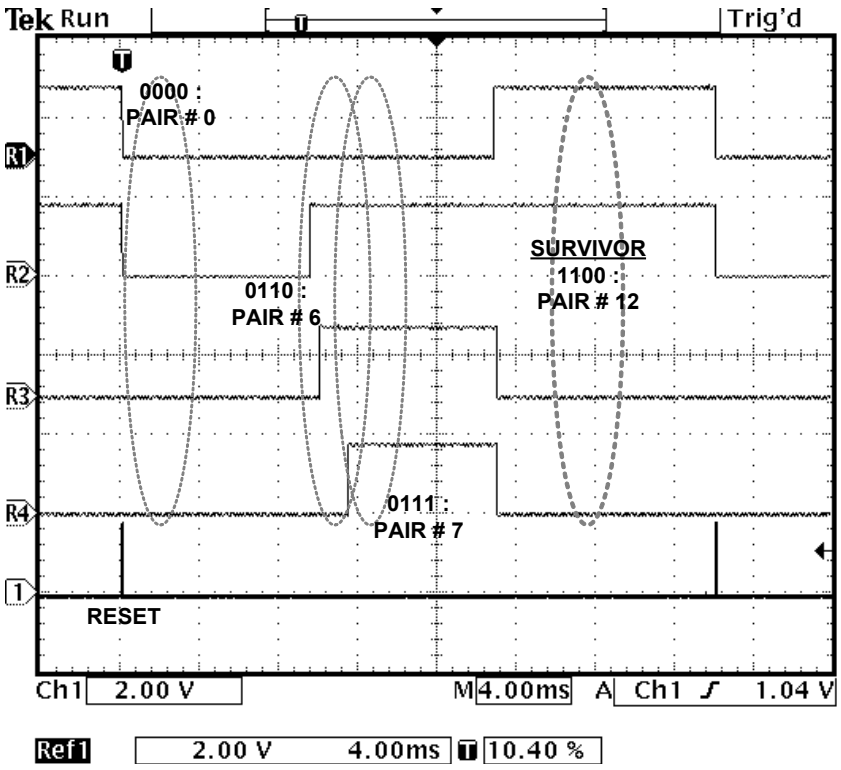


Fig. 11. Experimental digital-code progression of the winning pair for each cycle as the circuit converged on Pair 1100 (Pair 12).

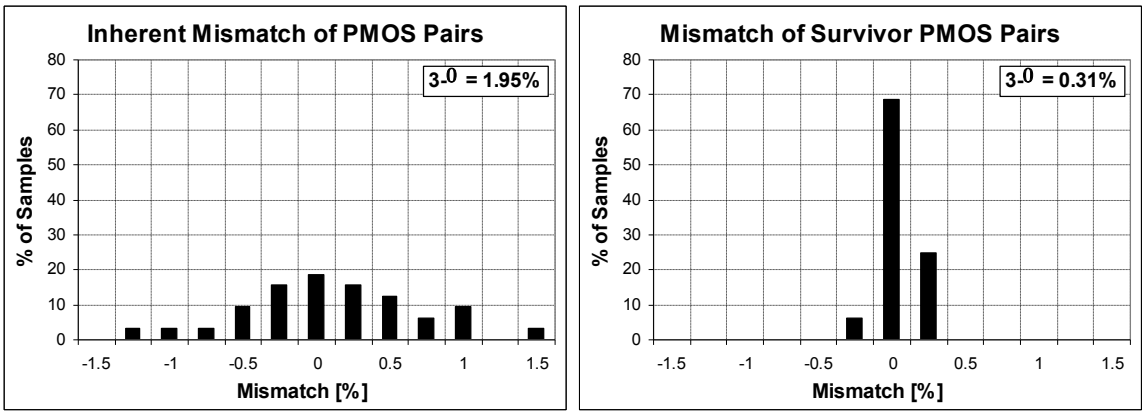


Fig. 12. Experimental statistical offset performance of a single PMOS pair without the Survivor circuit and the Survivor pair out of a bank of 16 pairs for 30 IC samples.

To verify if the foregoing Survivor scheme could viably replace the *trimming* process, the accuracies of the reference with and without the Survivor strategy were compared, wherein 4 trim bits were used in the latter to tune R_{15}. The two approaches achieved similar dc accuracy performance at -40°C, 25°C, and 125°C, respectively: 0.75%, 0.34%, and 0.71% with the Survivor strategy and 0.67%, 0.30%, and 0.61% without it, but with 4 bits of trim. The Survivor

scheme, as proposed, therefore circumvents the test-time and dedicated-pin (or pad) costs normally associated with pre- and post-package trimming of bandgap references.

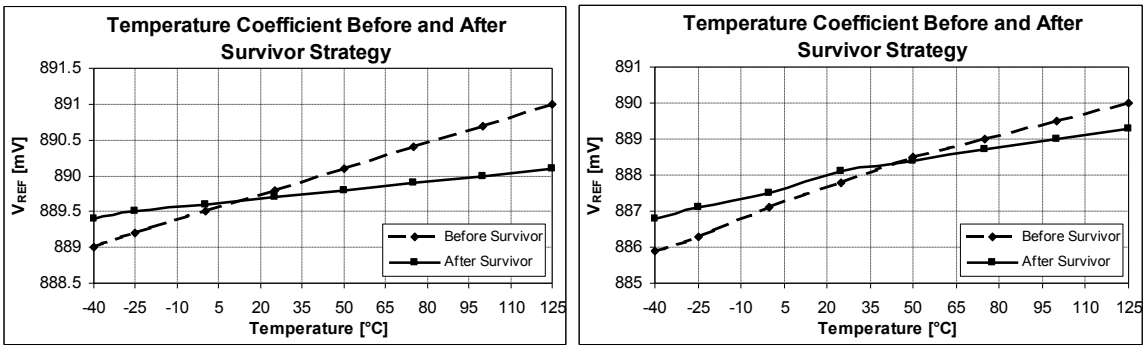


Fig. 13. Effect of Survivor strategy on the temperature coefficient (TC) of 2 die samples.

The techniques used in the proposed system –the Survivor strategy, charge-pumped cascode, and shunt-feedback regulation– all improve the dc and ac accuracy of the reference. The dc accuracy of the reference, in particular, is ultimately extrapolated as the linear sum of the initial 3-σ tolerance over process and temperature (ΔV_{TC}) and the average systematic load- and line-induced changes in the reference (ΔV_{LDR} and ΔV_{LDR}). The design produced an overall 3-σ, 0-5mA, 1.8-3V trimless accuracy of 2.74%:

$$\Delta V_{REF.DC-3\sigma} = \Delta V_{TC} + \Delta V_{LDR} + \Delta V_{LNR} = 14.9\text{mV} + 8\text{mV} + 1.5\text{mV} = 24.4\text{mV} \Rightarrow 2.74\%. \quad (12)$$

Another key feature of the design was its ability to reject supply ripple, i.e., ac line variations. The worst-case power-supply ripple-rejection (PSRR) performance of the proposed sub-bandgap reference was -30dB, which represents a 32dB improvement over its non-cascoded counterpart (Fig. 14). The crude reference presented a PSRR attenuation of -20dB at dc and the series RC filter a -3dB roll-off frequency of 20kHz to the supply and charge-pump output ripple. The low-frequency ripple that ultimately reached the gate of cascoding device MN_C, which was then impressed at its source, was attenuated by the loop gain of the shunt-feedback sub-bandgap reference, achieving an overall dc PSRR of approximately -70dB. At and past the unity-gain frequency of the reference, however, the loop gain is negligible, leaving the source-drain resistance of cascoding device MN_C ($r_{ds.MNc}$) the job of attenuating the supply ripple by -32dB, which constitutes the worst-case PSRR point (around 3.3MHz, which is the unity-gain of the reference). Beyond this point, the 10pF output capacitor presented a shunting pole, reducing the ripple at the output at 20dB per decade, as shown in the graph. In all, the PSRR performance shown was achieved with a combined on-chip capacitance of 60pF.

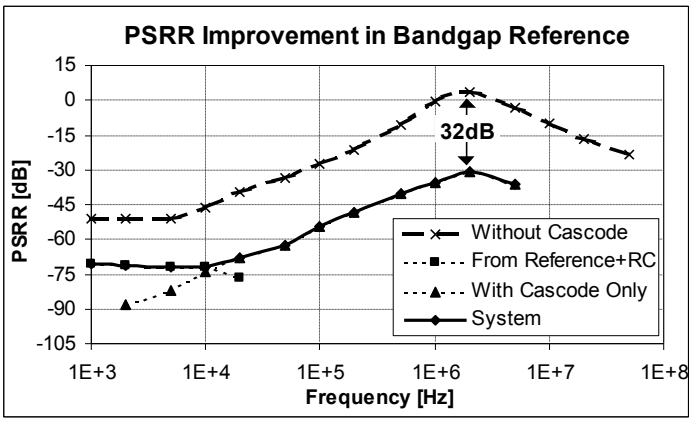


Fig. 14. Power-supply ripple-rejection (PSRR) performance with and without the charge-pumped NMOS cascode.

The start-up sequence of the complete system begins with an external RESET pulse, at the onset of which the low-impedance, sub-bandgap reference and cascoding circuit are disabled and the Survivor power-on-reset (PoR) sequence for choosing the NMOS and PMOS pairs begins. After the NMOS and PMOS survivor pairs are automatically determined, the chosen pairs are connected to the sub-bandgap reference and the DEM circuit and accompanying high-resolution comparator are disabled, at which point the reference is allowed to start. After a reset pulse, the system requires 15 comparisons to converge on the best matching pairs, taking 1.5ms for each comparison and a total of 22.5ms for the entire start-up time.

The combined initial accuracy (which refers to the 1-σ spread variation in the reference voltage at room temperature) and TC performance of the foregoing design (Table 2) is nearly twice (at 52ppm/°C) that presented in [21] (which was 24 ppm/°C), except the latter was achieved with 8 trim bits, the test-time costs of which are relatively severe. The proposed circuit achieved better initial accuracy than [14], and without the noise associated with the DEM used in [14]. [18] also used a cascoding scheme to improve PSRR, but their worst-case PSRR performance (-15dB) and associated dropout voltage (1.464V above output voltage 1.236V) were worse than in the proposed circuit (-30dB and 0.910V above output voltage 0.890V). Minimum supply voltage $V_{DD(min)}$ for the core sub-bandgap circuit at no load was 1.25V. However, the minimum supply for the entire circuit was 1.8V because it was designed to sustain a 5mA load. Had the load-current been reduced, the circuit could have been designed to sustain a $V_{DD(min)}$ of approximately 1.4-1.5V, which when comparing it against the state-of-the-art, would have been compatible with [14] and only been second to current-mode sub-bandgap topologies

like in [10], both of which suffer from relatively poor ac accuracy, that is, low PSRR and low coupled-noise-shunting capabilities.

In the 2.048V buffered bandgap reference of [22], low-power biasing resulted in a low gain-bandwidth product (80kHz), which when compared to the proposed scheme (3.3MHz), results in poorer ripple-noise immunity around the 50kHz-5MHz range. More importantly, however, the buffer used in [22] degrades the overall accuracy performance of the reference by introducing an additional error component (the input-referred offset of the buffer) that is normally non-linear with respect to temperature. Finally, though the BiCMOS topology in [25] used lateral PNP devices and shunt feedback to generate a first-order reference voltage, the topology is fundamentally constrained to considerably low reference voltage values because the feedback loop does not amplify the PTAT voltage (as in the proposed topology); in other words, the PTAT voltage can only compensate a small fraction of a base-emitter voltage. For instance, while the proposed topology generates a 890mV reference using lateral PNPs having a current density ratio of 8, the reference in [25] requires a ratio of roughly 1,500,000.

TABLE 2. PERFORMANCE COMPARISON AGAINST STATE-OF-THE-ART

("NA" INDICATES DATA NOT APPLICABLE AND "-" INDICATES DATA NOT AVAILABLE).

Parameter	Proposed Circuit	Degrauwe [21]	Ceekala [14]	Tham [18]	Doyle [10]	Manetakis [22]	Sanborn [25]
Strategies Used	a. Survivor b. Cascode c. Shunt Feedback	a. Trimming b. Shunt Feedback	DEM	Cascode	Trimming	Buffer	Shunt Feedback
CMOS Technology	0.6µm	4µm	0.18µm	0.9µm	0.5µm	0.35µm	0.5µm[5]
V_{REF} [V]	0.890	1.228	1.225	1.236	0.631	2.048[3]	0.191
Initial Accuracy @ 25°C [mV]	1	0.15[1]	3.5	-	0.5	$\sqrt{1.3^2+\sigma^2_{reference}}$ [4]	1
Box-Method TC [ppm/°C]	52	24[1]	-	-	-	-	-
Minimum Supply Voltage [V]	1.80	2.2	≈ 1.5[2]	2.7	0.95	2.5[3]	1[6]
PSRR @ 10kHz [dB]	-75	-30	-	-80	-	-37[3]	-
Worst-Case PSRR [dB]	-30	-	-	-15	-	-	-
Maximum load current [mA]	5	-	NA	NA	NA	±20[3]	-
Load Regulation [mV/mA]	1.570	3.6	NA	NA	NA	0.01[3]	-
Gain-Bandwidth of Loop [MHz]	3.30	-	NA	NA	NA	0.080[3]	-
Area [mm^2]	2.90	0.42	0.007	0.07	1.09	NA[3]	0.40
Total Power Consumption [mW]	0.35	0.17	6.00	1.0	0.01	0.08[3]	0.02

[1]8 trim bits, [2]$V_{REF}+V_{DS(sat)}$, [3]Simulation results, [4]1.3mV is the error introduced by the buffer, [5]BiCMOS, [6]$V_{REF}+V_{BE}+V_{DS(sat)}$.

V. Discussion on the Survivor Strategy

The number of devices (n) required in the bank of device pairs to achieve a specified mismatch performance (r), which, in turn, determines the accuracy of the bandgap reference, depends on the inherent offset of the pairs (R) and the specified probability of finding at least one pair in the bank with the desired matching performance (P). Assuming the inherent offset follows a normal distribution φ(x), the probability a pair within a sample has an offset lower than or equal to mismatch performance r is given by

$$p = \varphi\left(\frac{r}{R}\right) = \frac{1}{2}\,\mathrm{erf}\left(\frac{1}{\sqrt{2}}\cdot\frac{r}{R}\right). \tag{13}$$

As a result, the probability that *none* of the n devices within a sample has the required offset is $(1\text{-}p)^n$. If the probability of finding *at least one pair* from each sample within the desired resolution range is P,

$$P = 1-(1-p)^n \Rightarrow n = \frac{\log(1-P)}{\log(1-p)}. \tag{14}$$

For the current implementation, P was 0.9 and r/R was set to 0.1. In other words, the offset of the survivor pair was targeted to be 1/10 that of the intrinsic offset of the pairs in the bank. As seen from Eq. (14), increasing the desired accuracy of the survivor (i.e., decreasing its offset relative to that of the other pairs) necessarily implies more pairs in the bank. Increasing the probability of finding at least one pair with the desired offset performance (P) has a similar effect because more pairs in the bank are now required to *ensure* at least one pair meets the lower offset specification.

The primary trade-off of the Survivor strategy is silicon area. While the circuit improved the 3-σ matching performance of a 120/6 PMOS pair from 1.95% to 0.31% (6.3×), a bank of similar, yet unused pairs of devices were left on the silicon die. Assuming the offset performance is inversely proportional to the square root of the gate area [23], the resulting offset performance of the surviving 120/6 pair was equivalent to that of a 720/36 pair, which is $6.3^2\times$ or $40\times$ the gate area of a 120/6 pair. To put it in perspective, the bank of 16 120/6 pairs and the comparator and digital engine used in the survivor scheme required an area of 960,000μm^2 (Fig. 15) whereas the equivalent matching pair of 720/36 would have used 62,500μm^2, which means the survivor strategy used approximately $15\times$ the area of a 720/36 device. While a layout area of 960,000μm^2 may seem large, it is more reasonably compared against the number of fuses or EEPROM electronics used to trim a 120/6 device to yield the matching performance of a 720/36 transistor,

which is expected to yield similar tradeoffs as the Survivor strategy. Even if the proposed scheme demands more silicon real estate than trimming schemes, its resulting cost is arguably easier to absorb than the test-time costs associated with the increasingly dense CMOS ICs used to supply volume-intensive markets like the mobile business.

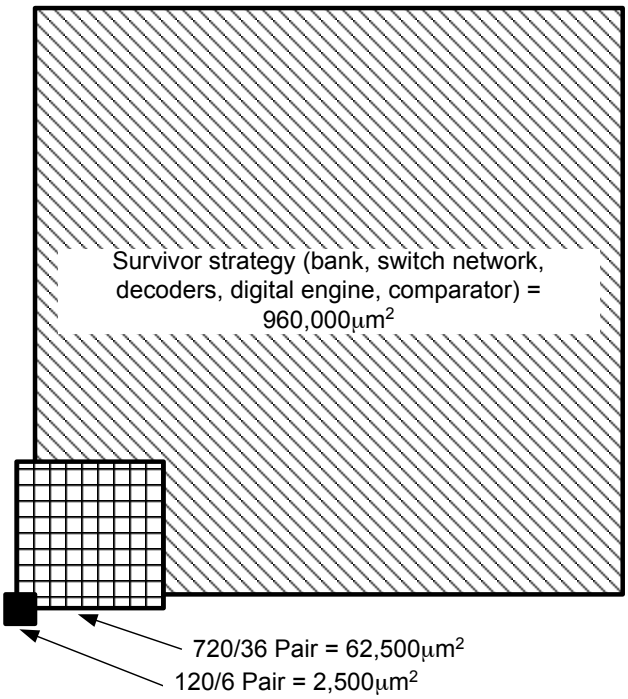
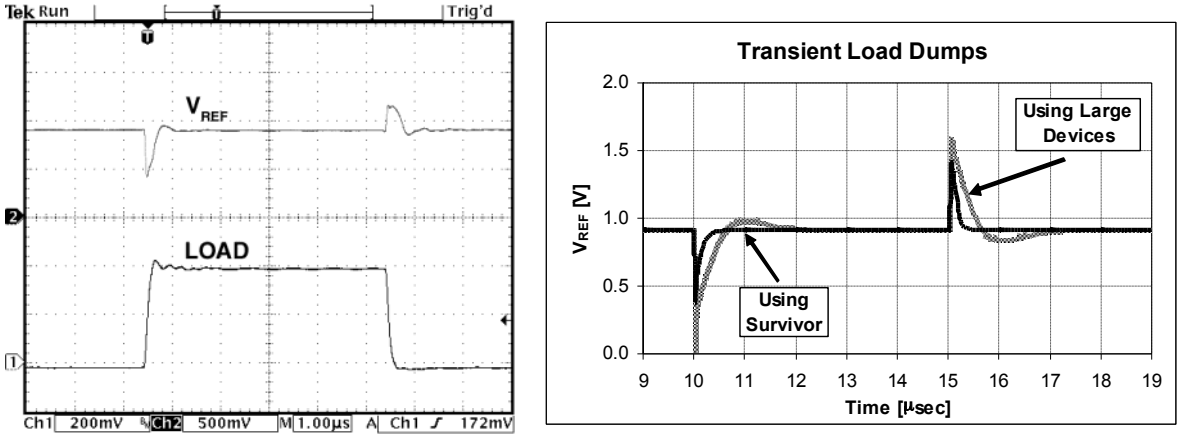


Fig. 15. Silicon-die area estimates for a 120/6 pair, Survivor circuit with 16 120/6 pairs, and a 720/36 pair whose offset performance matches that of the Survivor pair.

The main benefit of trimming and the Survivor strategy is, in the end, higher bandwidth. Increasing the size of a pair of devices from 120/6 to 720/36 to improve matching increases their respective gate-source capacitances by roughly $40\times$, reducing in the process their bandwidth by the same factor. The proposed Survivor scheme circumvents this tradeoff by selecting a 120/6 mirror that has the offset performance of its 720/36 counterpart, while not resorting to trim and therefore not increasing test time. Fig. 16(a) shows the measured load-dump response of the proposed reference for a 0-5mA load dump with 100ns rise and fall times whereas Fig. 16(b), to better ascertain the effects of the proposed strategy, shows that the simulated settling time of the same reference with the 120/6 PMOS and 60/6 NMOS surviving devices is four times faster than the circuit with their 720/36 PMOS and 360/36 NMOS equivalents. Further dedicating the entire $960{,}000\mu m^2$ area to a single critically matched pair not only incurs a prolonged response time but could also compromise the stability of the circuit, since these mirrors are normally non-dominant

poles in the feedback loop and adding this much capacitance may pull these poles to lower frequencies, near or below the unity-gain frequency of the reference.



(a) (b)

Fig. 16. (a) Measured transient-response performance of the proposed reference for a 0-5mA load dump and (b) a comparison of simulated response times using the smaller surviving pairs against their large-area equivalents.

VI. Conclusions

A 0-5mA, 890mV, low-impedance, sub-bandgap 0.6µm CMOS reference with a 3-σ trimless accuracy of 0.84% across -40°C to 125°C (2.74% when including 0-5mA load and 1.8-3V line effects) and a worst-case power-supply ripple rejection of -30dB for up to 50MHz was designed, fabricated, tested, and evaluated. The key features of the design were the Survivor scheme aimed at improving absolute dc accuracy and the charge-pumped cascode and integrated, sub-bandgap shunt-feedback architecture aimed at improving ac accuracy (i.e., rejecting supply noise and shunting coupled noise to ground). By automatically selecting best matching pairs during non-recurring start-up events, the Survivor-based reference achieves the 4-bit performance of trimmed references while circumventing the test-time costs associated with trimming and the switching noise associated with dynamic-element matching (DEM). By charge-pumping the gate of an NMOS and strategically filtering the noise present at its gate, the proposed cascode circuit improved worst-case ripple rejection by 32dB, which normally occurs around the unity-gain frequency of the reference (where the shunt-feedback benefits of the reference are non-existent) while only increasing the minimum supply voltage by a single $V_{DS(sat)}$. Ultimately, the minimum supply voltage of the entire circuit is limited to a PMOS threshold voltage and four $V_{DS(sat)}$'s,

which can be on the order of 1.2V, but was 1.8V mainly because of the unusually high PMOS threshold voltage of the technology used (0.9V) and the high load-current requirements (0-5mA) demanded of the circuit. The combined trimless dc and ac CMOS accuracy performance of the proposed low-impedance, sub-bandgap reference, in the end, meets the stringent performance requirements and low-cost (low test-time) demands of increasingly complex system-on-chip (SoC) solutions, with its tradeoff being silicon real estate, similar to the tradeoffs of trimming and EEPROM, except no test time is required.

ACKNOWLEDGEMENTS

The authors would like to thank Texas Instruments Inc. for its sponsorship of this research and Drs. Ramanathan Ramani and Wei-Chung Wu for their valuable advice and feedback.

REFERENCES

[1] W. Krenik, D. D. Buss, P. Rickert, "Cellular handset integration – SIP versus SOC," *IEEE Jour. of Solid-State Circuits*, vol. 40, pp. 1839-1846, Sept. 2005.

[2] C. Lee, K. McClellan, and J. Choma Jr., "A supply-noise-insensitive CMOS PLL with a voltage regulator using dc-dc capacitive converter," *IEEE Jour. of Solid-State Circuits*, vol. 36, pp. 1453-1463, Oct. 2001.

[3] P.E. Allen and D.R. Holberg, CMOS Analog Circuit Design, Oxford Univ. Press, 2002, ISBN: 0195116445.

[4] A. Bakker and J.H. Huijsing, "Micropower CMOS temperature sensor with digital output," *IEEE Jour. of Solid-State Circuits*, vol. 31, pp. 933-937, July 1996.

[5] G.A. Rincón-Mora, *Voltage References*. IEEE Press, John Wiley & Sons, Inc., 2002, ISBN: 0471143367.

[6] K.E. Kuijk, "A precision reference voltage source," *IEEE J. Solid-State Circuits*, vol. SC-6, pp. 2-7, June 1973.

[7] M. Gunawan, G. C. M. Meijer, J. Fonderie, and J. H. Huijsing, "A curvature-corrected low-voltage bandgap reference," *IEEE J. Solid-State Circuits*, vol. 28, pp. 667-670, June 1993.

[8] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference with sub-1-V operation," *IEEE J. Solid-State Circuits*, vol. 34, pp. 670-674, May 1999.

[9] K.N. Leung and P.K.T. Mok, "A sub-1V 15ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits*, vol. 37, pp. 526-530, April. 2002.

[10] J. Doyle, Y.J. Lee, Y. Kim, H. Wilsch, and F. Lombardi "A CMOS subbandgap reference circuit with 1-V power supply voltage," *IEEE J. Solid-State Circuits*, vol. 39, pp. 252-255, Jan. 2004.

[11] V. Gupta and G.A. Rincón-Mora, "Predicting the effects of error sources in bandgap reference circuits and evaluating their design implications," in *Proc. IEEE Midwest Symp. Circuits Systems,* Tulsa, 2002, pp. 575-578.

[12] A. Bakker and J.H. Huijsing, "A low-cost high-accuracy CMOS smart temperature sensor," in Proc. European Solid-State Circuits Conf., Duisburg, 1999, pp. 302-305.

[13] M.A.T. Sanduleanu, A.J.M. van Tuijl, and R.F. Wassenaar, "Accurate low power bandgap voltage reference in 0.5μm CMOS technology," *IEE Electronics Letters*, vol. 34, pp. 1025-1026, 14th May 1998.

[14] V.G. Ceekala, L.D. Lewicki, J.B. Wieser, D. Varadarajan, and J. Mohan, "A method for reducing the effects of random mismatch in CMOS bandgap references," in *Digest IEEE Intl. Solid-State Circuits Conf.*, vol. 2, pp. 318-319, 2002.

[15] A. Bakker, "CMOS smart temperature sensors – An overview," in *Proc. IEEE Sensors,* Orlando, FL, June 2002, pp. 1423-1427.

[16] F. Fruett, G.C.M. Meijer, and A. Bakker, "Minimization of the mechanical-stress-induced inaccuracy in bandgap voltage references," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1288-1291, July 2003.

[17] B. Abesinga, G.A. Rincón-Mora, and D. Briggs, "Voltage shift in plastic-packaged bandgap references," *IEEE Trans. Circuits Sys – II*, vol. 49, pp. 681-685, Oct. 2002.

[18] K. Tham and K. Nagaraj, "A low-voltage high PSRR voltage reference in CMOS process," *IEEE J. Solid-State Circuits*, vol. 5, pp. 586-590, May 1995.

[19] G. Giustolisi and G. Palumbo, "A detailed analysis of power-supply noise attenuation in bandgap voltage references," *IEEE Trans. Circuits Sys.- I*, vol. 50, pp. 185-197, Feb. 2003.

[20] D. Spady and V. Ivanov, "A CMOS bandgap voltage reference with absolute value and temperature drift trims," in *Proc. IEEE Intl. Symp. Circuits Systems*, pp. 3853-3856, 2005.

[21] M.G.R. Degrauwe, O.N. Leuthold, E.A. Vittoz, H.J. Oguey, and A. Descombes, "CMOS voltage references using lateral bipolar transistors," *IEEE J. Solid-State Circuits,* vol. 6, pp. 1151-1157, Dec. 1985.

[22] K. Manetakis, "CMOS micro-power output stage for integrated voltage references," *IEE* Electronics Letters, vol. 40, pp. 917-918, 22 July 2004.

[23] P. Gray, P. Hurst, S. Lewis, and R. Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley & Sons, ISBN: 0471321680.

[24] J. M. Ingino and V.R. von Kaenel, "A 4-GHz clock system for a high-performance system-on-a-chip design," IEEE J. of Solid-State Circuits, vol. 36, pp. 1693-1698, Nov. 2001.

[25] K. E. Sanborn, V. Ivanov, D. Ma, "A sub-1V low-noise bandgap voltage reference," in *Proc. IEEE Custom Integrated Circuits Conf.*, San Jose, CA, Sept. 2006, pp. 607-610.

[26] Linear Technology, Appl. Note 82, "Understanding and applying voltage references." [Online] Available: http://www.linear.com/pc/downloadDocument.do?navId=H0,C1,C1154,C1009,C1021,P1567,D4171.

[27] A.P. Brokaw, "A simple three-terminal IC bandgap reference", *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 388-393, Dec. 1974.

[28] V. Gupta and G. A. Rincón-Mora, "'Low output impedance 0.6µm-CMOS sub-bandgap reference," *IET Electronics Letters,* accepted for publication.

[29] V. Gupta and G. A. Rincón-Mora, "Achieving less than 2% 3-σ mismatch with minimum channel-length CMOS devices," *IEEE Trans. Circuits Sys.- II,* vol. 54, pp. 232-236, Mar. 2007.

[30] V. Gupta and G. A. Rincón-Mora, "A low dropout, CMOS regulator with high PSR over wideband frequencies," in *Proc. IEEE Intl. Symp. on Circuits and Systems*, vol. 5, pp. 4245-4248, May, 2005.

[31] V. Gupta and Rincón-Mora, "A 5mA 0.6µm CMOS Miller-compensated LDO regulator with -27db worst-case power-supply rejection using 60pf of on-chip capacitance," in *Digest IEEE Intl. Solid-State Circuits Conf.*, San Jose, CA, Feb. 2007, pp. 520-521.

[32] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE J. Solid-State Circuits,* vol. 3, pp. 365-373, Dec. 1968.

[33] J. M. Ingino, V.R. von Kaenel, "A 4-Ghz Clock System for a High-Performance System-on-a-Chip Design," *IEEE Jour. of Solid-State Circuits*, vol. 36, pp. 1693-1698, Nov. 2001.

[34] P. Favrat, P. Deval, M. J. Declercq, "A High-Efficiency CMOS Voltage Doubler," *IEEE Jour. of Solid-State Circuits*, vol. 33, pp. 410-416, March 1998.

[35] Wang G. and G. C. M. Meijer, "The temperature characteristics of bipolar transistors fabricated in CMOS technology," *Sensors and Actuators*, vol. 87, pp. 81-89.