A Non-Resonant Self-Synchronizing Inductively Coupled 0.18-µm CMOS Power Receiver and Charger

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Abstract: While the functionality of emerging wireless microsensors, cellular phones, and biomedical implants, to name a few, is on the rise, their dimensions continue to shrink. This is unfortunate because smaller batteries exhaust quicker. Not surprisingly, recharging batteries wirelessly is becoming increasingly popular today. Still, small pickup coils cannot harness much, so induced EMF voltages $v_{EMF.S}$ are low. Modern receivers can resonate these low input voltages to rectifiable levels, but only with a finely tuned capacitor that resonates at megahertz when on chip and at kilohertz when off chip. In other words, resonant rectifiers are sensitive to frequency and dissipate considerable switching power when integrated on chip. Unluckily, excluding the resonant capacitor requires a control signal that synchronizes switching events to the transmitter's operating frequency. The 0.18-µm CMOS prototype presented here derives this synchronizing signal from the coupled $v_{EMF.S}$ by counting the number of pulses of a higher-frequency clock across a half cycle during a calibration phase and using that number to forecast half-cycle crossings. This way, the prototyped IC switches every half cycle to draw up to 557 µW from 46.6–585-mV_{PK} signals with 38%–84% efficiency across 1.0–5.0 cm.

List of keywords: **Inductive power transmission, contactless charging, wireless power transfer, inductively coupled power, low-threshold rectifier, switched-inductor receiver.**

I. Inductively Powered Microsystems

Modern wireless microsystems incorporate sensors, analog and digital processors, and radio-frequency transceivers to satisfy the functional demands of emerging wireless sensor networks [1] and biomedical implants [2]. Unfortunately, the power needed to sense, transmit, receive, and process signals still outpaces power reductions won by the state of the art [3], so microsensors still require more power and energy than tiny batteries can supply [4]. In other words, either the operational life of these devices is short or their functionality is low. Luckily, coupling inductive power wirelessly can supply sufficient power to operate a microsensor [5]−[9] and replenish its onboard battery [10]−[12]. This means that a microsystem, like the one in Fig. 1, can operate on its own between recharge cycles, and as a result, enjoy the benefits of extended operational life.

Volumetric constraints also limit the size of the pickup coil. This means the receiver captures a small fraction of the magnetic flux available and produces a correspondingly low electromotive-force (EMF) voltage $v_{EMF.S}$ [13]. This low EMF voltage is the reason why state-of-the-art rectifiers use resonance to boost voltages to rectifiable levels [14]−[17]. When using a tuned capacitor for this purpose, however, the circuit is more sensitive to frequency. And when on chip, this frequency and its related switching power losses are high. The non-resonant receiver presented here excludes this capacitor and its shortcomings [18]–[19], and derives a synchronizing signal from its incoming signal to orchestrate switching events. To comprehend the benefits and limitations of this technology, Section II describes how resonant and non-resonant power receivers operate. Section III then discusses how the prototyped non-resonant system generates its synchronizing signal and Section IV quantifies how much power it transfers. Sections V and VI describe the IC implementation of the prototype and results measured. In the end, Section VII draws relevant conclusions.

II. The State of the Art

A. Resonant Receivers

Bridge-based resonant receivers use a resonating capacitor C_R like Fig. 2 shows to boost low input voltages to rectifiable levels [14]−[17]. This way, when the resonant frequency f_{LC} of C_R and the pickup coil's inductance L_S matches the frequency of the transmitted signal f_O, C_R receives and returns energy from and to L_S in alternating quarter cycles. As a result, the magnitude of C_R's voltage $|v_C|$ grows across time until v_C's positive and negative half cycles in Fig. 3 reaches two diodes above the receiving battery C_{BAT}: $2v_D + v_{BAT}$. Once this happens, C_R stores enough energy to raise v_C to $2v_D + v_{BAT}$ within a half cycle, so the diodes conduct all incoming positive and negative half-cycle charge from L_S into C_{BAT}. To reduce the voltage dropped across the diodes to millivolts, state-of-the-art implementations configure synchronous MOSFET switches to operate like diodes [21]–[23].

One drawback to this approach is that output power drops drastically when f_O deviates from f_{LC} [20]. Tuning f_{LC} to f_O by adjusting C_R dynamically with a slow feedback loop can overcome this deficiency [24]. But since 200–500-pF capacitors typically resonate with L_S at 7–14 MHz [21]–[23], receivers with C_R on chip operate at high frequency. This means that the gate-drive energy lost to charging and discharging the gates of diode-emulating MOSFETs can be substantial at 7–14 MHz, when C_R is on chip, especially when considering tiny coils generate little power. Raising C_R to nanofarads reduces this frequency and its related losses, but only at the expense of an off-chip capacitor and additional board space. Still, this technology is popular because it does not require a synchronizing signal and it transfers power even when the battery is empty.

B. Non-Resonant Receivers

The non-resonant receiver in Fig. 4 uses switches S_N^+ and S_N^- to short the pickup coil's L_S across each half cycle and therefore impress the induced EMF voltage $v_{EMF.S}$ across L_S. This way, L_S energizes from $v_{EMF.S}$ across each half cycle, which means L_S's current i_L in Fig. 5 climbs up across $v_{EMF.S}$'s positive half cycle and down across $v_{EMF.S}$'s negative half cycle. S_N^+ opens and S_P^+ closes near the end of the positive half cycle to steer i_L into C_{BAT}. Since a current flowing out of a voltage source constitutes power delivered, synchronizing switching events amounts to ensuring L_S's current i_L in Figs. 4 and 5 is positive when $v_{EMF.S}$ is positive. So depleting L_S and ensuring i_L reaches zero at $v_{EMF.S}$'s half-cycle crossing is optimal. S_P^+ can open after that [19] or remain closed for another brief period to draw some energy from C_{BAT} [20]. This investment from C_{BAT}, which raises i_L in the negative direction, boosts the electromagnetic damping force with which L_S draws energy from the magnetic flux present [20]. After this, S_N^+ again closes.

Similarly, S_N^- opens and S_P^- closes near the end of the negative half cycle to steer i_L, which now flows in the opposite direction, into C_{BAT}. S_P^- can open when i_L is zero [19] or remain closed for another brief period to draw an energy investment from C_{BAT} [20] that boosts the damping force in L_S. Note that, although depleting L_S into C_{BAT} requires time (part of τ_{BAT}^+ and τ_{BAT}^- in Fig. 5), $v_{EMF.S}$ still supplies charge to L_S and C_{BAT} during that time. In other words, the system draws power from $v_{EMF.S}$ across the entire period.

The main advantage with this approach is the absence of a resonating capacitor. Without C_R, the system is less sensitive to frequency and more compact. And switching losses are lower when fully integrated on chip because the operating frequency f_O is low at 125 kHz. Although raising f_O is possible, switching gate-drive losses can rise to such an extent that they can overwhelm the little power that a tiny pickup coil generates. The challenge here is synchronizing the switching events to $v_{EMF.S}$'s half-cycle crossings.

III. Self-Synchronizing Non-Resonant Power Receiver and Charger

Since i_L should be positive when $v_{EMF.S}$ is positive, L_S should begin draining before $v_{EMF.S}$ transitions between half cycles, as Fig. 5 illustrates, and i_L should reach zero at half-cycle crossings. For this, the system must determine the state of $v_{EMF.S}$, except neither $v_{EMF.S}$ nor the transmitter current i_P in Fig. 1 that sets $v_{EMF.S}$ are accessible. The system therefore disconnects L_S, which interrupts the power-transfer process, for one and a half periods to sense and program $v_{EMF.S}$'s transition points for subsequent cycles.

A. Calibration

During calibration, the system senses the beginning of $v_{EMF.S}$'s period T_O and counts how many clock pulses appear across v_{EMF}'s half cycle. For this, all switches in Fig. 4 except S_N^-, which corresponds to M_N^- in the calibration circuit of Fig. 6, open and M_{SEN}^+ and M_{SEN}^- connect L_S across R_{SEN}, whose impedance is much higher than that of L_S at $v_{EMF.S}$'s operating frequency f_O. This way, $v_{EMF.S}$ appears across R_{SEN}, as the switching nodes v_{SW}^+ and v_{SW}^- in Fig. 7 show at 0–11 and 71–82 μs, and CP_{SEN} in Fig. 6 compares $v_{EMF.S}$ against zero to generate a digital output v_{SEN} that is in phase with $v_{EMF.S}$. CNT_{PRED} then starts counting f_{CLK} pulses after v_{SEN}'s first rising transition and stops after v_{SEN} rises again, at which point register REG_{PRED} stores the count.

B. Synchronization

At the end of calibration, when $v_{EMF.S}$ enters its positive half cycle, M_{SEN}^+ and M_{SEN}^- open and CNT_{PRED} resets to start energizing L_S from $v_{EMF.S}$, as Fig. 7 shows at 11 and 82 μs. When the high-if-equal logic in the synchronizer of Fig. 8 determines that CNT_{PRED} reaches nearly half REG_{PRED}'s recorded count, CNT_{PRED} resets and v_{SYNC} commands L_S to drain into C_{BAT}. After that, L_S energizes from $v_{EMF.S}$ across the negative half cycle until CNT_{PRED} again reaches nearly half REG_{PRED}'s recorded count. Another half-cycle sequence then begins and the process repeats.

Since L_S should start draining before the onset of another half cycle to ensure i_L is in phase with $v_{EMF.S}$, the subtractor in Fig. 8 uses Phase Correct, which is an off-chip digital word that is programmable, to subtract $0.5\tau_{BAT}$ counts from the first half-cycle count. This means τ_{SHORT} is short of $0.5T_O$ by $0.5\tau_{BAT}$, where part of τ_{BAT} is the time that L_S requires to deplete. As a result, L_S empties near $v_{EMF.S}$'s half-cycle crossings, and in the case of Fig. 7, receives investment energy from C_{BAT} immediately after that, as τ_{BAT} ends. S_P^+ (or S_P^-) in Fig. 4 then opens and S_N^+ (or S_N^-) closes to energize L_S from $v_{EMF.S}$ alone. Note that L_S receives EMF energy as long as i_L is nonzero and in phase with $v_{EMF.S}$, across every half cycle. The purpose of the 0.5-bit correction is to add a bit every other half cycle when the stored count in REG_{PRED} is odd. This way, the 0.5-bit error that results toggles about half of REG_{PRED}'s recorded count and never grows.

C. Recalibration

Since the internal clock f_{CLK} has no relation to $v_{EMF.S}$'s f_O, T_O's half cycle normally does not fit an exact integer number of f_{CLK} periods. As a result, the system does not drain L_S into C_{BAT} exactly at the half-cycle crossings. Whether under or over forecasted, the synchronizer introduces a quantization error τ_E with every half cycle that compounds over time t to shift v_{SYNC} more and more out of phase with respect to $v_{EMF.S}$. This is why the compounded time and phase shifts $\Delta\tau$ and $\Delta\theta$ grow with t in Fig. 9, and v_{SYNC} is slow when τ_E is positive and fast otherwise:

$$\Delta\theta = \omega_O \Delta\tau = 2\pi f_O \left(\frac{\tau_E}{T_O}\right) t, \tag{1}$$

where ω_O is f_O in radians per second and t starts when calibration ends. Since the error should not be such that drawing energy from $v_{EMF.S}$ is impracticable, the system recalibrates after CNT_{RECAL} in Fig. 8 counts N_{PRED} number of f_O periods, which in the case of Fig. 7 is 7 periods. And since CNT_{RECAL}'s v_{RECAL} does not usually align exactly with a half-cycle crossing, v_{RECAL} reconfigures

S_P^+ in Fig. 4 to drain L_S like a diode. This way, L_S depletes and does not receive investment energy from C_{BAT} before a recalibration, as i_L in Fig. 7 shows at 70 μs when i_L falls to zero.

IV. Power Transfer

A. Uncollected Energy

When perfectly in phase, $v_{EMF.S}$ supplies i_L at f_O to source EMF energy per cycle $E_{EMF.S}^*$:

$$E_{EMF.S}^* = \int_0^{T_O} P_{EMF.S}\, dt = \int_0^{T_O} v_{EMF.S} i_L\, dt, \tag{2}$$

where * refers to perfect in-phase conditions. When out of phase by $\Delta\theta_i$, however, $v_{EMF.S}$ supplies a cosine fraction of $E_{EMF.S}^*$:

$$E_{EMF.S(i)} = E_{EMF.S}^* \cos\left(\Delta\theta_i\right). \tag{3}$$

So since v_{SYNC} is more out of phase with $v_{EMF.S}$ after each period, $E_{EMF.S(i)}$ falls after each period to accumulate E_{TOT} in N_{PER} periods between calibration cycles:

$$E_{TOT} = \sum_{i=1}^{N_{PER}} E_{EMF.S(i)} = E_{EMF.S}^* \left[\sum_{i=1}^{N_{PER}} \cos\left(\Delta\theta_i\right)\right]. \tag{4}$$

In other words, phase shift causes a loss E_{PH} between calibration cycles that is equivalent to

$$E_{PH} = N_{PER} E_{EMF.S}^* - E_{TOT} = E_{EMF.S}^* \left[N_{PER} - \sum_{i=1}^{N_{PER}} \cos\left(\Delta\theta_i\right)\right]. \tag{5}$$

The EMF energy that the system ceases to draw during a calibration cycle is unfortunately another loss E_{CAL}. Because the calibration cycle begins at the end of a positive half cycle and the system counts across one full cycle starting with a positive half cycle, E_{CAL} is roughly $1.5E_{EMF.S}^*$.

Together, unharnessed power in Fig. 10 first falls when the number of periods between calibrations N_{PER} rises because the fraction of uncollected energy E_{CAL} to output energy $E_{EMF.S}^*$ drops with more energy-collecting periods between calibrations. This trend reverses when a rise in compounded phase-shift losses E_{PH} outpaces reductions in calibration losses E_{CAL}, after which point recalibrations help. This is why E_{PH} and E_{CAL} are at their combined minimum with 7

periods between calibration cycles when f_{CLK} is 5 MHz. And because a higher sampling frequency reduces phase-shift error, E_{PH} does not surpass E_{CAL} until after 16 periods at 14 MHz.

B. Consumed Power

Since series resistances consume power, the system loses ohmic conduction power P_C to S_N^+, S_N^-, S_P^+, S_P^-, and the parasitic series resistance R_S of the pickup coil. R_S therefore loses $i_{L(RMS)}^2 R_S$ across entire half cycles, S_N^+ and S_N^-'s combined resistance $2R_N$ loses $i_{L.SHORT(RMS)}^2 (2R_N)$ across τ_{SHORT}, S_N^-–S_N^+ and S_P^+–S_P^-'s R_N and R_P lose $i_{L.BAT(RMS)}^2 (R_N + R_P)$ across τ_{BAT}, and S_P^+'s diode voltage v_D lose $i_{L.DIODE(AVG)} v_D$ just before every calibration cycle:

$$P_C = i_{L(RMS)}^2 R_S + i_{L.SHORT(RMS)}^2 (2R_N) + i_{L.BAT(RMS)}^2 (R_N + R_P) + i_{L.DIODE(AVG)} v_D . \tag{6}$$

Charging the combined gate capacitances C_G of the MOSFETs that comprise the switches also demands energy, so the battery loses gate-drive power P_G to charge C_G to v_{BAT} every period T_O, but only for N_{PER} of every $1.5 + N_{PER}$ cycles:

$$P_G = \left(\frac{E_G}{T_O}\right)\left(\frac{N_{PER}}{1.5 + N_{PER}}\right) = \left(\frac{Q_C v_{BAT}}{T_O}\right)\left(\frac{N_{PER}}{1.5 + N_{PER}}\right) = C_G v_{BAT}^2 f_O \left(\frac{N_{PER}}{1.5 + N_{PER}}\right). \tag{7}$$

Similarly, digital circuits and the oscillator draw gate-drive power P_{DIG} more frequently at f_{CLK} from the battery to charge capacitances. C_{OSC} in a relaxation oscillator, for example, charges across Δv_{OSC} and combined parasitic gate capacitance C_{DIG} charges across v_{BAT} to draw

$$P_{DIG} = (Q_{OSC} + Q_{DIG}) v_{BAT} f_{CLK} = (C_{OSC} \Delta v_{OSC} v_{BAT} + C_{DIG} v_{BAT}^2) f_{CLK} . \tag{8}$$

The controller also requires power P_{CNTRL} to operate. The blocks that operate continuously, for one, dissipate quiescent power P_Q. The timer circuit that defines τ_{BAT}, however, only engages across two τ_{BAT}'s of T_O, so it consumes $2\tau_{BAT}/T_O$ of the power P_{TMR} that it draws when it is on. The calibration circuit similarly operates 1.5 of $1.5 + N_{PER}$ periods, so the system loses a fraction of the calibration power P_{CLBRT} it requires. So overall, P_{CNTRL} is

$$P_{CNTRL} = P_Q + P_{TMR}\left(\frac{2\tau_{BAT}}{T_O}\right) + P_{CLBRT}\left(\frac{1.5}{1.5 + N_{PER}}\right). \tag{9}$$

But since f_{CLK} is so high, P_{DIG} overwhelms P_G and P_{CNTRL}, and P_{DIG} and P_C therefore dominate.

V. Integrated Circuit

The receiver in Fig. 11 uses v_{SYNC} from Fig. 8 to control when to switch the pickup coil and steer L_S's charge into the battery C_{BAT}. When enabled by v_{RECAL}, and v_{SYNC} is high, which corresponds to $v_{EMF.S}$'s positive half cycle, M_N^+ and M_N^- close to energize L_S from $v_{EMF.S}$, which is why L_S's current i_L in Fig. 7 rises across 11–14 μs. When v_{SYNC} falls, M_N^+ opens, and after comparator $CP_{ZVS.P}^+$ senses v_{SW}^+ surpasses v_{BAT}, M_P^+ closes to drain L_S into C_{BAT}. M_P^+ does not open until after a tunable delay τ_{BAT}, across which L_S drains and then draws energy from C_{BAT} to lower and reverse i_L at 15 μs, which raises L_S's damping force to derive more power from $v_{EMF.S}$ [18]–[19].

After M_P^+ opens, comparator $CP_{ZVS.N}^+$ closes M_N^+ when v_{SW}^+ drops below zero. From this point, L_S energizes across $v_{EMF.S}$'s negative half cycle from a negative $v_{EMF.S}$. When v_{SYNC} rises, just prior to $v_{EMF.S}$'s transition to its positive half cycle, M_N^- opens, and after comparator $CP_{ZVS.P}^-$ senses v_{SW}^- exceeds v_{BAT}, M_P^- closes to drain L_S into C_{BAT}. Like in the positive half cycle, M_P^- does not open until after a tunable delay τ_{BAT}, across which L_S first drains and then draws energy from C_{BAT}. After, comparator $CP_{ZVS.N}^-$ closes M_N^- when v_{SW}^- drops below zero to complete the cycle. The sequence then repeats until the system recalibrates.

Note that all switching events in Fig. 5 occur when L_S's i_L is nonzero. So when any of the power switches open, i_L automatically raises or lowers v_{SW}^+ or v_{SW}^- until $CP_{ZVS.N}^+$, $CP_{ZVS.N}^-$, $CP_{ZVS.P}^+$, or $CP_{ZVS.P}^-$ engages a switch. In other words, the comparators close M_N^+, M_N^-, M_P^+, and M_P^- only when their drain–source voltages v_{DS} are nearly zero. This means the MOSFETs do not dissipate I–V-overlap power when v_{SW}^+ and v_{SW}^- transition, when v_{DS}'s are high.

A. Zero-Volt Comparators

Since $CP_{ZVS.P}^{+}$ and $CP_{ZVS.P}^{-}$ compare v_{SW}^{+} and v_{SW}^{-} with v_{BAT}, PFET M_{GC2} in Fig. 12a balances M_{GC1}'s mirrored gate-coupled counterpart when v_{SW} is at v_{BAT}. But since M_{MIR3} steers an offset current only when v_{SW} is below v_{BAT}, the output $v_{ZVS(H)}$ rises when v_{SW} climbs over v_{BAT} and drops when v_{SW} crosses v_{BAT} on its way down. $v_{ZVS(H)}$ rises within 10 ns in Fig. 13 to engage and steer some of i_L through M_P^{+} or M_P^{-} because i_L supplies M_{GC2} considerably more current than M_{GC1}'s 50 nA. M_{GC2} in Fig. 12b similarly raises $v_{ZVS(L)}$ in 10 ns when v_{SW} falls below 0 V.

B. EMF Sense Comparator

Since the voltage across R_{SENSE} in the calibration circuit of Fig. 6 is low and near 0 V, gate-coupled NMOS pair M_{GC1} and M_{GC2} senses when v_{SW}^{+} and v_{SW}^{-} crisscross. The differential output, whose gain R_{DIFF1}–R_{DIFF2} limits, then drives an NMOS differential pair with a latching PMOS load mirror that accelerates its response. M_{HYST} sinks an offset current when sensing a positive to negative transition in $v_{EMF.S}$ to keep noise voltage in $v_{EMF.S}$ from producing jitter in the output v_{DEC}. To save power, v_{CAL} and v_{SEN} disconnect and disable the circuit between calibrations. When calibration begins, v_{CAL} rises to establish a bias voltage across M_{BI3} and connect R_{SENSE} across v_{SW}^{+} and v_{SW}^{-}. And after all other connections settle and R_{SENSE} consumes all remnant energy in the parasitic capacitances at v_{SW}^{+} and v_{SW}^{-}, v_{SEN} rises to connect R_{SENSE} across M_{GC1}–M_{GC2}'s sources. Then while sensing, C_{FILT} filters high-frequency noise.

C. Relaxation Oscillator

When v_{OSC} is high in Fig. 15, M_{CC1} shuts and the latching PMOS load feeds M_{CC2} two bias currents $2I_{OSC}$ to discharge C_{OSC} with I_{OSC}. v_{OSC} therefore falls across Δv_{OSC} until M_{L1}–M_{L2}'s source–gate voltage v_{SGL} is high enough to engage M_{L2}, after which M_{CC1}'s gate rises, M_{L4} shuts, and M_{CC2}'s gate drops. As a result, M_{CC2} shuts and the latching PMOS load steers $2I_{OSC}$ into

M_{CC1} to raise v_{OSC} until M_{L4}–M_{L3}'s v_{SGL} is again high enough to engage M_{CC2} and shut M_{CC1}. To swing each terminal across v_{SGL}, v_{OSC} swings $2v_{SGL}$ in alternating cycles:

$$\Delta v_{OSC} = 2v_{SGL} = \frac{I_{OSC}}{C_{OSC}}\left(\frac{T_{CLK}}{2}\right). \tag{10}$$

M_{PP1} and M_{PP2} then fold and compare the latching currents to generate a digital signal that a high-threshold inverter buffers for gain and sharper clock edges. The oscillating period T_{CLK} that results in the output v_{CLK} establishes the system's clock f_{CLK} to

$$f_{CLK} = \frac{1}{T_{CLK}} = \frac{I_{OSC}}{4v_{SGL}C_{OSC}}. \tag{11}$$

D. Delay Timer

A rise in v_{TMR} starts τ_{BAT} and opens M_{DIS} in Fig. 16a to allow M_{CHG}'s bias current I_{CHG} to charge C_{RAMP}. When C_{RAMP}'s v_{RAMP} rises above V_{REF}'s 0.8 V, comparator CP_{TMR} stops τ_{BAT} and closes M_{DIS} to reset v_{RAMP} to 0 V. τ_{BAT} is therefore the time that I_{CHG} requires to raise v_{RAMP} to V_{REF}:

$$\tau_{BAT} = \frac{C_{RAMP}V_{REF}}{I_{CHG}} = \frac{C_{RAMP}V_{REF}}{16I_{EXT}}, \tag{12}$$

where I_{CHG} is $16I_{EXT}$ and I_{EXT} and V_{REF} are off chip for testability purposes. This way, τ_{BAT} is 70 ns to 1.8 μs when I_{EXT} is 30 nA to 1 μA. The purpose of M_{PASS} is to keep M_{CHG} from conducting and dissipating power when the circuit is off.

For this functionality, CP_{TMR}'s M_{NIN-}–M_{PIN-} and M_{NIN+}–M_{PIN+} in Fig. 16b compare v_{RAMP} and V_{REF}. M_{OUT} then buffers M_{NIN-}–M_{PIN-}'s output to pull CP_{TMR}'s v_{OUT} to 0 V quickly. M_{NIN-}–M_{PIN-} sinks a current that is much greater than the circuit's bias current when v_{RAMP} rises above V_{REF} to accelerate the transition. And M_{HYS} sinks an offset current when CP_{TMR}'s v_{OUT} is high, after the circuit resets, to establish a hysteresis that reduces output jitter.

VI. Prototype

An off-chip 300-nF SMD ceramic capacitor C_{BAT}, off-chip 400-μH 2.6 × 3.5 × 11.7-mm^3 Coilcraft 4513TC pickup coil, and 0.18-μm 510 × 510-μm^2 receiver in Fig. 17 implement the battery and power receiver described in Sections III–V. Although larger pickup coils harness more electromagnetic energy, microsensors cannot accommodate large devices. So under given space constraints, the coil with the least series resistance (i.e., highest quality factor) dissipates the least power. And because transferring energy requires time, the coil's inductance should be low enough to draw the investment energy required from the battery within a half cycle. The pickup coil's equivalent series resistance (ESR) is 9.66 Ω with a quality factor of 29 at 125 kHz, which is the system's operating frequency f_O. Transmission distance d_C and the coil voltage that d_C induces as $v_{EMF.S}$ are adjustable. Since C_{BAT}'s 300 nF invests and receives power across discrete 0.5–1.5-μs τ_{BAT} intervals in Fig. 5, v_{BAT} incorporates a ripple that, in addition to C_{BAT}'s steady-state charge rate, is roughly 5–25 mV when the coils are 10 to 50 mm apart.

A. Output Power and Power-Conversion Efficiency

Since phase-shift and calibration losses P_{PS} and P_{CAL} subtract power from what $v_{EMF.S}$ can ultimately source as $P_{EMF.S}^*$, the system receives $P_{EMF.S}^* - P_{PS} - P_{CAL}$ as EMF power $P_{EMF.S}$. Conduction, gate-drive, digital, and quiescent losses in the circuit then subtract power from $P_{EMF.S}$ to leave $P_{EMF.S} - P_C - P_G - P_{DIG} - P_Q$ for C_{BAT}. Power-conversion efficiency η_R is therefore the fraction of $P_{EMF.S}$ that reaches C_{BAT} as P_{BAT}:

$$\eta_R \equiv \frac{P_O}{P_{IN}} = \frac{P_{BAT}}{P_{EMF.S}} = \frac{\left(P_{EMF.S}^* - P_{PS} - P_{CAL}\right) - P_C - P_G - P_{DIG} - P_Q}{P_{EMF.S}^* - P_{PS} - P_{CAL}}. \tag{13}$$

In this light, with 10 mm of separation d_C between the transmitting and receiving coils L_P and L_S in Fig. 1, the prototyped system draws energy from an induced 585-mV$_{PK}$ $v_{EMF.S}$ to output 560 μW into C_{BAT} as P_{BAT}, as Fig. 18 demonstrates. P_{BAT} is not higher because small coils

capture a small fraction of the emanating electromagnetic field and the system loses phase-shift, calibration, conduction, gate-drive, digital, and quiescent power. Of the power drawn from C_{BAT} and L_S, the fraction that C_{BAT} gains above what C_{BAT} supplies is 84% at 10 mm, as η_R shows.

Since coils harness less energy when farther apart from their emanating source, $v_{EMF.S}$'s peak–peak voltage falls as d_C increases, and as a result, so does P_{BAT}. In other words, power-transmission efficiency across the transponder, between the transmitting and receiving coils, falls when d_C rises. Receiver efficiency, however, η_R is fairly even at 70%–84% within 30 mm and only down to 67% at 40 mm because ESR and MOS conduction losses $P_{C(ESR)}$ and $P_{C(MOS)}$ dominate and scale with P_{BAT}. Beyond 40 mm, 7.8 μW of quiescent and f_O- and f_{CLK}-switched losses in P_G, P_{DIG}, and P_Q, which do not scale with P_{BAT}, dominate, so losses become a greater fraction of P_{BAT} and η_R drops more rapidly. At 50 mm and 66 mV_{PK} of $v_{EMF.S}$, P_{BAT} and η_R therefore fall to 16 μW and 38%. In this region, P_{BAT} peaks when τ_{BAT} is 1.8 μs, and falls when extending τ_{BAT} beyond 1.8 μs because investing more energy from C_{BAT} dissipates more power than it generates [19], [25]−[26].

For a given transmitted power, coil separation, and corresponding coupling factor, EMF power $P_{EMF.S}$ delivers maximum output power P_O when P_O matches ohmic losses in the pickup coil's equivalent series resistance $P_{C(ESR)}$ and conducting MOS switches $P_{C(MOS)}$. In this sense, P_O represents the loss of a resistance R_O whose value matches that of R_S, M_N^+, M_N^-, M_P^+, and M_P^- combined when P_O is at its maximum power point. But since $P_{EMF.S}$ also supplies gate-drive, digital, and quiescent losses, P_O is P_{BAT} plus all these losses. In Fig. 18, P_O is nearly P_{BAT} and matches $P_{C(ESR)}$ and $P_{C(MOS)}$ when the coils are roughly 36 mm apart, so P_{BAT} is as high as possible at this point. This, however, does not mean the transmitter delivers as much power as possible, because reflecting P_O, $P_{C(ESR)}$, and $P_{C(MOS)}$ back to the transmitter does not necessarily

match conduction losses in the transmitter $P_{C(T)}$. This is why P_O climbs with proximity in Fig. 18, because reflected load power in the transmitter rises, but never reaches or surpasses $P_{C(T)}$. In other words, P_{BAT} peaks when losses are low and the transmitter's reflected load matches $P_{C(T)}$, which is when the receiver optimally damps the transmitting source [18].

B. Calibration Frequency

Interestingly, reducing the frequency of calibrations, which amounts to counting more $v_{EMF.S}$ periods before recalibrating, raises P_{BAT}, at least initially, as Fig. 19 shows. The reason for this rise in P_{BAT} is the power that the system does not harness during a calibration phase is greater than the power lost to phase-shift error. With more $v_{EMF.S}$ periods between calibrations and a 9.2-MHz clock, P_{BAT} eventually flattens and ultimately peaks, past which point phase-shift error dominates. P_{BAT} does not peak with a 14-MHz clock because the programmable range of N_{PRED}, which is the number of $v_{EMF.S}$ periods between calibrations, tops at fifteen, below the threshold above which phase-shift error dominates when f_{CLK} is 14 MHz.

P_{BAT} also falls when f_{CLK} rises from 9.2 to 14 MHz. This reduction results because a faster clock consumes more power and a higher sampling rate raises f_{CLK}-switched losses P_{DIG} from 6.2 to 9.9 μW. So in spite of a lower phase-shift error, the system draws more additional power from C_{BAT} at 14 MHz than from $v_{EMF.S}$ to net a lower gain. In other words, power lost to phase-shift error is not as limiting as f_{CLK}-switched losses are, so a slower clock is better. This is why maximum transmission distance $d_{C(MAX)}$ in Fig. 20 peaks at 7 cm when f_{CLK} is 5.25 MHz. Note that $d_{C(MAX)}$ is the distance above which the system cannot output power, so $d_{C(MAX)}$ corresponds to the minimum EMF voltage $v_{EMF.S(MIN)}$ below which P_{BAT} is negative.

C. Operating Frequency

With a ±20% variation in $v_{EMF.S}$'s operating frequency f_O about 125 kHz, the minimum EMF

voltage $v_{EMF.S(MIN)}$ rises 33% in Fig. 21. Although the percentage drop seems significant, the resulting 15-mV deviation is small. This is because the synchronizer calibrates and adjusts to f_O. For perspective, consider that this adaptability is absent in resonant receivers, where a ±20% mismatch between operating and resonating frequencies results in a 530-mV variation in $v_{EMF.S(MIN)}$ [20].

D. Relative Performance

One fundamental advantage of the non-resonant receiver presented here and in [19]–[20] is that it can operate at kilohertz without off-chip capacitors, whereas resonant receivers with up to 514 pF operate at 7–14 MHz [21]–[23], as Table I shows. This means that switching losses are lower and output power is therefore higher when constrained to on-chip integration. Another benefit is frequency insensitivity, because mismatches in [25]–[26] reduces output power P_{BAT} by considerably more than the same variation would here. Another attribute is the ability to invest battery energy, and with it, raise the electrical damping force with which a small pickup coil can draw power. Note that the difference between [19] and [20] is the ability to invest battery energy and between [20] and this work the ability to synchronize to $v_{EMF.S}$. Ultimately, the drawback here is complexity, because controllers and synchronizers are not necessary in resonant receivers.

VII. Conclusions

With 38%–84% power-conversion efficiencies across 1.0–5.0 cm, the 0.18-μm CMOS power receiver prototyped and presented here generates up to 557 μW and operates when $v_{EMF.S}$ is as little as 46.6 mV_{PK} across a coil separation of up to 7.0 cm. The driving advantages of this technology and those of [19]−[20] over their resonant counterparts are low-frequency operation, on-chip integration, and frequency insensitivity. And while [19] and [20] require transmitter information, this system synchronizes to $v_{EMF.S}$ on its own by counting and using the number of

clock pulses across a full cycle during a calibration phase to forecast future switching events. This way, the self-synchronizing receiver adjusts to the transmitter and draws more energy across farther distances. This means a microsystem can remain wireless between longer recharge cycles.

ACKNOWLEDGEMENT

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FIGURES

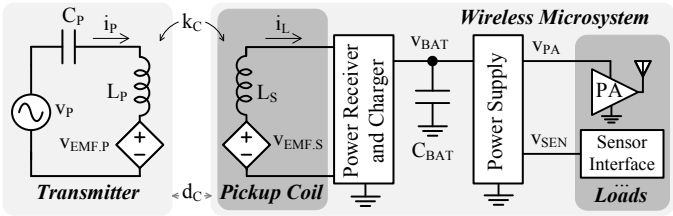


Figure 1. Inductively powered microsystem.

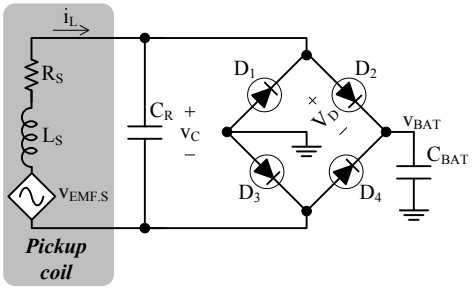


Figure 2. Resonant wireless power receiver.

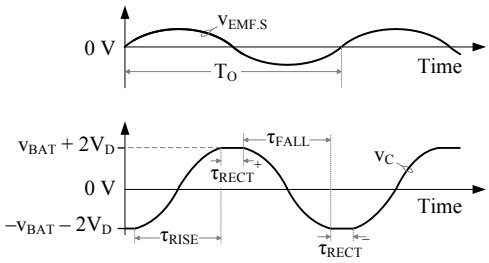


Figure 3. Time-domain waveforms of the resonant receiver.

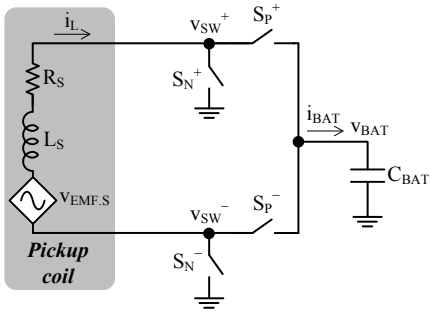


Figure 4. Non-resonant wireless power receiver.

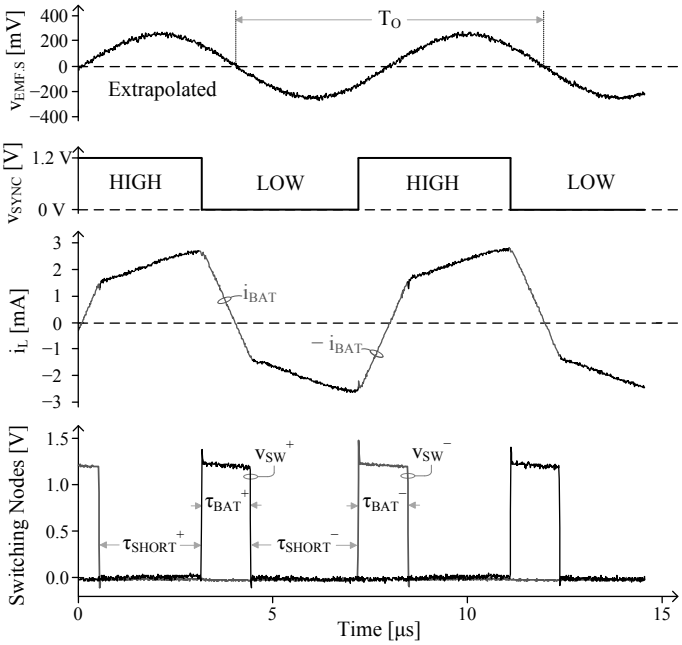


Figure 5. Induced EMF voltage $v_{EMF.S}$ and measured coil current, synchronizing signal, and switching node voltages.

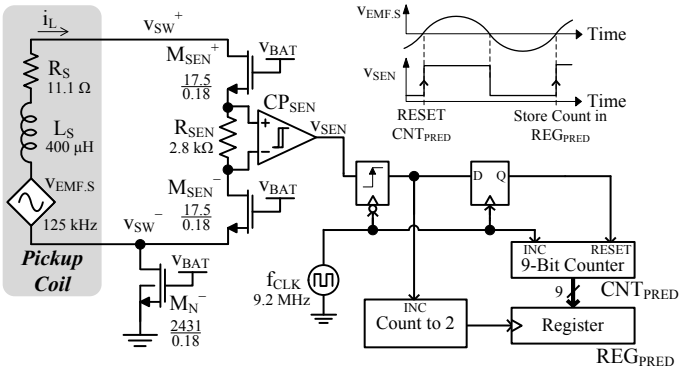


Figure 6. Calibration circuit – transistor dimensions are in µm.

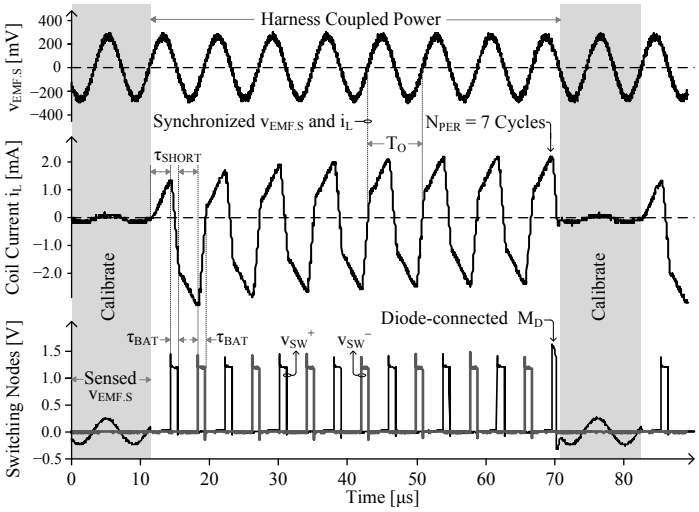


Figure 7. Measured coil voltage, coil current, and switching node voltages.

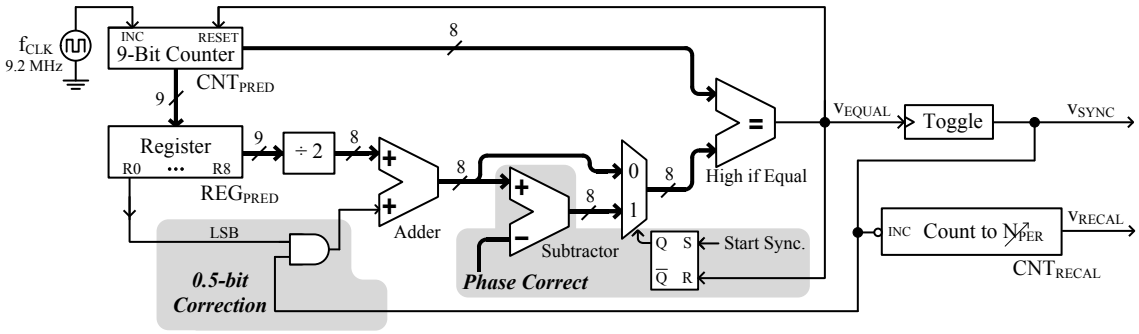


Figure 8. Synchronizer.

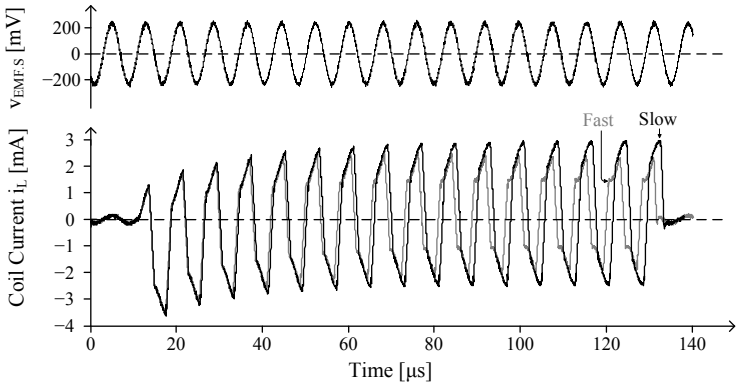


Figure 9. Measured coil currents for positive (slow) and negative (fast) phase-shift errors τ_E.

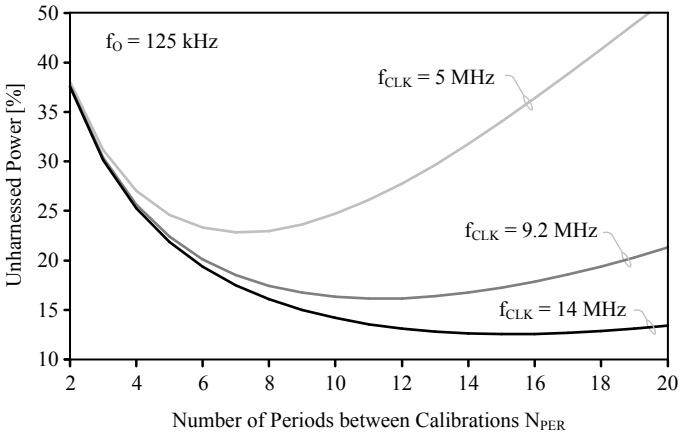


Figure 10. Unharnessed power across the number of periods per calibration cycle and sampling frequency.

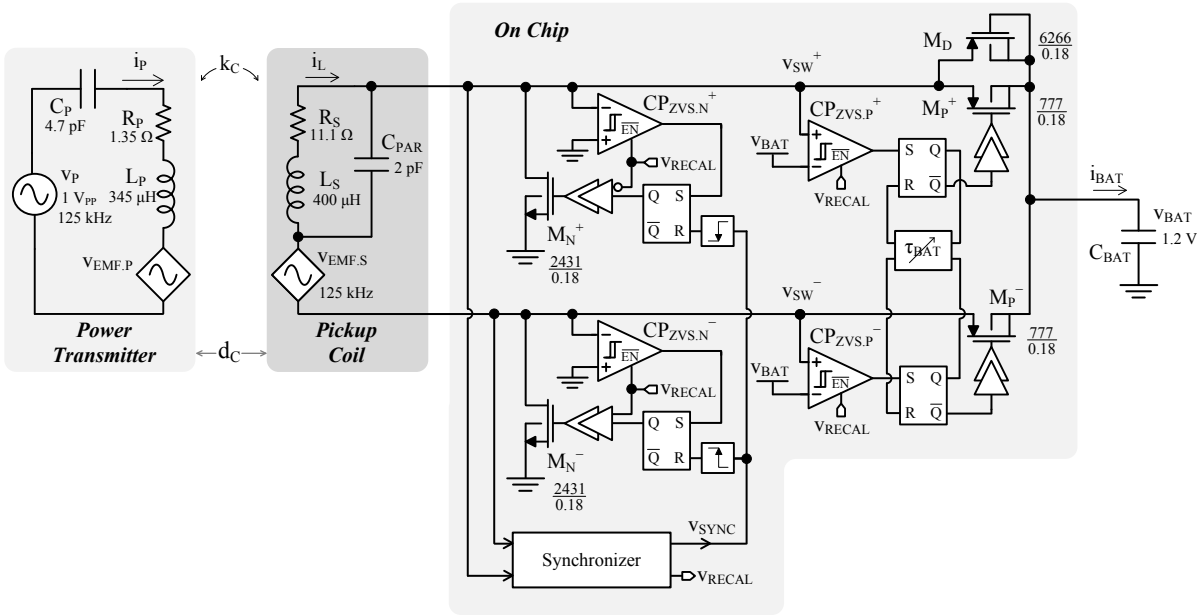


Figure 11. Prototyped non-resonant wireless power receiver.

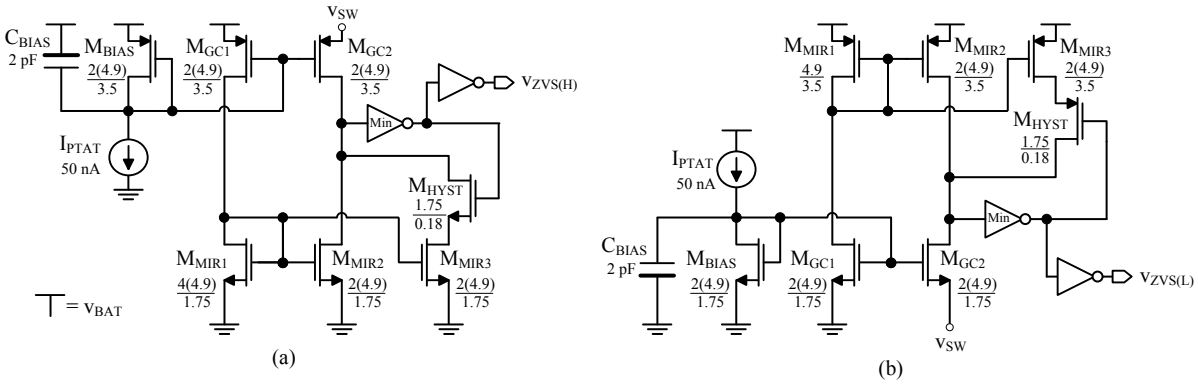


Figure 12. (a) High-side and (b) low-side zero-volt switching comparators $CP_{ZVS.P}$ and $CP_{ZVS.N}$.

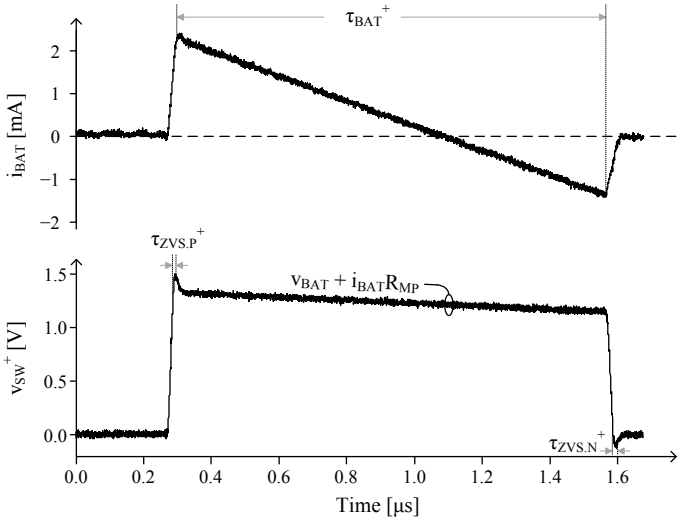


Figure 13. Measured battery current and positive switching node voltage about and across τ_{BAT}^+.

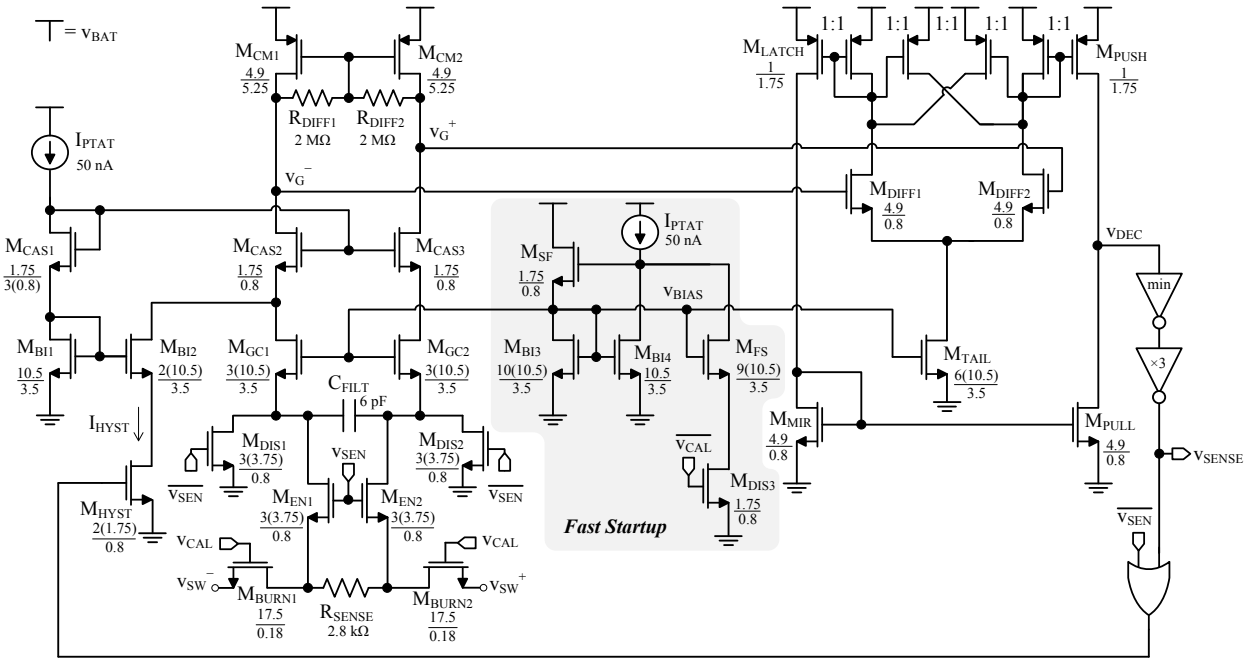


Figure 14. EMF sense comparator.

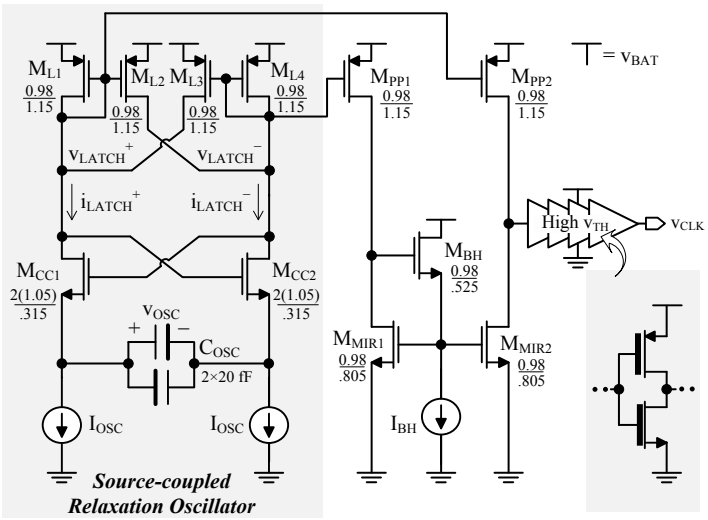
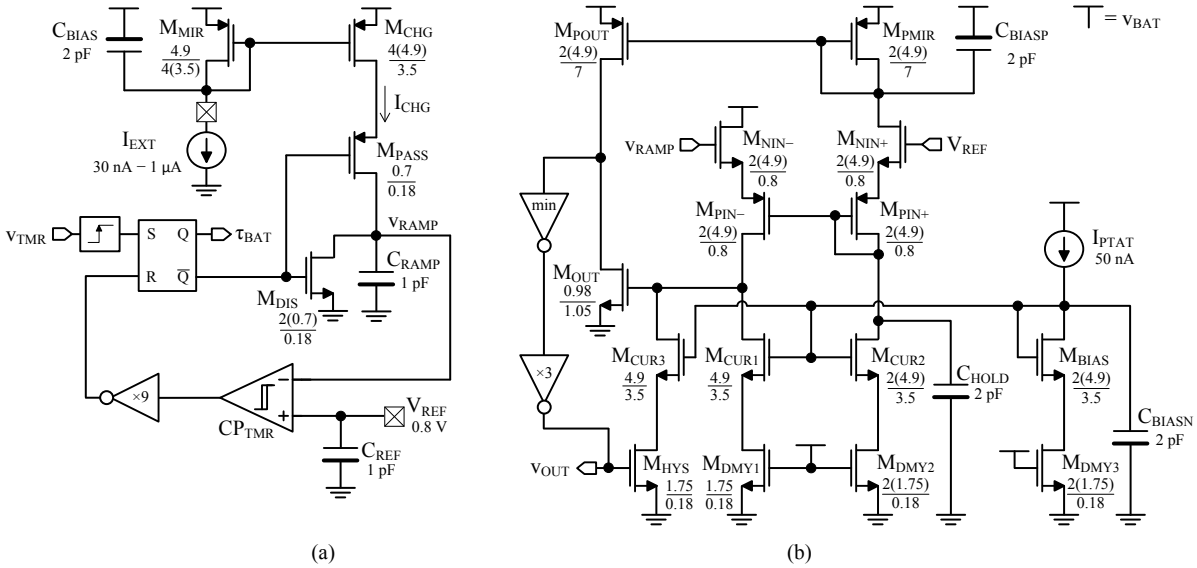


Figure 15. Relaxation oscillator.



(a) (b)

Figure 16. Delay (a) timer and (b) corresponding comparator.

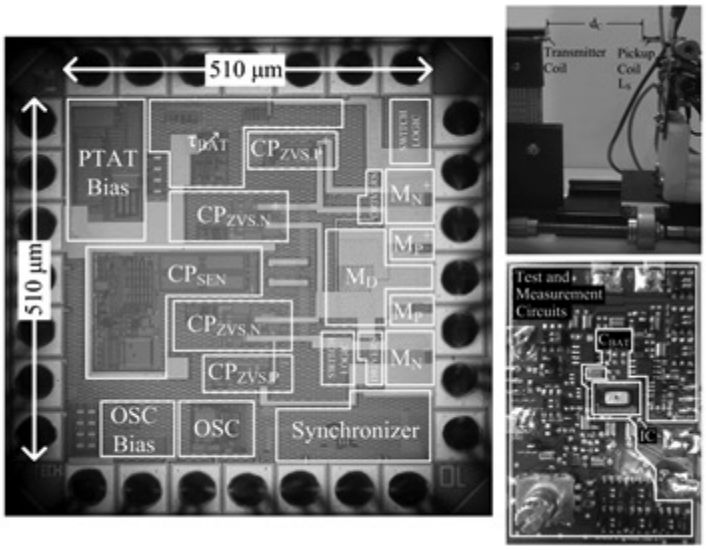


Figure 17. Photographs of the 0.18-μm CMOS die, PCB, and experimental setup.

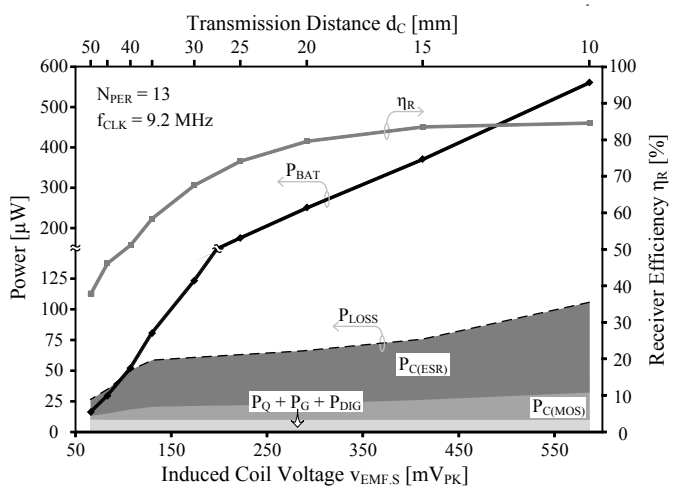


Figure 18. Measured output power, system losses, and power-conversion efficiency across transmission distance and induced coil voltage.

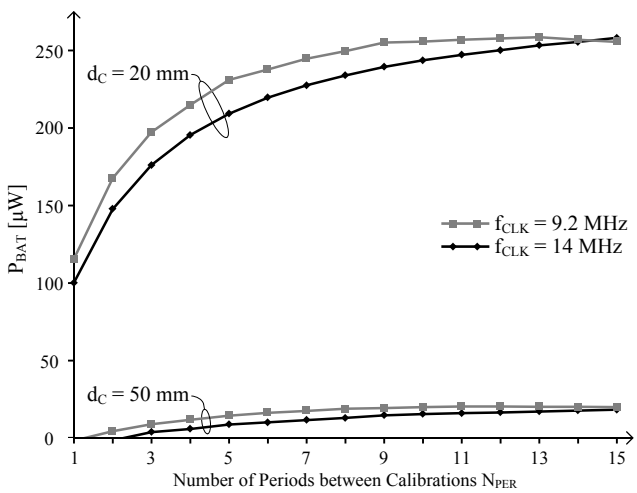


Figure 19. Measured output power across the number of $v_{EMF,S}$ periods between recalibrations at 9.2 and 14 MHz.

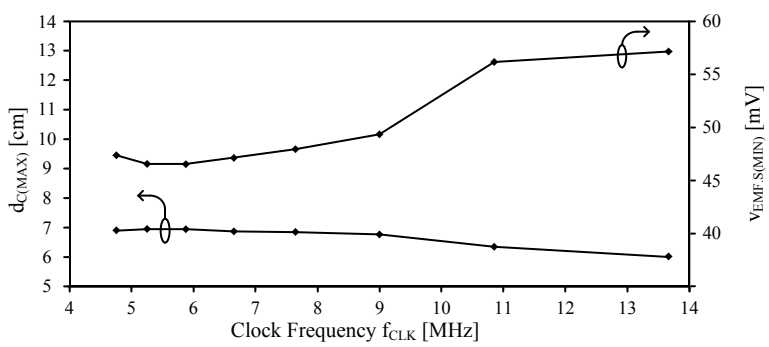


Figure 20. Measured maximum transmission distance and corresponding minimum EMF voltage across clock frequency.

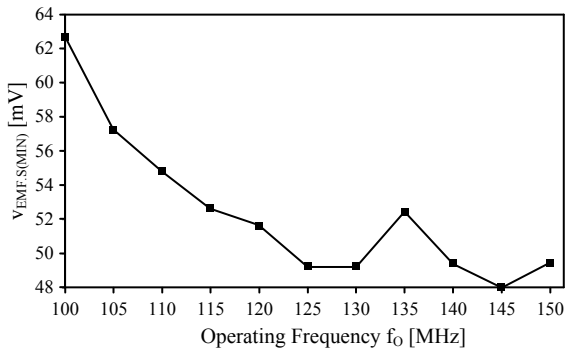


Figure 21. Measured minimum EMF voltage across operating frequency.

TABLE I. RELATIVE PERFORMANCE

	ISSCC13 [21]	**ISSCC13 [22]**	**ISSCC12 [23]**	**TCASII [19]**	**JSSC [20]**	**This Work**
Receiver Structure	Series Resonant	Parallel Resonant	Parallel Resonant	Non-resonant	Non-resonant	Non-resonant
Resonant Capacitor	200 pF	514 pF	336 pF	None	None	None
Rectifier Type	Regulating Rectifier	Voltage Doubler/ Rectifier	Voltage Doubler/ Rectifier	Inductor-based Current Rectifier	Inductor-based Current Rectifier	Inductor-based Current Rectifier
Synchronization	Self	Self	Self	Off Chip	Off Chip	Self
Battery Investment	Not Possible	Not Possible	Not Possible	Possible	Not Possible	Possible
Operating Frequency	6.78 MHz	13.56 MHz	13.56 MHz	125 kHz	125 kHz	125 kHz
Rectified Voltage	5 V	1.3 – 4 V	1X: 3.1 – 3.7 V 2X: 2.2 – 3.1 V	1 – 1.5 V	1 – 1.5 V	1 – 1.8 V
Receiver Efficiency	86%	1X: 84% 2X: 76%	1X: 77% 2X: 70%	86%	82%	84%
Chip Technology	0.35 µm BiCMOS/DMOS	0.35 µm CMOS	0.5 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Die Area	5.52 mm^2	0.11 mm^2	0.59 mm^2	0.26 mm^2	0.26 mm^2	0.26 mm^2
Pickup Coil Size	Not Stated	18 mm Diameter Loop Inductor	30 mm Diameter Loop Inductor	2.6×3.5×11.7 mm^3	2.6×3.5×11.7 mm^3	2.6×3.5×11.7 mm^3

1X: Rectifier Efficiency, 2X: Doubler Efficiency