A 1.3-µW 0.6-µm CMOS Current–Frequency Analog–Digital Converter for Implantable Blood-Glucose Monitors

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Abstract—*Blood-glucose monitors, like many biomedical implants, must operate autonomously, integrate into small spaces, and remain inconspicuous to the body. The problem is that, while including a battery large enough to sustain a system through its entire life impedes integration, under-sizing its energy reservoir to fit into a miniaturized platform shortens operational life. Fortunately, harvesting energy saves space because the environment (not the device) stores the energy a system requires. Harvesters, however, generate little power per unit volume so implantable sensors must operate under stringent power constraints. For this reason, this paper presents a 1.3-µW, 0.6-µm CMOS current–frequency (I–F) analog–digital converter (ADC). The differential, hysteretic-based ADC proposed uses nA-range input currents to set and compare voltage oscillations against a self-produced reference to resolve the input level an amperometric glucose sensor generates. The prototyped ADC ultimately draws 1.1 µA from a 1.2-V supply to resolve 0 – 32 nA with 4.25 bits of accuracy at a sampling rate of 225 Hz, which*

relatively simple and well-understood circuit and layout modifications can improve accuracy to over five bits.

***Keywords*—**Biomedical implant, blood-glucose monitor, sensor interface, CMOS analog–digital data converter, ADC.

1. INTRODUCTION

Diabetes is a disease that undermines the body's ability to metabolize glucose, and affects 2.8% of the world's population today and 4.4% by the year 2030 [1]. To control glucose levels in the bloodstream, treatment of the disease includes measuring blood-glucose concentration on a periodic basis. The benefit of such tight regulation of blood glucose is as much as 40% – 75% reductions in related complications [2], although increased prevalence of dangerously low blood sugars is also an unfortunate byproduct [3]. Currently, such monitors are commercially available, but the user must change the sensor approximately every three days, and wear an electronic reader in addition to any insulin pump the patient might use [3]. Such a maintenance schedule is not only emotionally taxing but also prone to oversights and, therefore, risks to the patient, which is why extending the operational life of blood-glucose monitors remains the subject of research today.

Inductively coupling power into the system is one way of bypassing the volumetric demands of a relatively large battery, except proximity to a powering source now becomes the constraint, as well as the frequency of such recharge cycles. The authors in [2], for example, power a complete *in-vivo* blood-glucose monitoring system wirelessly from a transmitting source; for the system to operate, however, the external source must remain within 4 cm of the implant and undergo frequent recharge cycles. Harvesting energy from the immediate surroundings, rather than external devices, removes these proximity and frequency requirements from biomedical implants [4]. The challenge here is that, while harvesters derive energy from a virtually boundless source, they generate considerably low power levels.

A tiny battery, like a thin-film lithium ion (Li Ion), for example, can compensate for the

harvester's irregularity, but not for its low power (because the battery must be small). In such a system, as Figure 1 illustrates, the Li Ion stores energy to supply on-demand power during times when the harvester is unable to harness sufficient energy. Still, because supplied power is low, the interface, processing, and telemetry components of the system cannot dissipate much power.

Although wireless telemetry is normally the primary power constraint, implants do not communicate often, and when they do, interrogators are typically nearby (within cm's). The sensor-interface block, on the other hand, operates more frequently, if not continuously, because sugar levels can rise or fall at any time. In this regard, analog–digital converters (ADCs), which continually translate sensory inputs into digital form for subsequent processing and storage (i.e., memory), are central to operating under tight power constraints [5]–[8]. Note that, without ADCs, processing and storing analog data require more power, as does transmitting more (unprocessed data).

This paper presents a proof-of-concept, current–frequency (I–F) 0.6-µm CMOS ADC that is able to resolve nA's to within five bits of accuracy while drawing 1.1 µA from a 1.2-V supply. The input range that the proposed ADC receives corresponds to what amperometric sensors produce and the power level it requires to operate is within the range that energy-harvested systems can supply [5]. This paper also studies the impact of delays on linearity in frequency-based ADCs, which is currently absent in literature, to understand and improve the linearity of the ADC presented. The novelty of the presented technology is circuit topology: how two hysteretic comparators in differential mode and simple logic convert and compare input and reference currents into frequency. Ultimately, the driving feature is compactness, the benefits of which are low power and built-in compensation of delay errors inherent to voltage/current–frequency ADCs.

In introducing the circuit, Section 2 provides architectural context to describe the criteria used to converge on the topology proposed. Section 3 follows by detailing the theoretical operation and limitations of the ADC, leaving transistor-level design details for Section 4. Sections 5 and 6 then present and evaluate experimental performance and Section 7 draws relevant conclusions.

2. MICROPOWER ANALOG–DIGITAL CONVERTERS

Most state-of-the-art micropower ADCs reported in literature today convert analog signals into the digital domain with successive-approximation techniques [9]–[15]. For that, they typically incorporate digital–analog converters (DACs) in the form of binary-weighted capacitors. Unfortunately, however, since capacitors require space and power (to charge and discharge), and capacitance in these DACs increases by a factor of two with each additional bit, both die area and power increase geometrically with precision. Ultimately, the only way to combat these effects is to decrease the size of all scaled capacitors, which degrades the matching performance of the array and, therefore, limits the accuracy performance of the ADC.

In contrast, the size of the analog components in low-speed architectures [16]–[22], such as in sigma–delta (ΣΔ), dual-slope, and voltage/current–frequency (V/I–F) converters, do not scale with precision [16], so power and die area do not increase with each additional bit. As a result, since sensors normally monitor slow-moving signals, these ADCs are better suited for harvester-powered (i.e., power-constrained) microsensors. Of these, V/I–F circuits enjoy additional advantages because they (*i*) are inherently monotonic [17], (*ii*) naturally produce a serial digital stream that a radio can use without further processing [17], (*iii*) embed an integrator that filters noise [18], and if processed differentially, (*iv*) generate time-domain signals that are relatively insensitive to ripples in the supplies (because processing voltages and currents in differential mode cancels common-mode variations).

However, nonlinearities in the voltage-controlled oscillator (VCO) that reported V/I–F ADCs employ typically limit linearity performance. Therefore, to improve linearity, [16] employs negative feedback with an amplifier and a DAC, which consume power. [21] similarly relies on negative feedback to linearize the response of a bulk-driven CMOS ring oscillator by dynamically adjusting its supply voltage. [21], on the other hand, limits the input signal range to only a few hundred mV's, which constrains the functionality of the ADC.

A fundamental issue with V/I–F ADCs is that delays across the circuit, which are inherent, constitute time-domain errors. In other words, high linearity requires delays to be considerably shorter than the shortest oscillation period. The problem with this requirement is that reducing delay amounts to increasing the speed (i.e., bandwidth) of critical blocks in the system, which normally means higher power consumption. As such, because low power means delays are a considerable fraction of the shortest oscillation period, understanding the impact of delays on linearity is critical in μW systems.

3. Proposed Microwatt Current–Frequency ADC

Frequency-based ADCs generally match the low-power and low-speed requirements that harvester-powered amperometric glucose monitors impose. More particularly, because glucose sensors ultimately generate a current, directing input current into the capacitor of a ramp-based oscillator converts current into frequency directly, which means current–frequency ADCs of this sort need not include additional power-consuming stages to condition the input. What is more, the integrating capacitor inherent in these ADCs filters unwanted noise.

Unfortunately, circuit delays, which are time-domain errors, are prevalent in these μW (i.e., bandwidth-limited) systems. For this reason, the current–frequency ADC proposed in Figure 2

attempts to match and cancel (rather than shorten) the delays across the input oscillator with those of a reference. The basic idea here is to count how many oscillations the input path experiences across a reference conversion time T_{REF}. Accordingly, output count D_O is both proportional to i_I and independent of delays, if delays in the two paths match.

3.1. Operation

More specifically, input and reference hysteretic comparators CP_I and CP_R toggle $v_{F(I)}$ and $v_{F(R)}$ when currents i_I and I_R raise and lower capacitor voltages $v_{C(I)}$ and $v_{C(R)}$ to the comparators' window limits. Tripping CP_I and CP_R changes the connectivity of switches SW_I and SW_R to reverse the direction of i_I and I_R, thereby reversing the ramps $v_{C(I)}$ and $v_{C(R)}$ carry. As a result, both loops oscillate back and forth as $v_{C(I)}$ and $v_{C(R)}$ ramp up and down to CP_I and CP_R's upper and lower window limits, as Figure 3 illustrates. To ensure CP_R switches faster than CP_I, I_R is, by design, greater than the highest possible i_I and, to ensure both loops emulate one another in every other respect, CP_I and CP_R are identical, as are C_I and C_R.

Because i_I is an indirect measure of glucose level, i_I changes so slowly that i_I is, for all practical purposes, constant over the ADC's entire sampling period, which is T_{REF} in this case. Accordingly, steering i_I into and away from C_R in alternate cycles ramps $v_{C(I)}$ up and down across CP_I's hysteretic window $V_{H(I)}$ at equal rates, so $v_{C(I)}$'s rise and fall times $t_{R(I)}$ and $t_{F(I)}$ equal and total input period T_I is

$$T_I = t_{R(I)} + t_{F(I)} = 2\left(\frac{C_I V_{H(I)}}{i_I}\right), \tag{1}$$

where $V_{H(I)}$ is $V_{T(I)}^{+} - V_{T(I)}^{-}$. The system similarly sets a reference period T_R from which to establish reference time T_{REF}:

$$T_R = t_{R(R)} + t_{F(R)} = 2\left(\frac{C_R V_{H(R)}}{i_R}\right), \tag{2}$$

where C_I equals C_R and I_R is greater than i_I (by design), so T_R is shorter than T_I. The reference path then counts 2^N (e.g., 32 in this case) instances of T_R in $v_{F(R)}$ to set T_{REF} (via D_{REF}) to $2^N T_R$. With T_I and T_{REF} established, the input-path counter counts T_I instances in $v_{F(I)}$ (with D_I) until D_{REF} at T_{REF} clocks and locks the output latch so D_O becomes

$$D_O = D_I\big|_{T_{REF}} = \text{floor}\left(\frac{T_{REF}}{T_I}\right) = \text{floor}\left(\frac{2^N T_R}{T_I}\right) = \text{floor}\left(\frac{2^N i_I}{i_R}\right), \tag{3}$$

where the *floor* function describes the counter's quantizing effect when rounding *down* to the nearest integer.

To ensure D_O is independent of previous conversions, $v_{C(R)}$ and $v_{C(I)}$ must be in phase when the counters start. Otherwise, allowing the counters to start at T_{REF} (in Figure 3) might shift the counting point in time just enough to alter the number of times the input path counts T_I in $v_{F(I)}$. Accordingly, the system holds $v_{C(R)}$ at V_T^+ by floating C_R at T_{REF} until $v_{C(I)}$ peaks at V_T^+, at which point the counters reset to zero and restart counting (at T_{START}), so the ADC can once again sample i_I.

Note that each oscillator is also a sigma–delta (ΣΔ) structure. From a ΣΔ perspective, switches SW_I and SW_R, which constitute one-bit DACs, mix input currents i_I and I_R with feedback signals $v_{F(I)}$ and $v_{F(R)}$ to generate error signals (which emulate the Δ role) for C_I and C_R to integrate (to perform the Σ function). CP_I and CP_R then quantize (i.e., digitize) the integrated error signals and the counters decimate them. Notice, however, that synchronizing $v_{C(I)}$ and $v_{C(R)}$ in the way described earlier removes the first-order noise-shaping feature normally inherent to these ΣΔ circuits [16].

3.2. Conversion Accuracy

Barring other non-idealities, conversion accuracy, as with any ADC, hinges on the reference. Current reference I_R must therefore resist variations in supply voltage, process parameters, and temperature. For this reason, design engineers typically incorporate power-supply-rejection (PSR) and temperature-compensation circuits into a bandgap-based reference [23]. Cascoding the reference and pre-regulating its supply (to increase the impedance to the supply) are typical in this regard, as are trimming (i.e., calibrating) and compensating for first- and second-order temperature-drift components in the output [24]. Fortunately, the surrounding environment of the glucose monitor is the human body, so temperature variations are small. Still, sensor current i_I ages, which is to say i_I, or for all practical purposes, I_R drifts over time. As a result, a trimmed low-power reference for I_R is necessary and therefore included in the prototype developed. The system, however, should calibrate I_R periodically to compensate for i_I's aging effects. For applications that suffer from wider temperature variations, the 6.7-nW, 165 ppm/°C bandgap-based reference of [25] may be sufficient.

3.2.1. Loop-delay Error

After the reference, the most significant source of error is the mismatch in the number of delays T_I and T_R introduce across T_{REF}, because a mismatch of this sort offsets the number of T_I's that fit into T_{REF}, which is another way of saying the ADC miscounts. Here, CP_I and CP_R, which match by design, introduce dominant but equal delays to each oscillating loop. The problem is, while CP_R consistently inserts 2^N effective delays (t_D) into T_{REF}, the number of effective delays CP_I inserts across T_{REF} varies between one and 2^N:

$$D_O' = \text{floor}\left(\frac{T_{REF}'}{T_I'}\right) = \text{floor}\left[\frac{2^N\left(T_R + t_D\right)}{T_I + \Delta T_I}\right], \tag{4}$$

where D_O', T_{REF}', and T_I' are actual (non-ideal) values. Mismatch error disappears when CP_I

switches as often as CP_R (i.e., 2^N times in one T_{REF}), which happens when i_I equals I_R so T_I equals T_R and D_O' reduces to D_O at 2^N.

When i_I is so low that $2^N t_D$ becomes a negligible fraction of T_I, D_O' also approximates to D_O:

$$D_O'\big|_{2^N t_d << T_I} \approx \text{floor}\left[\frac{2^N(T_R + t_D)}{T_I}\right] \approx \text{floor}\left(\frac{2^N T_R}{T_I}\right) \approx D_O, \tag{5}$$

which is why the difference between the ideal and actual values of the output, that is, word error D_E is lowest at the extreme ends of the input range, as Figure 4 corroborates:

$$D_E \equiv D_O - D_O' = \text{floor}\left(\frac{2^N T_R}{T_I}\right) - \text{floor}\left[\frac{2^N(T_R + t_D)}{T_I + t_D}\right]. \tag{6}$$

The maximum error, as a result, occurs towards the middle of the range. Even with comparator delays as low as 1.56% of T_R, mismatch error in D_O' (for a five-bit system) is still 0.5 LSB. Unfortunately, reducing the delay across the comparator requires additional quiescent power, which is difficult to justify when a harvester only supplies μW's. Although not as important, note that, even at the extremes, when errors disappear, t_D still extends conversion time T_{REF} by $2^N t_D$.

3.2.2. Delay-error Compensation

Literally, a delay t_d across the loop keeps SW_I from reversing the direction of i_I into C_I when $v_{C(I)}$ reaches CP_I's upper and lower window limits. As a result, $v_{C(I)}$, in practice, rises above and falls below CP_I's upper and lower thresholds $V_{T(I)}^+$ and $V_{T(I)}^-$, as Figure 5 illustrates. In other words, CP_I's hysteretic window effectively increases (to $V_{H(I)}'$). However, because CP_R suffers from the same (matched) delay, CP_R's window also increases (to $V_{H(R)}'$) and the ADC still miscounts how many T_I's fit in one T_{REF} when i_I is between its extreme values (e.g., three instead of six in Figure 5).

Because i_I is relatively constant across the ADC's sampling period (which is T_{REF} in this case)

and SW_I simply dictates direction, $v_{C(I)}$ ramps up and down at equal rates. As a result, $v_{C(I)}$ rises above and falls back to $V_{T(I)}^{+}$ in $2t_d$, and falls below and rises back up to $V_{T(I)}^{-}$ in, again, $2t_d$. This means CP_I and CP_R insert $4t_d$ (as t_D) in T_I and T_R and CP_R introduces $2^N t_D$ in T_{REF}.

Unfortunately, CP_I's delay contribution across T_{REF} is $t_D D_O$, which is not the same as CP_R's contribution of $2^N t_D$, so the resulting time difference introduces an error in the ADC:

$$T_E' = 2^N t_D - t_D D_O = 2^N t_D - t_D \text{floor}\left(\frac{i_I}{i_R / 2^N}\right). \tag{7}$$

Delay t_d's manifestation in $v_{C(I)}$, however, presents an opportunity for compensating this delay mismatch because increasing CP_I's hysteretic window $V_{H(I)}$ extends T_I. The idea is to introduce enough time ΔT_I into T_I (by increasing $V_{H(I)}$ by $\Delta v_{H(I)}$) to ensure a total of $2^N t_D$ appears across T_{REF}, which is what CP_R inserts into T_{REF}. In other words, incorporating T_E'/D_O into T_I offsets the error. This way, T_I's total delay component ΔT_I is

$$\Delta T_I = t_D + \frac{T_E'}{D_O} = 4t_d + \frac{T_E'}{D_O} \equiv 4\left(t_d + \Delta t_{H(I)}\right), \tag{8}$$

where $\Delta t_{H(I)}$ is $\Delta v_{H(I)}$'s delay contribution to ΔT_I. Since the number of T_I's in T_{REF} varies with i_I (with D_O), ΔT_I must also change with i_I (with D_O) to keep the total delay time in T_I ($\Delta T_I D_O$) across T_{REF} unchanged at $2^N t_D$:

$$\Delta T_I D_O = \Delta T_I \text{floor}\left(\frac{2^N i_I}{i_R}\right) \approx \Delta T_I \left(\frac{2^N i_I}{i_R}\right) \equiv 2^N t_D = 2^N (4t_d), \tag{9}$$

so rearranging (8) to solve for $\Delta t_{H(I)}$ and imposing (9)'s design objective for ΔT_I implies that

$$\Delta t_{H(I)} = \frac{\Delta T_I}{4} - t_d \equiv \frac{2^N (4t_d)}{4\left(\frac{2^N i_I}{i_R}\right)} - t_d = t_d\left(\frac{i_R}{i_I} - 1\right). \tag{10}$$

Since $\Delta t_{H(I)}$ lets i_I slew C_I's $v_{C(I)}$ beyond $V_{H(I)}$ in both directions, $\Delta v_{H(I)}$ reduces to

$$\Delta v_{H(I)} = \Delta v_{T(I)}^{+} + \Delta v_{T(I)}^{-} = 2\left(\frac{\Delta t_{H(I)} i_I}{C_I}\right) = \left(\frac{2t_d}{C_I}\right)\left(i_R - i_I\right). \tag{11}$$

Therefore, adding $\Delta v_{H(I)}$ to CP_I compensates for the error t_d creates in D_O. From a design perspective, establishing $\Delta v_{H(I)}$ amounts to mirroring I_R and i_I so their difference flows through a resistor R_{COMP} whose value is, by design, $2t_d/C_I$, so $V_{H(I)}$ becomes

$$V_{H(I)} = V_{H(R)} + \Delta v_{H(I)} = V_{H(R)} + \left(i_R - i_I\right)R_{COMP}. \tag{12}$$

Note, however, the absolute values of t_d, C_I, and R_{COMP} vary independently with process, which means R_{COMP} requires calibration. Still, the benefit of this form of correction is reducing power because decreasing the actual delay across the comparators requires additional quiescent power, which is often unacceptable in power-constrained systems like the harvester-powered glucose-monitor implant envisioned in this research.

4. Circuit Design

4.1. System Requirements

Monitoring and correcting the sugar level in the body accurately requires a sensitivity of 2 mg/dL across a range of 20 to 600 mg/dL, or about eight bits of accuracy [26]. However, five bits accommodates an accuracy of 10 mg/dL across dangerously low and high extremes, from 20 to 340 mg/dL, offering considerable (and practical) value to the patient. Accordingly, the ADC must resolve the current that a miniaturized amperometric glucose sensor generates, which is typically in the range of 1 nA to 1 μA [2], which in this case can reach up to 31 nA with five bits of resolution. Similarly, because miniaturized kinetic harvesters can generate less than 10 μW [27], the design aims to dissipate around 1 μW. As alluded earlier, the time constant associated with glucose variations in the body is on the order of minutes [26], so over-sampling the system

at around 100 Hz is sufficient. To meet these requirements, as summarized in Table 1, the following subsections describe the design of a 0.6-µm CMOS proof-of-concept prototype IC when supplied from a 1.2-V source.

4.2. Current–Frequency (I–F) Converter

To match the input path to its reference as much as possible, their oscillating current–frequency (I–F) converters share the same design, which is the one Figure 6 illustrates. Here, cascode-mirrors M_{N1}–M_{N9} and M_{P1}–M_{P5} receive and fold input current i_I or I_R so switches M_{SWN1} and M_{SWP2} can steer it into or away from integrating capacitor C_I. Hysteretic comparator CP_H senses C_I's voltage v_C to determine the connectivity of M_{SWN1} and M_{SWP1}. M_{SWP2} and M_{SWN2} keep the mirrors conducting to the supply and ground when their corresponding switches M_{SWN1} and M_{SWP1} are off, so the mirrors do not suffer from start-up delays, which would otherwise extend the delay across the loop (i.e., increase t_d) and distort v_C's ramp. Diode-connected M_{NREF} ultimately establishes the voltage about which v_C oscillates to ensure CP_H remains within its allowable input common-mode range (ICMR). More specifically, trip-point generator TP_{VT} references V_T^- to set CP_I and CP_R's respective upper and lower threshold levels, where CP_I's vary with i_I and CP_R's do not. In all, the reference converter uses roughly 314 nA and the input counterpart 154 – 314 nA, when processing 0 – 32 nA of i_I, so together, they draw 468 – 628 nA.

4.3. Quantizing Hysteretic Comparator

The main features of the quantizing comparator are hysteretic thresholds, low power, and short delay. To detect when capacitor voltage v_C rises above upper threshold limit V_T^+, sub-comparator CP_A's output in Figure 7 transitions high to set the S–R latch it drives. The latch, which ultimately determines the output of the overall circuit, ignores CP_A's falling transition, which means CP_A only detects a rising v_C. Conversely, sub-comparator CP_B transitions high

when v_C falls below lower threshold V_T^- to reset the latch, and the latch ignores the other transition.

For speed (i.e., high bandwidth), which is to say for short delays, CP_A and CP_B fold and combine differential input currents in push-pull fashion into a single high-impedance node. The positive feedback action of the latch then accelerates (i.e., regenerates) transitions to further improve the circuit's overall speed [28]. Also for speed, at the cost of matching (input-offset) performance, all transistors have minimum channel lengths. Finally, to keep power dissipation low, all transistors operate in sub-threshold. In the end, the entire circuit draws 50 nA from a 1.2-V supply to exhibit a nominal delay of 7 μs.

4.4. Trip-point Generator

The first objective of the trip-point generator is to set CP_R's static threshold voltages. For this, V_T^- in Figure 6 sets the lower point. Unity-gain amplifier M_{P1}–M_{P5} in Figure 8 then buffers and duplicates V_T^- on M_{P2}'s gate. As such, steering bias current I_H through resistor R_H down to M_{P2}'s gate sets a second trip point V_T^+ that is above V_T^- by $I_H R_H$, or as defined earlier, by $V_{H(R)}$.

The second aim of the circuit is to establish CP_I's dynamic trip points. For this, the circuit uses V_T^- as the lower threshold and adds a dynamic voltage to $V_{H(R)}$'s V_T^+ (as $\Delta v_{H(I)}$) to set CP_I's upper trip point $V_{T(I)}^+$. Similar to the previous case, unity-gain amplifier M_{N1}–M_{N5} buffers and duplicates V_T^+ onto M_{N2}'s gate so that steering $I_R - i_I$ through R_{COMP} adds the desired $\Delta v_{H(I)}$ to V_T^+ to generate CP_I's upper trip point $V_{T(I)}^+$. As prescribed in the delay-compensation discussion, $\Delta v_{H(I)}$ changes with i_I.

Notice the amplifiers absorb offsets between corresponding source and sink currents I_H, I_R, and i_R, albeit with a relatively minor penalty in offset voltage across input pairs M_{P1}–M_{P2} and M_{N1}–

M_{N2}. R_H is a 10-MΩ on-chip resistor that occupies 340 × 280 μm^2 and sets, together with I_H, $V_{H(R)}$ to roughly 100 mV. The absolute value of $V_{H(R)}$ does not matter, though, as long as CP_I also incorporates $V_{H(R)}$ into its hysteresis, which is the case here because $V_{H(I)}$ is $V_{H(R)}$ plus $\Delta v_{H(I)}$. R_{COMP}, however, as mentioned earlier, requires calibration, so for proof-of-concept and testability purposes, R_{COMP} is off chip in this design. In the end, the circuit draws 62 – 94 nA across i_I's 0 – 32 nA range.

4.5. Bias-current Generator

The current generator in Figure 9 generates I_R and all bias currents in the system. Here, current mirror M_3–M_4 ensures M_1 and M_2 conduct the same current so only the width difference between M_1 and M_2 can establish and impress a ΔV_{GS} across R_{PTAT} that, because M_1 and M_2 are in sub-threshold, is proportional to thermal voltage V_t, that is, proportional to absolute temperature (PTAT). However, since the sensor is in the human body (i.e., *in vivo*) and power dissipation is low, temperature is practically invariant. Operationally, M_6, M_7, and M_8 steer current into the generator when the circuit is off to ensure M_3 and M_4's positive feedback keeps the loop latched in the desired operating state. M_3–M_4's RC filter attenuates the feedback gain at higher frequencies so noise does not induce inadvertent transitions in the circuit. R_{PTAT} is off chip for tuning purposes only, to set I_R to 32 nA precisely via a 3.2 current mirror-ratio gain. In the final implementation, MOS long- and thin-channel triode resistors in sub-threshold can ultimately implement R_{PTAT} and all other mega- and giga-Ohm resistors [29]. Conventional trimming circuits and algorithms [24] would then calibrate R_{PTAT} to ensure I_R is 32 nA.

5. EXPERIMENTAL RESULTS

The prototyped 0.6-μm CMOS current–frequency (I–F) ADC IC occupies roughly 2.76 mm^2 of the 2.35 × 2.3-mm^2 die shown in Figure 10. The die is larger than required by the ADC to

accommodate several test pins. To test the system, an off-chip 0 – 32-nA current source supplied i_I by ramping slowly from 0 to 32 nA in 0.1 nA steps. For calibration, off-chip, user-defined resistors R_{PTAT} and R_{COMP} tuned I_{PTAT} to 32.0 nA at room temperature and D_O to 16 when i_I was 16 nA, halfway across i_I's 0 – 32-nA range.

On average, across six chips, as Table 2 also tabulates, the worst-case power consumption was, as expected, when i_I was 32 nA (at 1.34 μW). The reference oscillator cycled through T_R in 139 μs, on average, and through reference/conversion time T_{REF} in 4.448 ms, so the maximum possible sampling rate was 225 Hz, which meets the performance targeted in Table 1. With respect to accuracy, as Figure 11a demonstrates, output D_O increased with i_I with one LSB of error D_E up to 20 nA, after which point errors worsened considerably. On average, Figure 11b's results show that worst-case error $D_{E(MAX)}$ was 2.34 LSB. The average worst-case differential nonlinearity (DNL) depicted in Figure 11c was 0.32 LSB, which is within the 0.5-LSB window required. The average worst-case integral nonlinearity (INL) in Figure 11d was 1.68 LSB, however, which means the system was linear to 4.25 bits, not the five bits originally targeted.

6. Random Errors

While half of the ICs tested were accurate to five bits with ±0.5 LSB of DNL and ±1 LSB of INL, as originally targeted, the others were not. This discrepancy highlights a weakness in the design. Further scrutiny of the errors reveals that uncorrelated random mismatches in comparators CP_I and CP_R and trip-point generator TP_{VT} introduce a considerable offset between input and reference periods T_I and T_R that the compensation network fails to correct.

Consider random mismatches between bias currents and transistors inside each comparator ultimately refer back to the input as an offset voltage, which random mismatches in the trip-point

generator further aggravate. As a result, comparator trip points shift in relation to the other, and so do the oscillating periods they define in the proposed current–frequency ADC of Figure 2, which is equivalent to saying T_I includes a random, uncorrelated delay component Δt_d^* that T_R does not, or vice versa, or

$$\Delta T_I = 4\left(t_d \pm \Delta t_d^* + \Delta t_{H(I)}\right), \tag{13}$$

where ΔT_R is just $4t_d$. Because the system inserts D_O instances of ΔT_I across T_{REF} and 2^N instances of $4t_d$ in T_{REF}, and ΔT_I's $\Delta t_{H(I)}$ and t_d already compensate for $2^N(4t_d)$ in T_{REF}, total mismatch time and word errors T_E and D_E after compensation reduce to

$$T_E = \Delta T_I D_O - 2^N\left(4t_d\right) \approx \pm 4\Delta t_d^* D_O \approx \pm 4\Delta t_d^*\left(\frac{2^N i_I}{i_R}\right) \tag{14}$$

and

$$D_E \approx \frac{T_E}{T_I} \approx \left(\frac{2^N i_I}{i_R}\right)\left[\frac{\pm 4\Delta t_d^*}{2\left(\frac{C_I V_{H(I)}}{i_I}\right) + 4\left(t_d + \Delta t_{H(I)}\right)}\right], \tag{15}$$

where T_I is the time $v_{C(I)}$ requires to cross $V_{H(I)}$ up and down, or $2C_I V_{H(I)}/i_I$, plus comparator delay and random delay mismatch times t_d and Δt_d^*. As such, T_E and D_E increase with i_I, as the experimental results of Figure 11 exhibit and the simulation results of Figure 12 corroborate for various comparator delay mismatches. Figure 12 also shows that the errors disappear when R_{COMP} accounts for $\pm\Delta t_I^*$. Notice errors also disappear when i_I is $0.5I_R$, but this is only because the tuning point for R_{COMP} was at that setting.

The fundamental weakness in the design is transistor mismatch. Short channel lengths in comparators CP_I and CP_R and trip-point generator TP_{VT}, for example, account for a substantial offset component in CP_I and CP_R's threshold points. Mismatches in the currents that define $V_{H(I)}$

and $V_{H(R)}$ inside TP_{VT} further compound the problem.

Generally, many devices in the system should match considerably well, yet actual dimensions and layouts in the prototyped IC were (as a result of schedule constrains) not optimal for the task. Accordingly, increasing channel lengths and improving the layout of all critical transistors (with cross-coupling and common-centroid techniques and peripheral dummy devices) would improve accuracy performance. Designing an architecture that relies on fewer transistors also improves accuracy, by for example, (*i*) time-multiplexing sub-comparator CP_A in Figure 7 (i.e., CP_I and CP_R) so it functions as both CP_A and CP_B, (*ii*) eliminating the differential amplifiers from the trip-generator circuit and connecting both hysteresis and compensating resistors R_H and R_{COMP} along with their corresponding bias currents in series with V_T^-'s M_{NREF} in Figure 6 to derive $V_{T(R)}^+$ and $V_{T(I)}^+$ directly, and so on. Note that simplifying the trip-generator circuit as just described is a better solution because it reduces power and silicon area and improves performance at no expense. Trimming comparator delay mismatch Δt_d^* directly would also eliminate the problem, albeit at the cost of test time in a production environment. Regardless, keeping the maximum error below 0.5 LSB amounts to maintaining mismatch error in t_d below $1/2^{(N+1)}$, or for a five-bit system, below 1.56%, which longer channel lengths and careful layout alone should achieve [28].

Comparing the proposed technique with the state of the art is not straightforward because the prototype built suffered from significant shortcomings in the implementation. For one, resizing transistors for improved matching performance, adopting better layout techniques, and removing the amplifiers from the trip-generator circuit would improve accuracy considerably. Plus, eliminating the two amplifiers would reduce power and area, and using a technology with a finer pitch would increase speed and also reduce area. As a result, measured accuracy and speed do

not compare favorably with the state of the art, as Table 3 shows. In the end, the fundamental feature of the topology proposed is compactness, the advantages of which are low power and built-in delay-error compensation. Accordingly, even with two unnecessary amplifiers in the trip-generator circuit, power was as low as in [30] at 1.3 μW. In other words, although measured accuracy performance is not on par with the state of the art, a better implementation of the presented technique would be.

7. CONCLUSIONS

This paper presents, discusses, evaluates, and validates how the 0.6-μm CMOS current–frequency (I–F) analog–digital converter (ADC) proposed can resolve 0 – 32 nA with five bits of precision at a sampling rate of 225 Hz while only dissipating 1.3-μW (for a figure of merit of 182 pJ/level). The circuit achieves this performance by setting and comparing input-defined oscillations against a self-produced reference to resolve what input level an amperometric glucose sensor can generate. The importance of only drawing 1.1 μA at 1.2 V is that it falls within the power range that ambient kinetic and light-energy harvesters, miniaturized fuel cells, and beta-voltaic (nuclear) microbatteries produce [32]. The crux of the design is mitigating the tradeoff between power and performance, which is why the proposed ADC compensates for delay errors, which this paper proves is the dominant source of error in the system. While the prototyped proof-of-concept design produced 4.25 bits of accuracy, increasing channel lengths and optimizing the layout for matching performance with well-known techniques should improve accuracy to five bits, if not more. Ultimately, the benefit of the proposed technology is the ability to miniaturize (or equivalently, extend the life of) continuous *in-vivo* blood-glucose monitors, because small batteries exhibit short life times and large ones are invasive to the body. Inductively coupled power is appealing, but periodic recharge cycles are cumbersome to the

patient. Harnessing energy from the surrounding environment is therefore an appealing alternative, but the power levels they generate are in μW's, which is where the proposed ADC offers a significant edge, because an ADC in a microsensor usually dissipates considerably more energy than other blocks in the system, and the ADC presented here only requires 1.3 μW.

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FIGURES AND TABLES

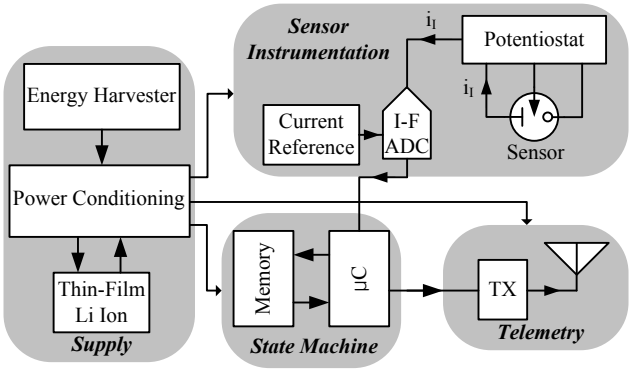

Figure 1. Harvester-powered blood-glucose monitoring implant system.

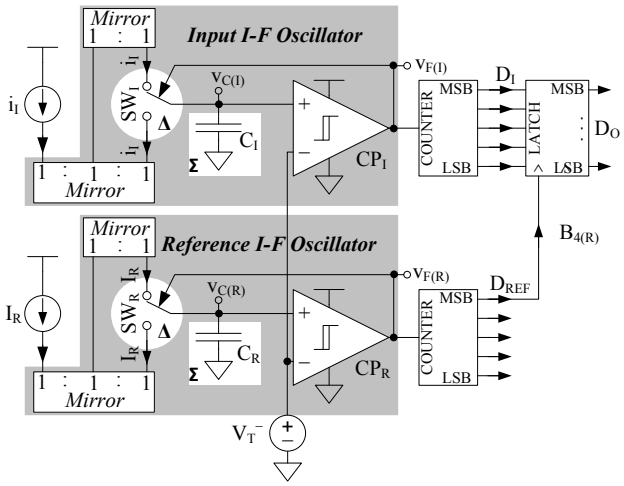

Figure 2. Proposed current–frequency (I–F) ADC.

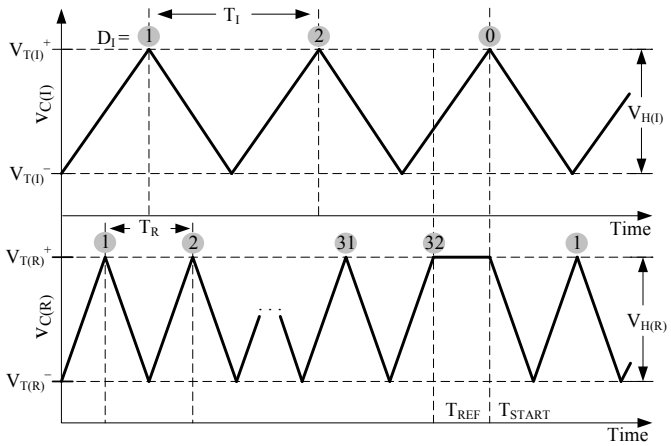

Figure 3. Input and reference capacitor voltages $v_{C(I)}$ and $v_{C(R)}$ across time.

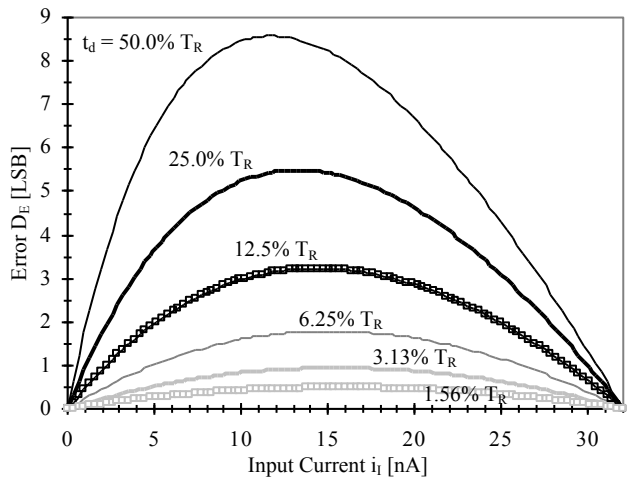

Figure 4. Word error D_E across input current i_I for several comparator delays t_d.

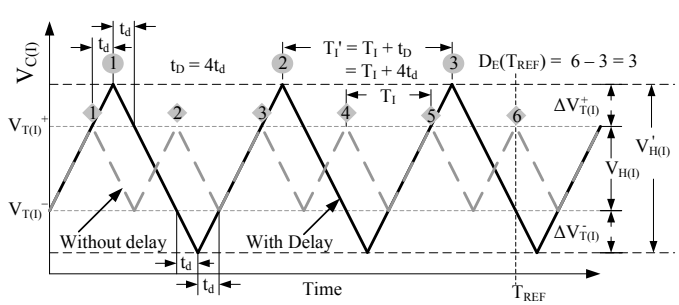

Figure 5. Input-capacitor voltage $v_{C(I)}$ with and without the effects of delay.

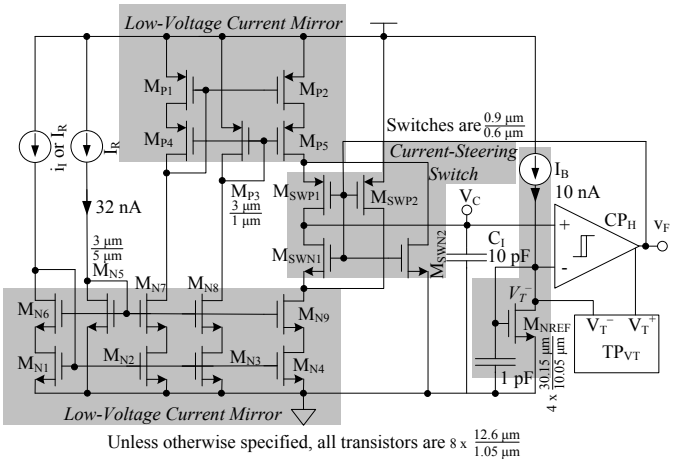

Figure 6. Oscillating current–frequency (I–F) converter circuit.

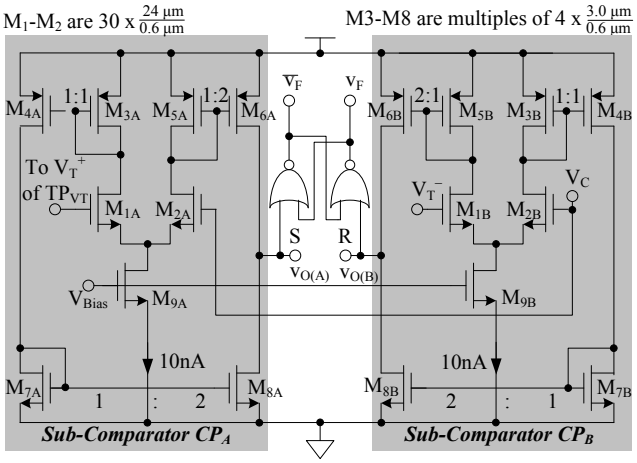

Figure 7. Quantizing hysteretic comparator.

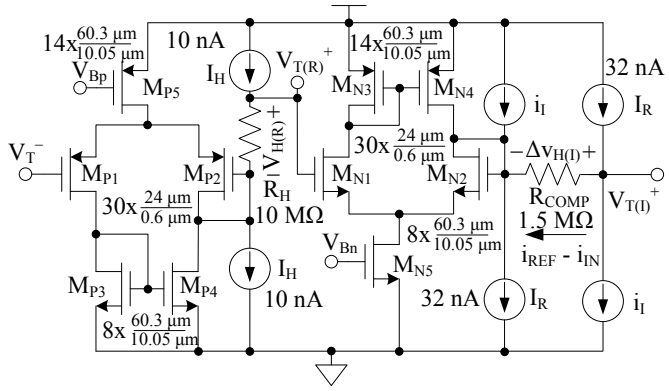

Figure 8. Trip-point generator circuit.

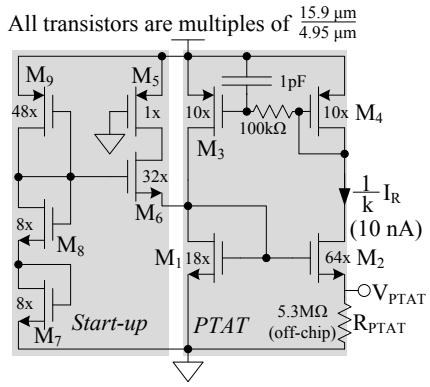

Figure 9. Proportional-to-absolute-temperature (PTAT) current reference.

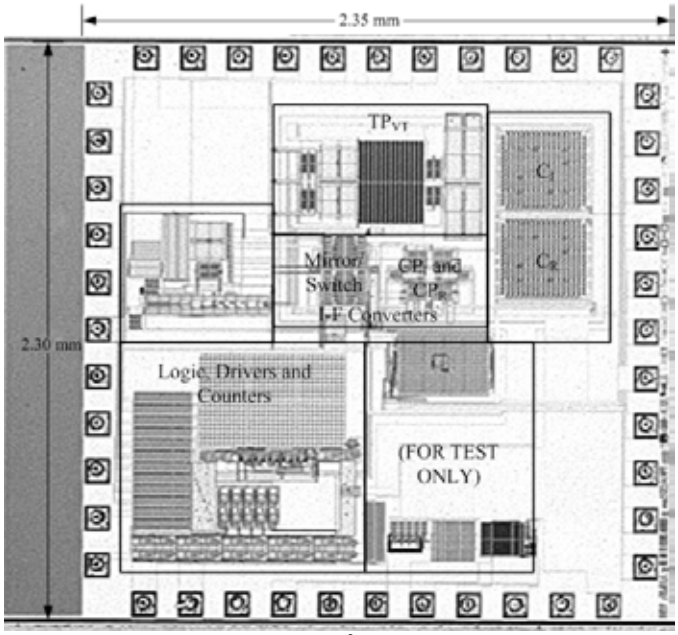

Figure 10. Prototyped 2.76 mm^2, 0.6-µm CMOS I–F ADC IC.

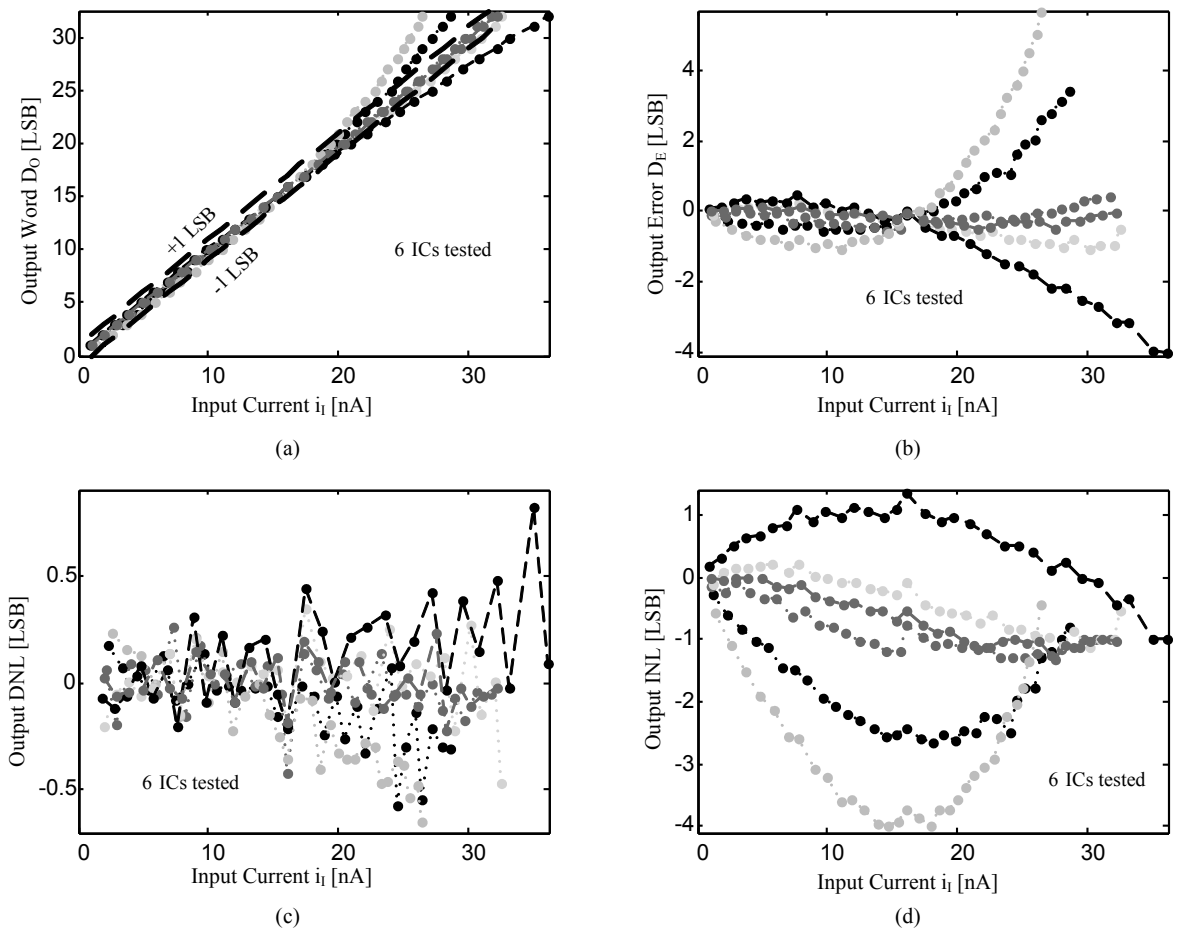

Figure 11. Measured results from six ICs across input current i_I: (a) output word D_O, (b) word error D_E, (c) differential nonlinearity, and (d) integral nonlinearity.

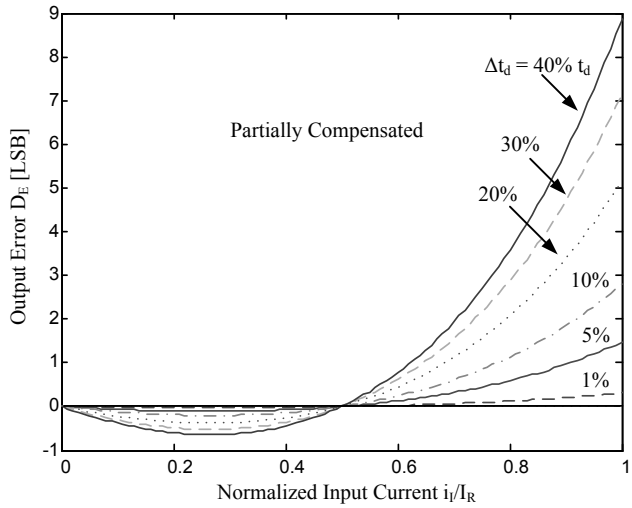

Figure 12. Error D_E across i_I/i_R for various comparator delay mismatches.

TABLE 1
SYSTEM REQUIREMENTS.

Parameter	Target
Process	0.6-µm CMOS
Supply Voltage	1.2 V
Resolution	5 Bits
Input Dynamic Range	0 – 32 nA
Sampling Rate	> 100 Hz
Power Consumption	≈ 1 µW

TABLE 2
MEASURED RESULTS FROM SIX IC PROTOTYPES.

Parameter		Mean	±3σ
Technology		0.6-µm CMOS	
Active Die Area		2.76 mm^2	
Supply Voltage V_{DD}		1.2 V	
Maximum Supply Power P_{DD}		1.34 µW	159 nW
Idle Quiescent Current I_Q		160 nA	12.2 nA
Active Current	$i_I = 0$ nA	810 nA	126 nA
	$i_I = I_R$	1120 nA	133 nA
Reference Period T_R		139 µs	67.6 µs
Reference Time T_{REF}		4.448 ms	2.163 ms
Sampling Rate f_{SAMPLE}		225 Hz	114 Hz
Maximum DNL		0.32 LSB	0.96 LSB
Maximum INL		1.68 LSB	4.32 LSB
Maximum Error $D_{E(MAX)}$		2.34 LSB	7.04 LSB
Effective Number of Bits		4.25 Bits	4.64 Bits

TABLE 3
COMPARISON AGAINST THE STATE OF THE ART.

Source	This Work	[14]	[15]	[30]	[31]
Process	0.6-µm CMOS	65-nm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS
Supply Voltage	1.2 V	1 V	1 V	0.6 V	1 V
Resolution	4.25 Bits	10 Bits	8 Bits	9.3 Bits	7.31 Bits
Input Range	0 – 32 nA	2 V_{PP}	2 V_{PP}	0.6 V	1 V
Sampling Rate	225 S/s	1 MS/s	200 KS/s	100 KS/s	400 KS/s
Power Consumption	1.3 µW	1.9 µW	19 µW	1.3 µW	6.15 µW
INL	0.32 LSB	0.56 LSB	0.68 LSB	0.8 LSB	0.53 LSB
DNL	1.68 LSB	2.4 LSB	0.66 LSB	0.7 LSB	0.9 LSB

BIOGRAPHIES

Gabriel A. Rincón-Mora (B.S., M.S., Ph.D., IEEE Fellow, IET Fellow) worked for Texas Instruments in 1994-2003, was Adjunct Professor for Georgia Tech in 1999-2001, and has now been a faculty member at Georgia Tech since 2001. His scholarly products include 8 books, 1 book chapter, 37 issued patents, over 120 scientific publications, over 26 commercial power chip designs, and over 60 international speaking engagements. Awards include SHPE's "National Hispanic in Technology Award," FIU's "Charles E. Perry Visionary Award," a "Commendation Certificate" from the Lieutenant Governor of California, IEEE CASS Service Award, Robins Air Force Base's "Orgullo Hispano" and "Hispanic Heritage" awards, and induction into Georgia Tech's "Council of Outstanding Young Engineering Alumni." He is an IEEE Fellow "for contributions to energy and power integrated circuit design;" Institution of Engineering and Technology (IET) Fellow (2009); Associate Editor for IEEE's JSSC; Associate Editor for IEEE's TCAS II; Chairman of Atlanta's Joint IEEE SSCS-CASS Chapter; Editorial Board Member for the Journal of Low-Power Electronics (JOLPE); and Technical Program Co-Chair for IEEE's ISOCC in 2011. He was a Distinguished Lecturer for IEEE's CASS in 2009-2010; General Chair for the SRC's Energy and Power IC Workshop in 2009; Circuit Design Vice Chair for IEEE's ICCDCS in 2008; Technical Program Chair for IEEE's MWSCAS in 2007; Technical Program Co-Chair for IEEE's MWSCAS in 2006; Steering Committee Member for MWSCAS since 2006; SBIR Selection Committee Review Panelist for the NSF in 2003-2007; and Vice Chairman of Atlanta's SSCS-CASS Chapter in 2004.

Andres A Blanco (B.S.) received the B.S degree in Electrical Engineering from the Georgia Institute of Technology. He is currently pursuing a Ph. D in the Georgia Tech Analog, Power, and Energy Research Laboratory under the guidance of Prof. Gabriel A. Rincon-Mora.

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