Voltage Shift in Plastic-Packaged Bandgap References

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Abstract: Bandgap references, packaged in plastic, have been known to shift in voltage, a pre-package to post-package voltage variation. This *package shift* has been analytically discussed and experimentally investigated in this paper. The culprits for such a variation are the package-induced stresses present once the reference is encapsulated. Systematic voltage shifts can range from –3 to –7 mV, and is closely related to package type and processing. Major emphasis has been placed on reducing the random package-shift component, since systematic package shift can be trimmed and its temperature coefficient compensated. The package shift is seen to have a systematic positive temperature coefficient; its effects are mitigated as temperature increases. In summary, results of the study show that die-surface planarization techniques and mechanically elastic compliant layers between the die and the package reduce random as well as systematic package shifts. In particular, systematic variations improved from –5 to –2 mV (0.4 to 0.17 % bandgap error) and three-sigma (3σ) variations improved from 8 to 4 mV (0.67 to 0.33 % bandgap error) when adding a 15 μm mechanically compliant layer between the die and the package.

I. INTRODUCTION

Bandgap references are used in a wide variety of integrated systems where accurate and precise voltage references with excellent line regulation and temperature-drift performance are required [1]. Fig. 1 shows, generically, a typical first-order Brokaw type bandgap circuit realized in a Bipolar or a BiCMOS technology. Bandgap references are critical in systems such as linear and switching regulators, analog-to-digital converters, digital-to-analog converters, and other circuits where accuracy and precision as a whole are in great demand. Bandgap references play a pivotal role in determining the accuracy and precision of these systems. Therefore, designers employ different types of trimming techniques and algorithms to compensate for process variations, temperature, and complex second-order and third-order effects [2].

However, bandgap references encapsulated in plastic packages exhibit a characteristic shift in voltage. Once it is packaged in plastic, the bandgap reference's output voltage differs from its original, non-packaged value. This *package shift*, unfortunately, is not completely consistent from unit to unit, even if the same encapsulant and packaging technique is used. This randomness is detrimental since designers cannot easily account for this variant in the design phase. Various authors have reported changes in device parameters as a result of mechanical stresses exerted by the plastic encapsulant and the packaging techniques used [3]-[6].

This paper reports the investigation of post-package shift in bandgap voltage references, including the effects on its temperature coefficient. Primary consideration is placed on minimizing the systematic and random package shift. Section II, particularly, discusses the causes of stress in plastic-packaged devices as well as the types of stresses present within the package. Section III delves into the specific effects of mechanical stress on bandgap references. Section IV illustrates the techniques used to minimize package shifts while Section V details the

experimental results of the techniques implemented. In Section VI, conclusions are drawn and discussed.

II. STRESS IN PLASTIC PACKAGES

Integrated Circuits (ICs) encapsulated in plastic have enjoyed popularity in the semiconductor industry because they are relatively inexpensive, compact, and moisture resistant. In search of system-on-chip solutions, more and more functionality is incorporated into ICs, which increases die size. In the meantime, however, all attempts are also made to reduce the size of the package encapsulating these chips. For plastic packages, unfortunately, this trend implies an increase in the internal stresses placed on the die by the plastic encapsulant, which lead to parametric shifts, cracked passivation, metal movement, and even die cracking [7].

The main cause for internal stresses in plastic packages is the difference in coefficient of thermal expansion of the plastic mold and the silicon die. Most of the plastic molding is done at a temperature of 175 ^{o}C to lower the viscosity of the plastic mold. The plastic, which has a typical coefficient of thermal expansion greater than ten times that of silicon, transmits an ever-increasing stress to the chip as the package cools from molding to ambient temperature. While encapsulation is the primary culprit of plastic package shift, the process of die attachment to the leadframe also plays a minor role [5].

A. Die Attachment

There is a significant difference in the thermal expansion coefficients of silicon and the leadframe. The die-attach process takes place at elevated temperatures, and as the die-leadframe is allowed to cool, the leadframe portion contracts to a greater degree than the silicon die, resulting in residual tensile stresses at the chip surface. This residual stress state prevails in ceramic packages. However, the magnitude of the stress is not sufficient to cause significant

parametric shifts, assuming an epoxy die-attach process is used, which is the typical case for plastic packages. The use of solder or gold eutectics for the die-attach process, on the other hand, imposes more stresses on the die. Different types of die-attach compounds as well as mechanically compliant layers between the die and the leadframe have been used to minimize stress at this level [5].

B. Plastic Encapsulation

After wire bonding, plastic encapsulation is performed at about 175 ^{o}C. As the structure is brought to room temperature, the plastic mold contracts to a greater extent than the die due to, again, differences in thermal expansion coefficients. This difference results in normal compressive stresses and shear stresses on the die. For most plastic packages, the normal compressive stresses in the *x*-direction (s_{xx}) and the *y*-direction (s_{yy}) are about an order of magnitude larger than the normal stress in the vertical *z*-direction (s_{zz}). This characteristic difference results because the lateral dimensions of the plastic mold are significantly larger than the thin vertical plastic layer on top. Vertical s_{zz}, of course, increases with thicker layers of plastic mold. The shear-stress tensor $\langle\tau_{xy}, \tau_{yz}, \tau_{xz}\rangle$ for *x*-*y*, *y*-*z*, and *x*-*z* planes, respectively, is also about an order of magnitude smaller than normal compressive stresses s_{xx} and s_{yy}. A combination of surface normal stresses and shear stresses at the die-plastic interface is responsible for such catastrophic failures as metal deformation, plastic cracking, and die cracking [7].

Strain gauges placed on chips to identify package stresses have shown that surface compressive stresses s_{xx} and s_{yy} are highest at the center of the die, while s_{zz} is highest at the corners and the edges of the die. All three normal stresses, however, are uniform towards the center of the die while showing large gradients towards the edges and, especially, the corners of the die. All three shear stress components, τ_{xy}, τ_{yz}, and τ_{xz}, are highest at the corners and the

edges of the die and lowest towards the center of the die. The shear components show large gradients but they tend to be minimal at the center of the die. Fig. 2 shows the relative magnitudes and distribution of the stresses obtained through finite-element simulations for one quarter of the die [8]. These calculated values may not agree exactly with actual conditions; but, the relative stress magnitudes and the distribution shape are accurate. These stress distributions warrant designers to be conscious of the placement of sensitive analog circuitry on the die.

One of the main vertical compressive stress-related failure mechanisms reported in the literature is the filler-induced mechanism [9]. The plastic mold consists of silica fillers that vary in size and shape, as shown in Fig 3. The fillers are used, among other reasons, to reduce the thermal coefficient expansion of the package to prevent destructive effects like corner and passivation layer cracking as well as metal-line shifts. Depending on the size, shape, and orientation of these fillers, they exert intense stress fields on localized regions of the die. These fillers have been reported to cause failures in sense amplifiers of DRAMs by increasing the source-bulk and drain-bulk leakage currents of MOSFETs by several orders of magnitude [9].

III. EFFECTS OF MECHANICAL STRESS ON BANDGAP REFERENCES

Compressive stresses, and the resulting strain, can change several physical characteristics of semiconductors. The most significant of these changes are variations in the energy band structure of the semiconductor, which is manifested by increases in minority carrier concentrations. Other important changes include variations in hole and electron mobility as well as generation-recombination levels.

A. Stress Effects in BJTs

Quantum-mechanical studies have shown that changes in the energy band structure results in a decrease in the bandgap energy of semiconductors, like silicon and germanium, and a

corresponding increase in minority carrier concentration [10]. Furthermore, these increases in minority carrier concentration depend on the crystalline direction (e.g. [100], [111], or [011]) in which the stress is applied; although, this effect is minimal in silicon. The ratio of stressed minority carrier density to that of unstressed minority carrier density can be written, in general, as

$$\frac{p_n}{p_{no}} \equiv \gamma(\varepsilon_n) \geq 1 \qquad (1)$$

and

$$\frac{n_p}{n_{po}} \equiv \gamma(\varepsilon_p) \geq 1, \qquad (2)$$

where p_n and n_p are the stressed minority carrier concentrations in *n*-type and *p*-type material, respectively, p_{no} and n_{po} are unstressed minority carrier concentrations, and ε_n and ε_p are the position-dependant strains in *n*-type and *p*- type material, respectively, which emphasize that γ is a function of stress. Fig. 4 depicts theoretically calculated values of $\gamma(\varepsilon)$ for silicon. The term $\gamma(\varepsilon)$ is a function of several exponentials, and could be approximated by a single exponential in the stress region 10^8-10^9 Pa, which is the order of magnitude for stresses in plastic packages (Fig. 2).

The reverse saturation current (I_s) of an *n-p-n* BJT can be written as

$$I_s = \frac{qA\overline{D}_n n_p}{W_B} = \frac{kA\overline{\mu}_n T n_p}{W_B}, \qquad (3)$$

where q is the electric charge, k is Boltzman's constant, A is the cross-sectional area of the emitter, $\overline{D}_n$ is the average effective electron-diffusion constant $(\overline{D}_n = \overline{\mu}_n V_T)$, $\overline{\mu}_n$ is the average

effective electron mobility, V_T is thermal voltage $(V_T = kT/q)$, T is temperature, W_B is the base width, and n_p is the base minority carrier density. By substituting (2) in (3), I_s can be written as

$$I_s = \frac{kA\bar{\mu}_n T n_{po} \gamma(\varepsilon)}{W_B} \approx I_{so}\gamma(\varepsilon), \tag{4}$$

where I_{so} is the reverse saturation current of the BJT in the unstressed state. Note that, compared to increases in minority carrier concentration, stress-related changes in the electron mobility have been assumed to be negligible on I_s as [10] points out. Thus, one of the results of placing stress on a BJT is to increase its reverse saturation current.

B. Stress Effects on Bandgap Voltage

The bandgap voltage V_{BG} for a first-order Brokaw bandgap reference circuit, shown in Fig. 1, is given by

$$V_{BG} = V_{BE1} + 2\frac{R_2}{R_1} V_T \ln(N), \tag{5}$$

where V_{BE1} is the base-emitter voltage of Q_1, V_T is the thermal voltage, and N is the ratio of base-emitter areas of Q_2 and Q_1 ($N = I_{s2}/I_{s1}$), and I_{s1} and I_{s2} are the reverse saturation currents of Q_1 and Q_2, respectively. If V_{BGo} is taken to be the unstressed bandgap voltage, then the shift in the bandgap voltage ΔV_{BG} due to stress can be defined as

$$\begin{aligned} \Delta V_{BG} &= V_{BG} - V_{BGo} \\ &= \left[V_{BE1} + 2\frac{R_2}{R_1} V_T \ln(N) \right] - \left[V_{BE1o} + 2\frac{R_{2o}}{R_{1o}} V_T \ln(N_o) \right], \end{aligned} \tag{6}$$

where the "*o*" subscript denotes unstressed values. If the bandgap reference is placed in a uniform stress field and proper layout techniques have been used to match resistors as well as BJTs (discussed further in Section IV), then

$$\frac{I_{s2}}{I_{s1}} \approx \frac{I_{s2o}}{I_{s1o}} \Rightarrow N \approx N_o \tag{7}$$

and

$$\frac{R_2}{R_1} \approx \frac{R_{2o}}{R_{1o}}. \tag{8}$$

Then, the bandgap voltage shift becomes

$$\Delta V_{BG} \approx V_{BE1} - V_{BE1o} = V_T \ln\left(\frac{I}{I_{s1}}\right) - V_T \ln\left(\frac{I_o}{I_{s1}}\right) = V_T \ln\left(\frac{I\,I_{s1o}}{I_o\,I_{s1}}\right), \tag{9}$$

where

$$I = \frac{V_T \ln(N)}{R_1}. \tag{10}$$

Currents I and I_o are the corresponding collector currents of the stressed and unstressed bandgap circuit, respectively. Since N is approximately equal to N_o, and assuming that the stress effects on resistor R_1 are negligible (e.g., polysilicon resistors [11]), I is roughly equal to I_o, thereby making package shift ΔV_{BG} equal to

$$\Delta V_{BG} \approx V_T \ln\left(\frac{I_{s1o}}{I_{s1}}\right) \approx V_T \ln\left(\frac{1}{\gamma(\varepsilon)}\right) = -V_T \ln[\gamma(\varepsilon)]. \tag{11}$$

Therefore, the effect of package stress on the bandgap reference is to lower its voltage by an amount approximately given by (11).

C. Temperature Effects on the Bandgap's Package Shift

Theoretically, post package stress is a result of a difference in the thermal expansion coefficients of the plastic mold and the silicon die. Therefore, it can be shown, approximately, that:

$$\varepsilon \propto s \propto (T_{sp} - T); \quad T < T_{sp}, \tag{12}$$

where ε is the die strain, s is the stress on the die, and T is temperature below the molding set-point T_{sp}, which is usually around 175 ^{o}C [12]. The stress placed on the die by the plastic is directly proportional to the molding set temperature. As a result, the bandgap voltage shift worsens with higher temperature differentials from the molding set point. Because stress is directly proportional to temperature deviations, and since $\gamma(\varepsilon)$ can be approximated by an exponential relationship (Fig. 4), (11) and (12) show that the bandgap voltage shift resembles a parabolic relationship with temperature:

$$\Delta V_{BG} \approx -V_T \ln[\gamma(\varepsilon)] \approx -V_T \ln\left[e^{k_1 s + c_2}\right] = -V_T \ln\left[e^{c_1 (T_{sp} - T) + c_2}\right] = -c_0 T\left[c_1\left(T_{sp} - T\right) + c_2\right], \quad (13)$$

where k_1, c_0, c_1, and c_2 are physical, semiconductor, and package related constants.

IV. MINIMIZING PACKAGE SHIFT

Because of the complexity and irregularity of the stress in plastic packages, the bandgap package shift, from unit to unit, is not completely consistent. The package shift can therefore be represented with two components: a systematic mean component and a random component. The systematic mean component is largely based on the particular plastic package used and the process used to package it, and is reflective of the stress placed on the die by that package type. Consequently, the systematic component can be compensated in the design phase. The random component of the shift, on the other hand, is the result of unpredictable variations of the stress matrix and is assumed to conform to a Gaussian distribution.

In statistical analysis, the systematic component can be characterized by the mean (μ) of the distribution and the random component by the standard deviation (σ). Fig. 5 depicts the systematic and random components of package shift. In the case of bandgap package shift, the systematic component and the random component are not entirely independent, as shown in Fig.

6. Since bandgap package shift is almost always negative, reducing the systematic mean component reduces the available window for random variations. Unfortunately, stress in plastic packages cannot be eliminated unless expensive packaging techniques are used. From a designers perspective, the best approach to package shift is to trim off the systematic shift and somehow minimize the random shift. Fig. 5c illustrates the projected response of the solution to package shift, once trimmed.

Minimizing the random component of the package shift mainly involves reducing the stress gradients, or conversely, achieving a uniform stress field in and around the area where the bandgap reference is located. Location of the bandgap reference on the die could be a very important factor in minimizing the random component. As discussed earlier, at the center of die, normal in-plane compressive stresses tend to be uniform and shear stresses along with vertical compressive stresses tend to be minimal. Therefore, the center would offer the best protection against stress gradients. The edges and, especially, the corners yield the worst performance since normal compressive stresses at those locations, although minimal, show large gradients. Additionally, shear and vertical stresses are at their highest and also show large gradients at the edges and corners of the die. Therefore, to minimize the random component, the two BJTs and the resistors that constitute the bandgap cell shown in Fig. 1 should always be placed as close to the center as possible. Stresses near the vicinity of the bondwires, as expected, are also high and have significant effects on package shifts.

Precise matching of devices also helps to minimize the random component of the package shift, as well as improve inherent accuracy, of course. For the first-order bandgap reference in Fig. 1, devices that require matching include BJTs Q_1 and Q_2 and resistors R_1 and R_2. Precise matching of devices minimizes any variations in their ratios after packaging. Its primary intent is

to reduce the effects of uniform and linearly process-dependent gradients across the die. Proper layout techniques, such as interdigitization, common-centroid techniques, and cross-coupling are utilized effectively towards this end. If possible, matched devices, which must be close to each other and be compact, should be placed on locations that would take advantage of the symmetrical nature of the stress components (Fig. 2). If the fabrication process permits, R_1 and R_2 should be designed with a low piezoresistive material. In general, polysilicon resistors exhibit much lower piezoresistivity than diffused resistors.

In minimizing package shift, the effects of overall die aspect ratio, die surface texture, and mechanically compliant layers (“sandwich layers”) have been investigated. These experiments were performed with the bandgap reference circuits placed squarely on the center of the die, taking care of matching all appropriate devices. The aspect ratio of the die can determine the level of strain the die experiences under stress. Deformation of the die, such as structural twisting and bending, which is a function of torque placed on the die, affects all the devices on the die and adds to the effects of localized strain. Rectangular structures with large aspect ratios, length to width, are more prone to such deformations under stress than square structures made of the same material. An example of this type of deformation is shown in Fig. 7. Therefore, square dies potentially yield better performance than their rectangular counterparts in minimizing the random component of the package shift.

Under normal processing, the surface of the die has an uneven texture, mainly a result of the presence of the top metal layer. The top metal lines yield abrupt topographical “humps” while the pitch between them creates “troughs.” The field-oxide and passivation layers on top mimic this incoherent texture. A cross-sectional image of a non-planarized wafer is shown in Fig. 8a. As a result of this coarse surface texture and the fillers in the plastic mold, the stress-field from

the plastic mold is non-uniform, as shown in Figs. 8 and 9. Such a non-uniform field leads to enhanced random shift behavior. Therefore, planarizing the surface, to flatten it, alleviates the random shift. A cross-sectional image of a planarized wafer is shown in Fig. 8b.

An elastic thick-film layer in-between the plastic mold and the die surface can absorb some of the stress from the plastic mold and minimize the "filler-induced effects" by distancing the die away from the filler-loaded plastic. As discussed earlier, the filler–induced effect is very random in nature, depending on the size, the orientation, and the position of the filler particles with respect to the chip surface. Therefore, this 15 μm elastic "sandwich layer" can minimize the random package shift component by achieving a uniform stress field. Fig. 8c shows an image of a chip with a "sandwich layer" placed between the die and the plastic. Note that, before depositing the "sandwich layer" (proprietary stress-relief material), the wafer was planarized. Other techniques used to minimize package-induced stresses include dropper-applied and spin-on overcoats. The dropper-applied and spin-on overcoats are typically very thick layers ultimately preventing the use of very low profile packages. Low stress molding compounds are also used but they are intended to prevent die cracking and delamination and actually yield marginal package-shift improvements.

V. EXPERIMENTAL SETUP AND RESULTS

A test suite was designed to investigate the effects of aspect ratio, die surface texture, and "sandwich layers" on bandgap package shift. The test suite consisted of a well-characterized bandgap reference (Fig. 10) placed squarely on the center of both a square die ($W \times L$ = 2034 × 2034 μm^2) and a rectangular die ($W \times L$ = 2034 × 4193 μm^2), shown in Fig 11. The practical bandgap reference used is shown in detail in Fig. 10, which is a Brokaw cell ($Q_{6\text{-}10}$ and $R_{2\text{-}3}$) biased with a Proportional-to-Absolute-Temperature (PTAT) current generator ($Q_{1\text{-}4}$, $M_{2\text{-}3}$, and

R_1) and a current-mode startup circuit (M_1, M_6, M_5, and Q_5). As to layout, by choosing the width of the rectangular die to be equal to the square die, any difference in lateral displacement of the bandgap reference from the edges is eliminated. Even though the rectangular die seems to reap the benefits of longitudinal displacement from the bandgap circuit to the edge, the overall performance is still degraded because of the effects of aspect ratio, as discussed earlier and depicted in Fig. 7.

To ascertain the effects of planarization and the 15 μm thick "sandwich layer," only the square dies were tested. Non-planarized dies were used to test aspect ratio effects. To simulate and statistically analyze the effects of the planarization and the "sandwich layer" methods in actual production, some of the devices were trimmed to 1.2 V before packaging. As a result, these devices display a narrow rectangular distribution resulting from finite trim resolution, as shown in Fig. 5. A probe station was used to measure the bandgap voltage before the IC was packaged. The probe station was enclosed by a dark cover to eliminate any extraneous illumination effects on the reference voltage. Normal fluorescent lighting, depending on the shading provided by the probe station itself, was found to cause a 1-3 mV decrease in the bandgap voltage. Additionally, *n-p-n* BJT structures were packaged and tested to determine the package shift in their reverse saturation currents, I_s.

Each die was data logged, for tracking purposes, before and after packaging. Keeping track of each device allowed the individual package shifts to be monitored and statistically analyzed. The square and rectangular dies, as well as the *n-p-n* BJT structures were packaged in 16-pin Plastic Dual-Inline-Packages (PDIP). The standard characteristics of the leadframe and the plastic resin are shown in Table 1. For the devices that were trimmed, only post-package data

was obtained. As a result, offset voltage from the "ideal" voltage of 1.2 V was collected for these particular devices, and not the actual package shift.

The packaged *n-p-n* BJTs' reverse saturation currents increased by roughly 27 % at room temperature. The statistical mean and the standard deviation results of the package shift for the square dies sent through all three processes, the rectangular dies sent through just the normal non-planarizing process, and post-package voltage variations for the trimmed devices are summarized in Table 2. The table also provides the number of devices tested. The measurements were taken at room temperature. The non-planarized square dies yielded a package shift mean of about 14 % lower than the rectangular dies. The square dies produced a three-sigma (3σ) package shift improvement of 4 % over the rectangular dies. This is marginally better performance and may not be economically justifiable.

When planarized, both the mean and the standard deviation of the square die improved by 16 and 18 %, respectively. With the "sandwich layer" the mean and the standard deviation improved even further. From the planarized to the especially coated dies, the mean improved by 37 % and the standard deviation improved by 36 % while improving 47 and 48 %, respectively, relative to non-planarized dies. Thus, in these experiments, coating the top of the die by a layer of about 15 μm in thickness alleviated random package shift by almost one-half. The offset performance of the trimmed devices showed no significant improvement with planarization. With the "sandwich layer," however, a 3σ improvement of 35 % was achieved. This sigma improvement, which is the result of the 15 μm layer of mechanically compliant material, intimates that random local stresses were reduced, i.e. the silica-filler effects (Fig. 3). Global effects caused by die-wide stresses are not expected to improve with a layer only 15 μm thick,

which corroborates the hypothesis that global gradients have a lower random component effect. Improvements are expected to be more significant as the elasticity of the material used for stress relief increases as well as its thickness, of course.

The temperature dependence of the bandgap package shift was also investigated. Measurements were performed at 15, 25, 50, 75, and 100 ^{o}C. The range of temperatures tested was limited by the physical constraints of subjecting the wafer to temperature extremes at the probe station. For example, the temperature could not be taken below 15 ^{o}C due to the condensation on the wafer surface; and, similarly, it was difficult to reliably maintain a very high temperature above 100 ^{o}C. Fig. 12 shows the temperature variation of the bandgap package shift for several devices. Note that the empirical data indicates a mostly linear relationship of package shift versus temperature, which may just be because a relatively small range of temperature was measured. However, the Temperature Coefficient (TC) of the package shift shows variation from unit to unit, just like package shift itself. For this experiment, assuming a mostly linear TC for the package shift, the average TC was about 0.044 mV/^{o}C and its standard deviation was about 0.012 mV/^{o}C. Fig. 13 shows a temperature measurement of a bandgap reference before and after packaging. Note that the TC of the bandgap reference becomes more positive after packaging. The designer, as a result, can compensate the mean by including the TC of the package shift in the temperature compensation of the circuit.

VI. CONCLUSION

Package-induced offsets, like most real-life parameters, unfortunately, vary from unit to unit while roughly conforming to a Gaussian distribution. For sensitive systems that depend on the bandgap reference for accuracy and precision, this random voltage shift can be a major

detriment. From a designer's perspective, the problem is addressed in two ways: (1) compensating the mean offset as well as the mean TC and (2) minimizing the effects of the mechanisms that cause random variation. The best approach to compensate for the mean package shift offset and its TC, which turns out to be mostly linearly positive in the temperature range of interest, is to include it in the design of the circuit itself. Particularly, it can be included when ascertaining the trim-target voltage, by appropriately adjusting the Proportional-To-Absolute Temperature (PTAT) component. As a result, characterization of the bandgap circuit within its particular package is required. With regards to random variations, incremental improvement is obtained by planarizing the IC. This improvement, however, may not be cost-efficient in a mass production environment. Placing the die in the center of a square die, given the choice and flexibility, is prudent. Additionally, if the process technology permits, adding a moderately thick, yet thin relative to dropper-applied and spin-on overcoats, layer of elastic material between the die and the plastic mold yields significant improvements, a cost that, depending on the application, may be worthwhile.

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Table 1. Package Characteristics [5].

MATERIAL	ELASTIC MODULUS (psi)	THERMAL EXPANSION COEFFICIENT $(^{o}C)^{-1}$
Plastic	1.6-2.0 x 10^{-6}	17-20 x 10^{-6}
Leadframe (copper)	17.5 x 10^{-6}	16.5 x 10^{-6}

Table 2. Package-Shift Statistics.

		SQUARE DIE ΔV_{BG}	RECTANGULAR DIE ΔV_{BG}	TRIMMED UNITS ΔV_{OFFSET}
NON-PLANARIZED	μ [mV] 3σ[mV] # of DUT	-5.06 7.92 18	-5.87 8.25 16	-5.1 10.8 27
PLANARIZED	μ [mV] 3σ[mV] # of DUT	-4.26 6.51 17		-4.9 10.34 32
SANDWICH LAYER	μ [mV] 3σ[mV] # of DUT	-2.26 4.14 10		-3.9 7.05 31

FIGURE CAPTIONS

Fig. 1. First-order Brokaw type bandgap reference.

Fig. 2. Normal and shear stress for one-quarter of the die (in 10^5 Pa).

Fig. 3. Filler-loaded plastic mold.

Fig. 4. Ratio of stressed to unstressed minority carrier density as a function of stress in silicon. Values are given for <000>, <111>, and <011> uniaxial compression stress [10].

Fig. 5. Systematic and random package shift: (a) normalized distribution before packaging for a bandgap reference trimmed to V_{BGo} within $\pm$ 1/2 LSB, (b) normalized distribution after packaging, and (c) desired distribution after packaging.

Fig. 6. Effect of systematic shift on the random component: smaller systematic shifts provide potentially smaller random components.

Fig. 7. Structural deformation of the die as a result of stress.

Fig. 8. Cross-sectional images of (a) non-planarized, (b) planarized, and (c) mechanically compliant layer ("sandwich layer") dies.

Fig. 9. Non-uniform stress field in non-planarized dies.

Fig. 10. Practical bandgap circuit used for measuring package shift.

Fig. 11. Rectangular and square die plots.

Fig. 12. Measurements of package shift offset (ΔV_{BG}) with temperature.

Fig. 13. Temperature variations of (a) V_{BG} before and after packaging,and (b) ΔV_{BG}.

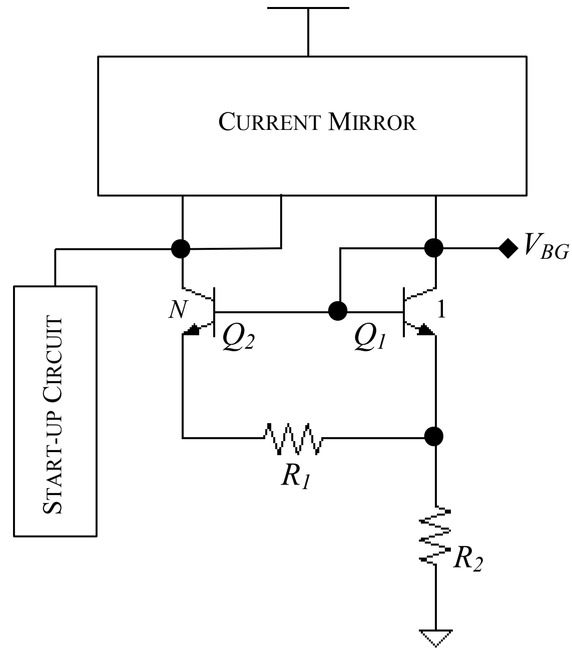

Fig. 1. First-order Brokaw type bandgap reference.

s_{xx}
s_{yy}
s_{zz}

Die Corner

-1788 -1762 -397	-2015 -1320 -95	-2080 -1278 -63	-1788 -1762 -397	-2148 -1271 -73	-2200 -1261 -74	-2235 -1266 -75	-2253 -1266 -76
-1783 -1661 +129	-1939 -1551 +39	-2028 -1476 +68	-1418 -1873 +98	-2100 -1451 +63	-2153 -1438 +64	-2188 -1431 +65	-2206 -1429 +65
-1711 -1775 +42	-1893 -1694 -56	-2016 -1610 -28	-1423 -1856 -88	-2102 -1571 -31	-2161 -1548 -30	-2199 -1536 -30	-2218 -1531 -30
-1679 -1821 +75	-1843 -1780 -34	-1971 -1703 -4	-1430 -1886 -65	-2066 -1659 -9	-2131 -1631 -8	-2172 -1615 -8	-2193 -1608 -8
-1688 -1856 +75	-1830 -1830 -36	-1953 -1761 -7	-1471 -1942 -77	-2050 -1720 -12	-2118 -1689 -12	-2162 -1671 -12	-2183 -1663 -11
-1694 -1880 +78	-1828 -1853 -37	-1945 -1788 -6	-1499 -1963 -72	-2042 -1748 -12	-2110 -1718 -11	-2155 -1699 -11	-2177 -1690 -11

Die Center

τ_{zy}
τ_{zx}
τ_{xy}

Die Corner

+614 -647 +624	+221 -230 +512	+250 -163 +329	+239 -134 +235	+238 -95 +167	+238 -65 +112	+239 -38 +64	+239 -12 +2
+203 -235 +491	+2 +7 +512	+19 +13 +375	+20 -4 +266	+21 -2 +187	+21 -2 +124	+21 -2 +71	+21 -1 +23
+121 -281 +284	-16 -6 +351	+5 +5 +291	+4 -14 +218	+6 -9 +154	+7 -8 +103	+6 -4 +59	+7 -1 +19
+100 -292 +175	+2 -5 +216	+3 -3 +195	+11 -13 +155	+13 -7 +113	+14 -6 +76	+14 -3 +43	+14 -1 +14
+69 -300 +95	+2 -5 +122	+7 -4 +110	+5 -16 +91	+7 -8 +68	+7 -6 +47	+7 -4 +27	+7 -1 +9
+22 -302 +27	+1 -2 +40	+2 -4 +35	+2 -15 +30	+2 -8 +22	+2 -6 +15	+2 -4 +9	-2 -1 +3

Die Center

Fig. 2. Normal and shear stress for one-quarter of the die (in 10^5 Pa).

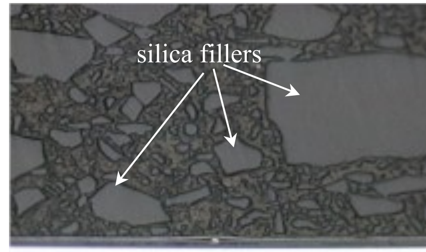

Fig. 3. Filler-loaded plastic mold.

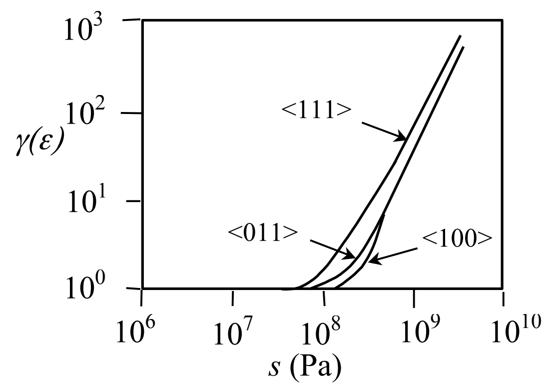

Fig. 4. Ratio of stressed to unstressed minority carrier density as a function of stress in silicon. Values are given for <000>, <111>, and <011> uniaxial compression stress [10].

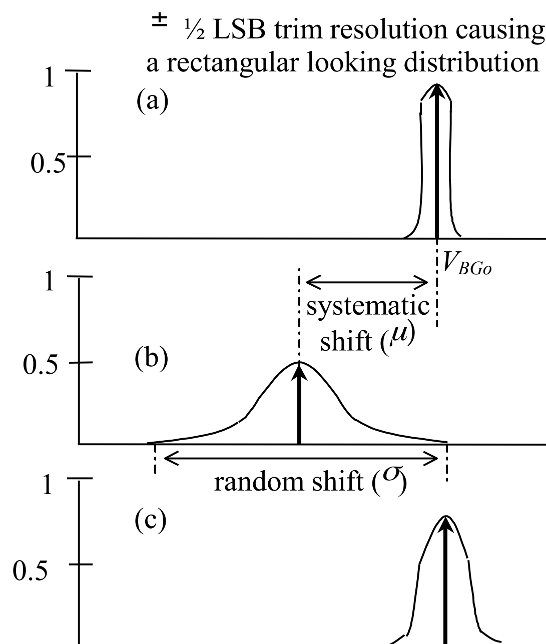

Fig. 5. Systematic and random package shift: (a) normalized distribution before packaging for a bandgap reference trimmed to V_{BGo} within ± 1/2 LSB, (b) normalized distribution after packaging, and (c) desired distribution after packaging.

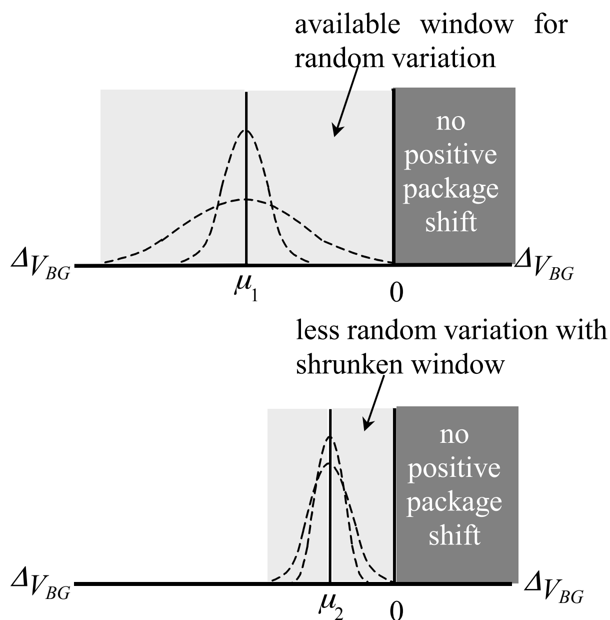

Fig. 6. Effect of systematic shift on the random component: smaller systematic shifts provide potentially smaller random components.

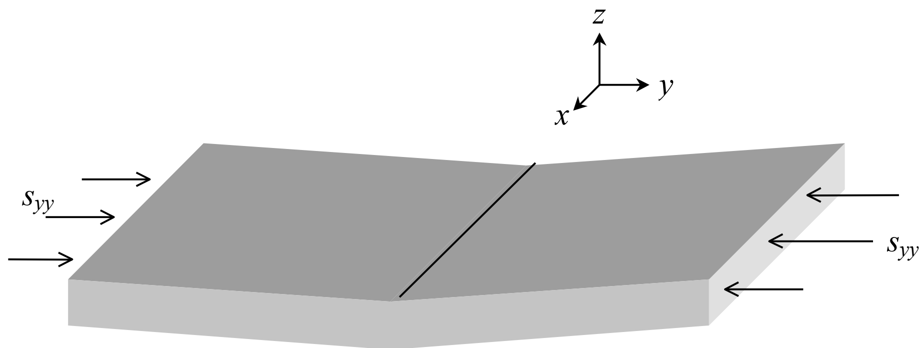

Fig. 7. Structural deformation of the die as a result of stress.

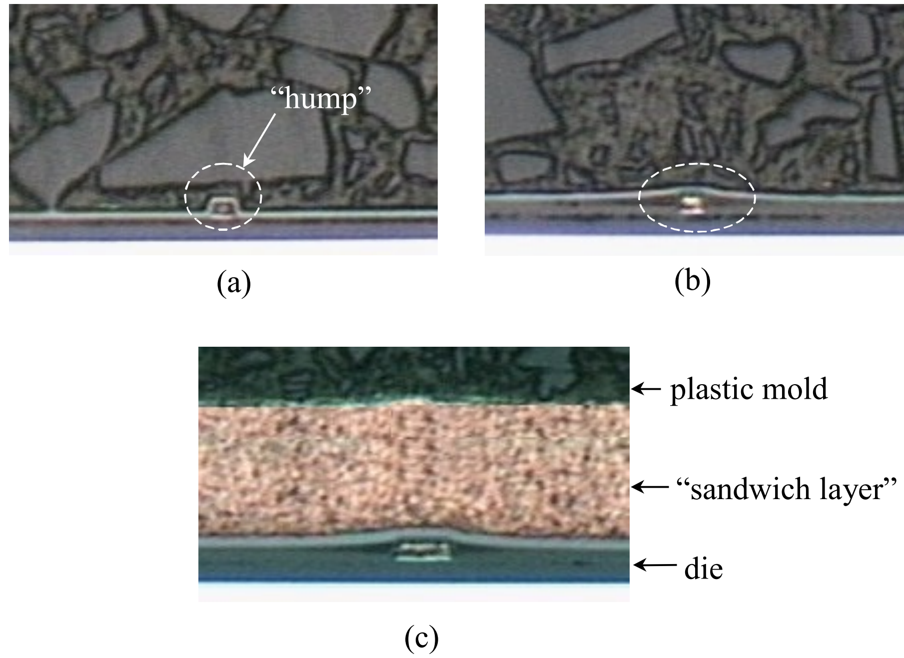

Fig. 8. Cross-sectional images of (a) non-planarized, (b) planarized, and (c) mechanically compliant layer ("sandwich layer") dies.

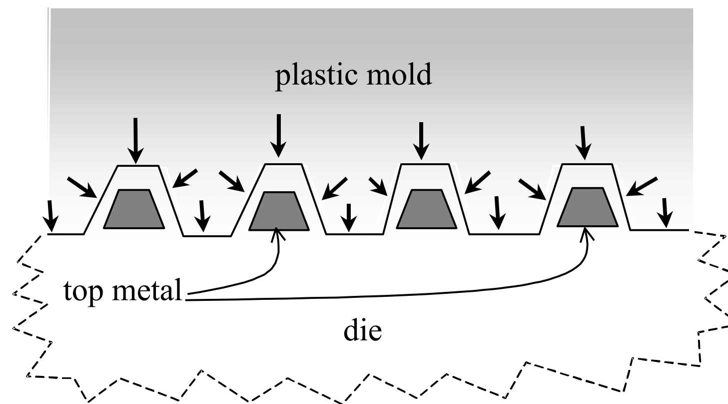

Fig. 9. Non-uniform stress field in non-planarized dies.

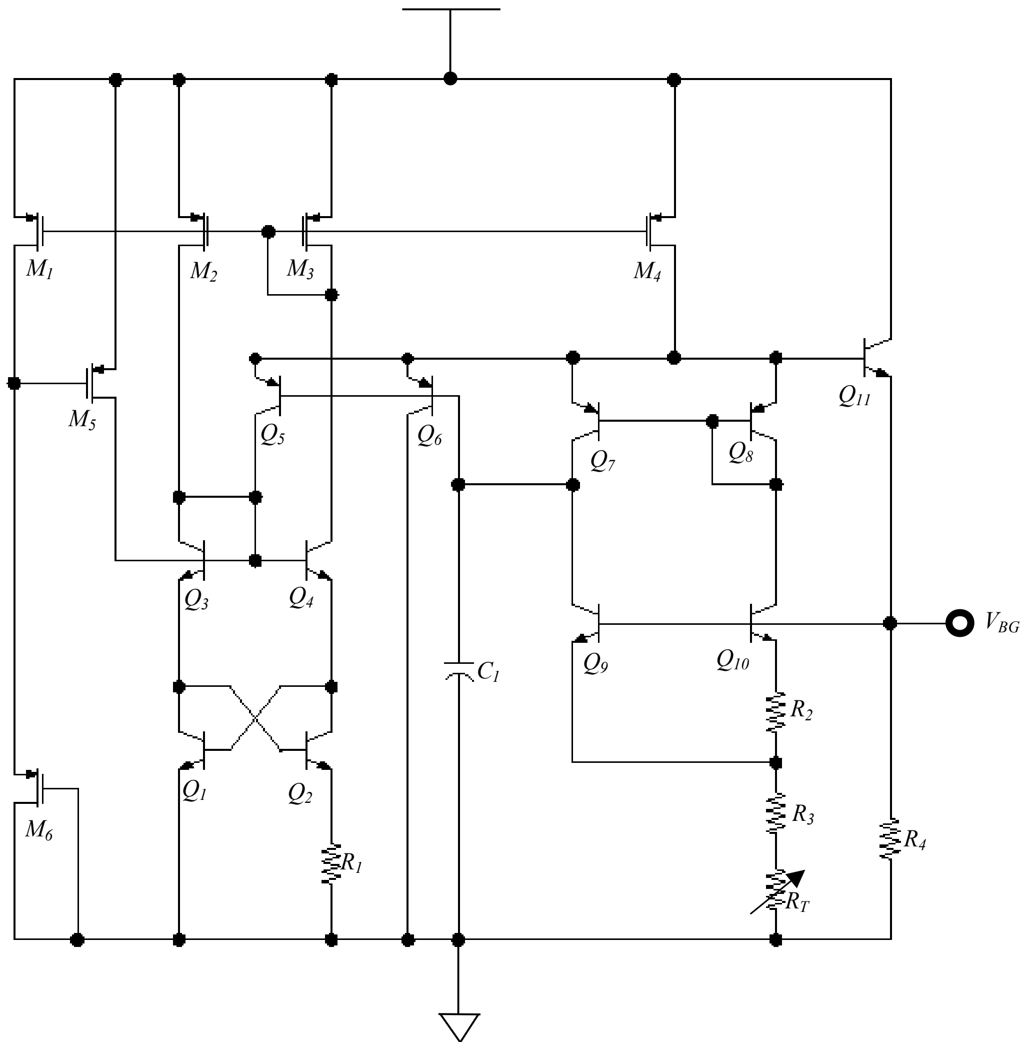

Fig. 10. Practical bandgap circuit used for measuring package shift.

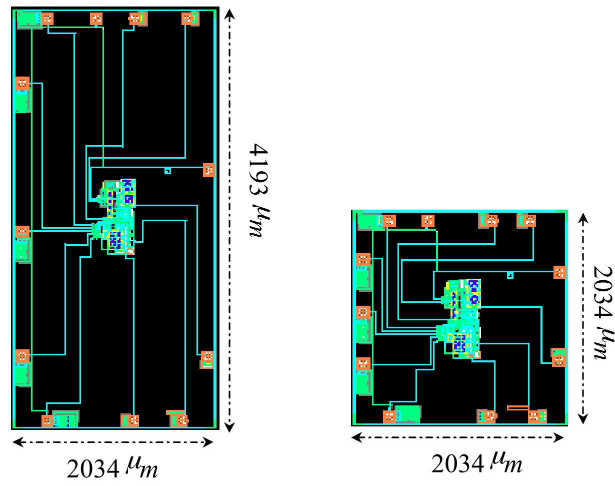

Fig. 11. Rectangular and square die plots.

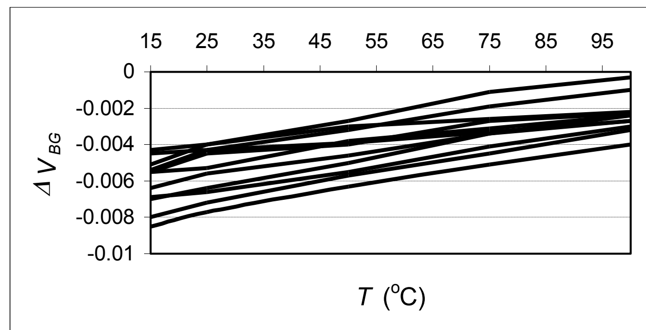

Fig. 12. Measurements of package shift offset (ΔV_{BG}) with temperature.

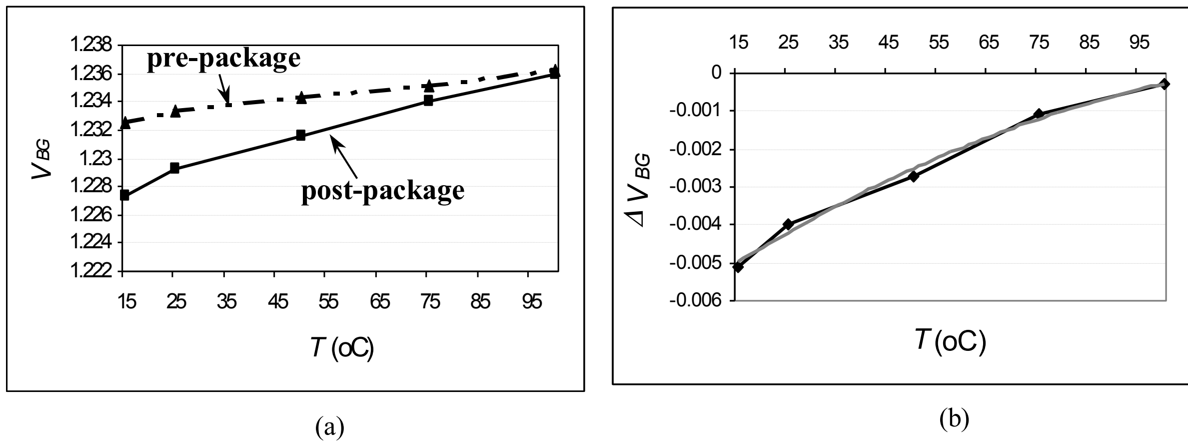

Fig. 13. Temperature variations of (a) V_{BG} before and after packaging,and (b) ΔV_{BG}.