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A user-friendly boost DC-DC converter topology - it's fast and widely stable

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In battery-powered applications, like cell phones, PDAs, digital cameras, etc., an integrated dc-dc converter circuit solution offers several advantages in terms of cost, size, and design complexity. A critical hurdle in obtaining a fully integrated solution is the frequency compensation circuit, which has to be designed based on the values of external passive filter components (L-C) and associated parasitic elements, like the capacitor equivalent series resistance (ESR). The values of these off-chip components vary due to manufacturing tolerances, parameter drift, and design requirements. Capacitor ESR can vary by orders of magnitude, based on whether the capacitor is electrolytic or ceramic, not to mention its variation across temperature. As such, it is required to have a DC-DC controller IC that can provide fast control and stable operation with widely varying passive component values. In hysteretic control for buck converters, the regulated output voltage includes inductor current ripple information sensed indirectly through capacitor ESR, thus simplifying the loop characteristics. This circuit displays an inherently stable performance and any change in L-C values is accommodated through a change in the converter switching frequency, maintaining stable operation without the use of frequency compensation circuits [1-2]. However, in boost converters, which are used for stepping up single or dual-cell battery voltages for 3.3 or 5 V applications, the technique is not readily applicable because the inductor current cannot be determined entirely from the output voltage. A strategy that overcomes this limitation in boost converters is presented in Figure 1 [3].

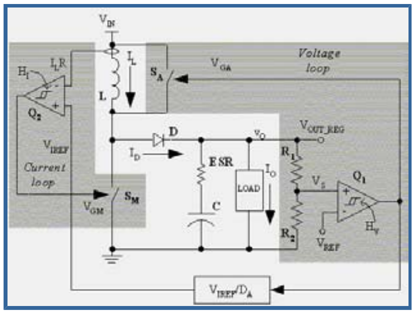


Figure 1a Simplified schematic of the proposed boost converter

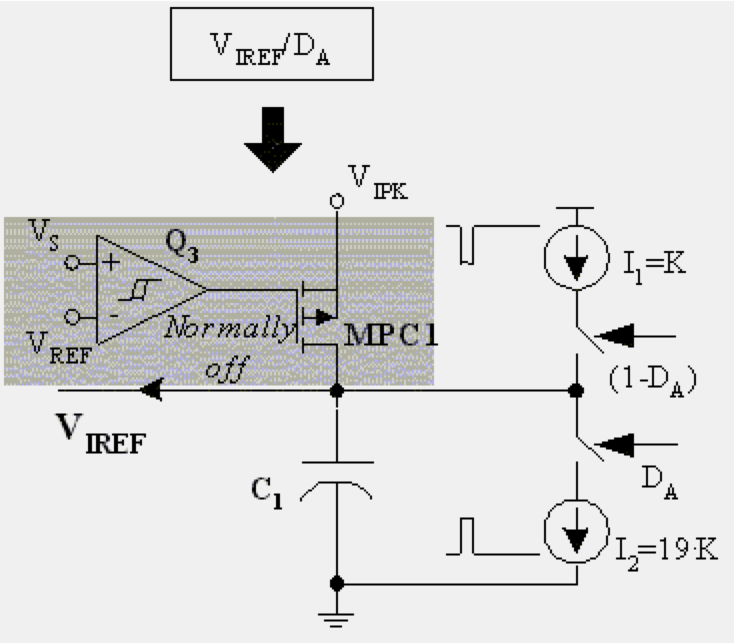


Figure 1b Duty cycle D_A to V_{IREF} demodulator

PROPOSED STRATEGY

The inductor current, which cannot be determined completely through the capacitor voltage ripple, is independently sensed and regulated through a separate hysteretic loop, containing the main switch S_M. The average inductor current I_L is raised above the minimum value required to support load current I_O. Starting with a standard boost converter, an additional auxiliary switch S_A is added across the inductor L. When the switch S_A is open, the excess inductor current (above the minimum value) tends to charge the capacitor C beyond the desired output voltage. This overcharge is sensed and prevented by comparator Q_1, which turns on switch S_A and shorts inductor L. Therefore, the inductor current freewheels, shutting off diode D and letting the capacitor voltage discharge. Switch S_A is turned back off when the sensed capacitor voltage V_S discharges below reference V_{REF}. The hysteretic problem is thus defined to regulate the output voltage to a desired value between (V_{IN} - V_{Diode}), which is its equilibrium value with switch S_A closed, and I_D (V_{OUT}/I_O), which is its equilibrium value with switch SA open. This regulation is performed by controlling the duty cycle D_A of switch S_A. At the appropriate duty cycle D_A, the diode current I_D, averaged over a switching cycle of S_A, equals the load current I_O, and average V_{OUT} is stabilized to equal V_{REF}. Switch S_A switches asynchronously to switch S_M at a much lower switching frequency.

The additional power loss due to higher inductor current is kept low by maintaining the inductor current only 5% above the minimum required value (I_{L_Min}). A representative inductor current reference (V_{IREF}) is derived from duty cycle D_A, by means of a charge-pump-based duty-cycle-to-voltage demodulator shown in Fig. 1b. Capacitor C_1 is charged and discharged by complementarily switching current sources I_1 and I_2, which are gated by the controlling signal of switch S_A. The average capacitor current equals zero and the voltage VIREF stabilizes when the total charge injected into the capacitor by I1 during the off time of switch S_A balances the total charge removed by I_2 during the on time of switch S_A. By setting I_2 to be 19 times larger than I_1, V_{IREF} reaches steady state only when the off time of S_A (I_1 charging C_1) is 19 times greater than the on time of S_A (I_2 discharging C_1), i.e., duty cycle D_A is 5%. If the steady-state duty cycle D_A is increased, the load transient response of the converter improves at the cost of reduced power efficiency. With duty-cycle D_A chosen as 5%, the efficiency of the proposed converter is degraded by approximately 2% as compared to a standard boost converter, at a load of 0.5A [3].

A fast, large increase in load current causes the output voltage to drop sharply because the inductor current is not high enough to support the increased load. Comparator Q_3 senses this voltage drop and turns on switch MPC1, thereby raising the inductor current reference to the level that is required to support the maximum designed load current. The inductor current rises, in a single cycle of switch S_M, to the new reference and then charges the output capacitor, in a single cycle of switch S_A, to V_{REF}. Once the output voltage reaches V_{REF}, switch M_1 turns off and the inductor current reference V_{IREF} decays until the duty-cycle D_A reaches the 5% limit. The comparator is designed with an asymmetrical hysteresis, being narrower than that of Q_2 on the positive side and wider than that of Q_2 on the negative side.

Simulated waveforms in steady state for the operating conditions tabulated in Table 1, are shown in Fig. 2a. The output voltage V_{OUT} and inductor current I_L are seen to have two ripples viz. a high frequency ripple corresponding to the switching of switch S_M and a larger, low frequency ripple corresponding to switching of switch S_A. Transient waveforms for a step load change from 0.3 to 0.6 A are shown in Fig. 2b. Simulations show that stable converter operation is obtained for capacitor (C) and ESR ranges of 3-200μF and 0-35mΩ respectively, under inductor (L) variation of 1-30μH at 1 A load. The acceptable ESR range is extended further at lower load levels.

Parameter	Value	Parameter	Value
V_{IN}	1-1.5 V	V_O	3.3±5%
I_O	0.1-1 A	L	2 μH
C	44 μF	ESR_C	20mΩ
S_M (N-ch) R_{ON}	0.1 Ω	S_A (N-ch) R_{ON}	0.1 Ω
D (P-ch) R_{ON}	0.15 Ω	I_1	1 μA
I_2	19 μA	C_1	3 nF
V_{OUT} H_V	25 mV	I_L hysteresis H_I	20 mV
M	0.364	R_s	0.1 Ω
Simulator	Spectre -S	Technology	0.5μ CMOS

Table 1. Simulation parameters and conditions

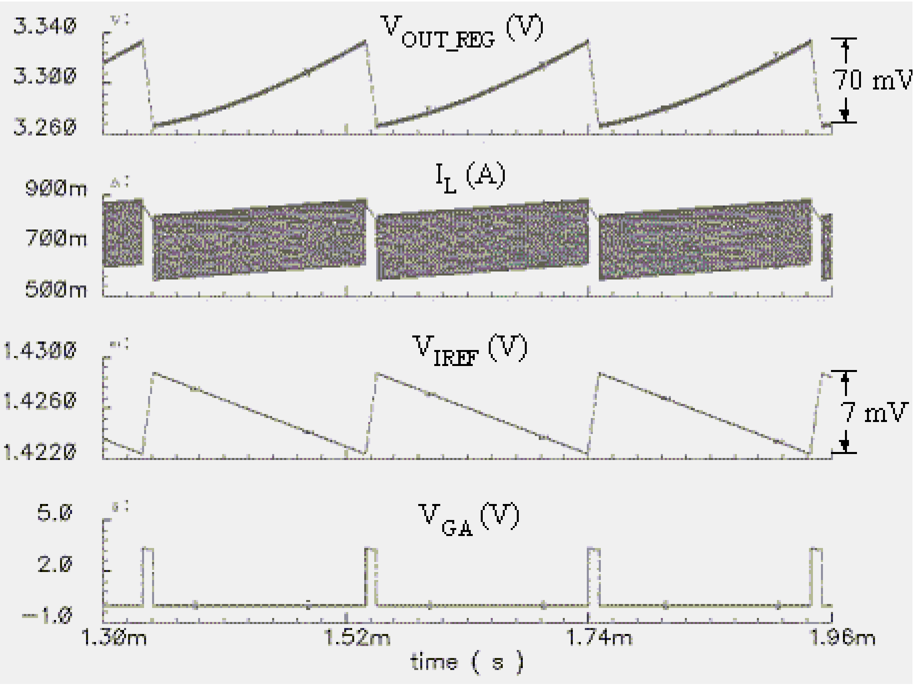
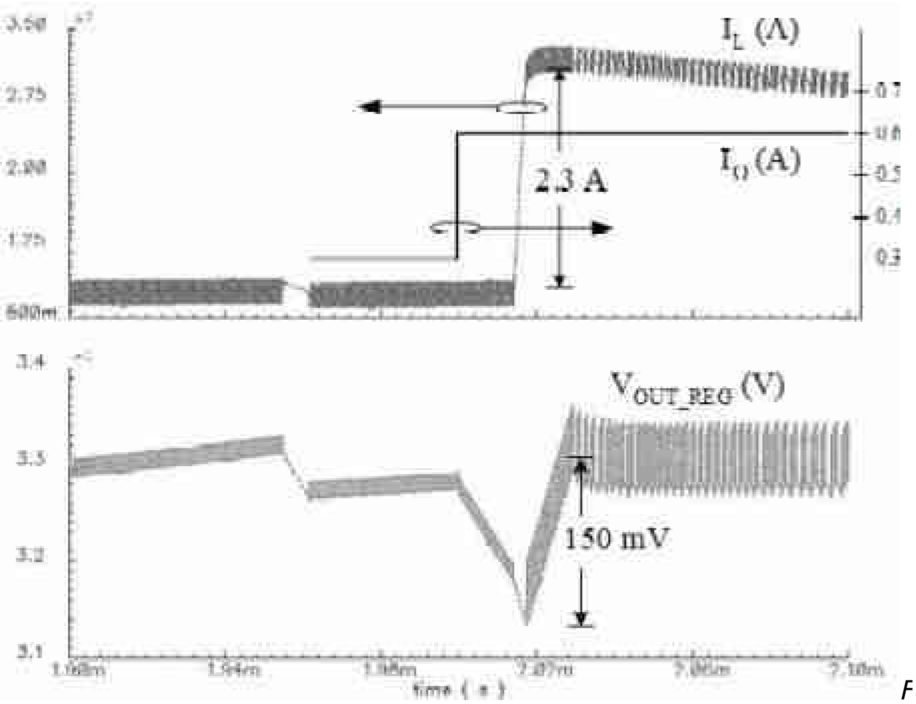


Figure 2a. Simulated waveforms in a steady state for the proposed circuit at V_{IN}=1.5V, I_O=0.3A, V_{OUT}=3.3V, f_{SW} (SA) =5kHz, $f_{SW}(S_M)$ =1.6MHz with three switching cycles

of switch S_A showing V_{OUT}, I_L, V_{IREF}, and V_{GA}



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2b. Step load from 0.3 to 0.6A, V_{IN}=1.5V, V_{OUT} = 3.3V showing I_L and V_{OUT}.

FUTURE WORK

The proposed technique provides stable performance and single-step transient response for a wide range of filter L-C values without the use of any external compensation circuit, thus suitable for integration. However, three main drawbacks are evident. Firstly, the output voltage has a somewhat large steady-state ripple at a low frequency, which may lie in the audible range; secondly, the additional switch S_A, which carries current in steady state, can be quite large in size, and, thirdly, the additional inductor current leads to a reduction in power efficiency. The future work in this research involves addressing all these concerns while maintaining the aforementioned benefits. Currently, a prototype board is being built to verify the simulations through experimental results and to determine the L-C compliance of the proposed circuit.

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[2] R. Miftakhutdinov, "Analysis of synchronous buck converter with hysteretic controller at high slew-rate load current transients," Proceedings of High Frequency Power Conversion Conference, 1999, pp. 55-69.

[3] N. Keskar and G.A. Rincn-Mora, "Self-Stabilizing, hysteretic, boost DC-DC converter," The 30th Annual Conference of the IEEE Industrial Electronics Society, IECON 2004, Nov 2004, TA3-4.

For additional details, questions, and/or comments on this article, please contact us, the Georgia Tech Analog and Power IC Design Lab, at gtap@ece.gatech.edu.

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