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Improve top-level simulation strategy for switching DC-DC converters

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Just before fabrication, the design flow of all integrated circuits (ICs) culminates in transistor-based, top-level simulations. Unfortunately, verifying functionality, connectivity, and performance with simulations tends to be complicated and cumbersome because of the growing mixed-signal complexity of state-of-the-art systems. A switching DC-DC regulator is such an example, where high performance analog and high power switching electronics interrelate and co-exist on the same bulk-silicon substrate. The resulting circuit complexity (for example, the number of equations to solve at each transient step of a simulation run) imposes serious challenges to the simulator and the computing platform supporting it. Typically, top-level simulations exceed 1,000 switching cycles, and that is just for start-up, incurring considerable CPU time in the process (for example, on the order of several hours and sometimes days) and therefore costly design time and time-to-market. Decreasing top-level simulation time, unfortunately, often implies sacrificing fault-detection coverage, in other words, implies adding risk to the project, which is why an optimized simulation strategy is presented.

The problem

Identifying and defining a market or research segment and application marks the beginning of a typical design cycle, establishing performance specifications for a target system. A suitable top-level system architecture is then designed and simulated using simple behaviorally based macro-models, after which specifications for each macro model (that is, sub-block) are generated. This part of the process constitutes the *system design* phase. At this point, transistor-level design, simulation, and verification of each sub-block against its specific target specifications are performed, both nominally and over process corners and temperature extremes. Since the simulations are relatively short, given the relatively low number of transistors used and the computing power of state-of-the-art computers, quasi-exhaustive verification is often achieved. Finally, before having the design fabricated (that is, before tape-out), all the sub-blocks are interconnected and simulated together, all with a transistor-based, top-level schematic.

Circuit verification is by nature an iterative process, whereby each problem found requires another simulation to ensure a proper fix is in place, and because of the complexity of a large transistor-based, top-level system, minor errors can cost days. Consequently, considering the competitive time-to-market nature of the semiconductor industry, most designers concentrate their efforts on exhaustive, transistor-level, sub-block designs and opt for simple transistor-based, top-level simulations to verify inter-block connectivity and basic system functionality [1-2]. That is to say, designers often sacrifice top-level verification for time-to-market, which is not ideal and sometimes costly.

Increasing Fault Coverage with Little Time Overhead

The basic premise of the foregoing top-level simulation strategy is that simulating more transistors together incurs more simulation time than using simpler macro models. The idea is therefore to use the all behaviorally based macro-model simulation used in the system-design phase and selectively replace each sub-block, one at a time, with its appropriate transistor-level circuit in the final verification phase, as shown in Figure 1, gradually transitioning from an all macro-model to a full transistor-level simulation. The sub-blocks that are first substituted must be the least time-consuming circuits to simulate, consequently fully debugging and verifying the connectivity and system performance parameters associated with that specific sub-block. Substituting the next least time-consuming sub-block, and keeping the first one in place, accomplishes similar goals for the new block. The process continues until all of the blocks are fully replaced with their circuit-level models.

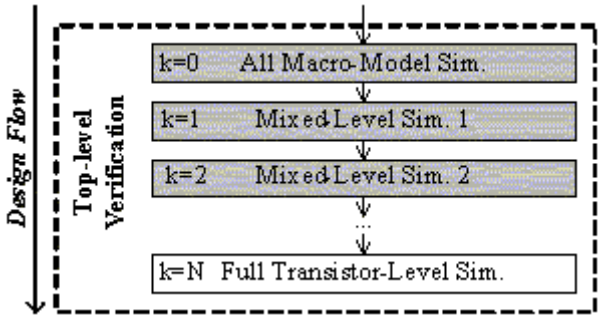

Figure 1. Proposed top-level verification sequence of a complex, k-block mixed-signal system

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The total expected simulation time of this strategy is the sum of the various intermediate simulations,

$$E\left(t_{Total\_Proposed}\right)=\sum_{k=0}^{N}\overline{m}_k t_{sim-k} \quad \textbf{(1)}$$

where $\overline{m}_1$ is the average number of iterations a circuit is simulated at each given step and t_{sim-k} is the simulation time of the k^{th} verification step in the top-level verification phase. The two extreme steps correspond to the all behaviorally based macro-model (k is zero) and all transistor-level (k is N) simulations, respectively. The total expected simulation time of the conventional approach (that is, a single, all transistor-based top-level simulation) is, on the other hand,

$$E\left(t_{Total\_Conv.}\right)=\overline{L}t_{sim-N} \quad \textbf{(2)}$$

where $\overline{L}$ is the average number of iterations the top-level circuit is simulated and t_{sim-N} is the simulation time of a single, all transistor-level run. Consequently, the basic goal of the proposed strategy is for its total expected simulation time to be equal or shorter than the conventional approach, noting that iterations are necessary to identify problems and verify solutions. The goal is that the number of iterations of the most time-consuming all-transistor circuit with the proposed strategy is low enough,

$$\overline{m}_N < \overline{L} \quad \textbf{(3)}$$

and the fault coverage of the overall sequence expansive enough to merit its use. Most errors, especially the ones resulting from connectivity, are typically found early with quick part macro- and part transistor-based simulations because t_{sim-0} is shorter than t_{sim-1}, which is in turn shorter than t_{sim-2} and shorter than any subsequent simulation, effectively decreasing the number of iterations required to simulate each successive step in the process (that is, $\overline{m}_0 > \overline{m}_1 > \ldots > \overline{m}_N$), the net result of which is a reduction in the iterations required to simulate the costly all-transistor circuit, as illustrated in Figure 2.

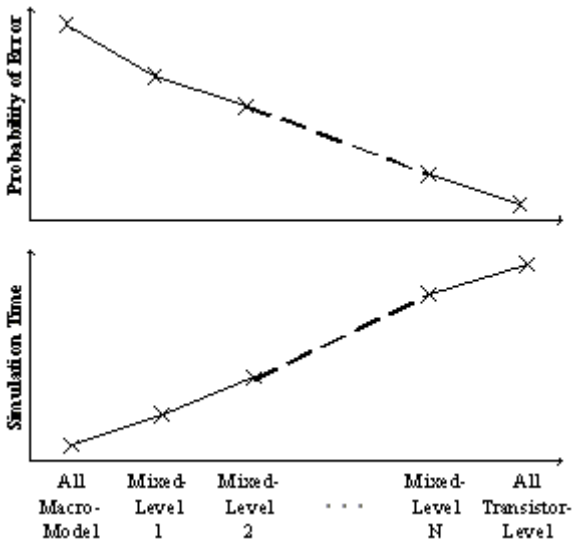


Figure 2. Probability of finding errors and expected simulation time of each step in the foregoing top-level verification strategy

In practice, however, each sub-block in a system affects full transistor-level simulations differently and only a select few tend to be mostly responsible for prolonged computational times [1, 3]. Therefore, verification time is minimized if less computationally intensive blocks are replaced earlier in the process. As a result, the optimal replacement order is one where each subsequent mixed-signal simulation time t_{sim-i} is the shortest possible out of all possible choices.

Determining the replacement order

To determine an optimized replacement order, a case study of a current-mode, pulse-width modulated (PWM) buck (step-down) DC-DC converter, shown in Figure 3, is presented and assessed within the context of simulation time [4-5]. Evaluating the resulting replacement order sheds insight into the computational needs of the various components comprising the mixed-signal environment, especially switching regulators, most of which have similar functional units like error amplifiers, bandgap references, drivers, control electronics, etc. The 0.5 µm CMOS switching regulator circuit shown was designed to convert a Lithium-Ion (Li-Ion) battery voltage (2.7 - 4.2 V) to a constant 1.5 V output voltage and source up to 1 A of load current at a switching frequency of 1 MHz. The complete design flow (that is, system and block-level design and top-level verification) was executed within a Cadence platform. After the design was finished, simulations were repeated to ascertain and record the simulation times and transient points of each mixed-level simulation step using Spectre on an Ultra 10 Sun workstation with *moderate* tolerance and *trapezoidal* integration settings.

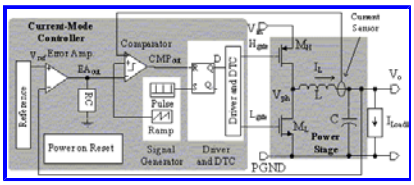
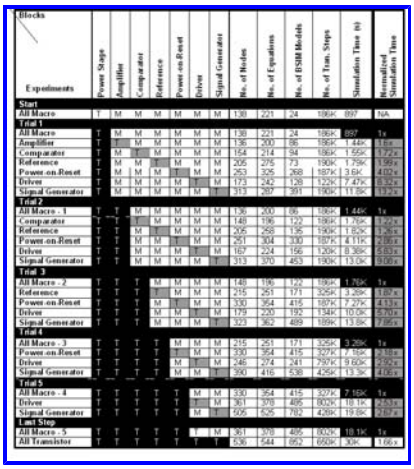


Figure 3. Current-mode buck (step-down) pulse-width modulated (PWM) switching regulator circuit used to evaluate the foregoing verification strategy

To ascertain an optimum replacement sequence, the least time-consuming block must be identified first. An all macro-model simulation of the system (with the exception of the power stage for which no behavioral model was used because of its low transistor count) was therefore performed, after which only one macro-model at a time was replaced (six simulations for six major circuit blocks), recording and comparing simulation times and performance characteristics against each other and the all macro-model simulation. This experiment showed that the error amplifier incurred the least simulation time, consequently defining the first replacement step in the foregoing verification sequence. For the second replacement, the transistor-based version of the error amplifier was used and the next least time-consuming block was then similarly identified by replacing each of the remaining macro-models with their respective transistor-level equivalents, one at a time. This process was repeated for every subsequent step in the replacement sequence, resulting in a total of 22 simulations, one for all macro models, six for the first step, five for the second, four for the third, and so on, the outcome of which is summarized in Table 1. The next least time-consuming replacement circuit was found to be the comparator, followed by the reference, power-on-reset, driver and dead-time control, and signal generator circuits.



Blocks / Experiments	Power Stage	Amplifier	Comparator	Reference	Power-on-Reset	Driver	Signal Generator	No. of Nodes	No. of Equations	No. of RSIM Models	No. of Tran. Steps	Simulation Time (s)	Normalized Simulation Time
Start													
All Macro	T	M	M	M	M	M	M	138	221	24	198K	897	NA
Trial 1													
All Macro	T	M	M	M	M	M	M	138	221	24	198K	897	1x
Amplifier	T	T	M	M	M	M	M	136	200	86	198K	1.44K	1.6x
Comparator	T	M	T	M	M	M	M	164	274	94	198K	1.56K	1.72x
Reference	T	M	M	T	M	M	M	205	275	73	190K	1.79K	1.99x
Power-on-Reset	T	M	M	M	T	M	M	253	325	268	187K	3.6K	4.02x
Driver	T	M	M	M	M	T	M	173	242	128	125K	7.47K	8.32x
Signal Generator	T	M	M	M	M	M	T	313	287	391	190K	11.8K	13.2x
Trial 2													
All Macro - 1	T	T	M	M	M	M	M	138	200	86	198K	1.44K	1x
Comparator	T	T	T	M	M	M	M	148	196	122	198K	1.76K	1.22x
Reference	T	T	M	T	M	M	M	205	258	135	190K	1.82K	1.26x
Power-on-Reset	T	T	M	M	T	M	M	251	304	330	187K	4.11K	2.86x
Driver	T	T	M	M	M	T	M	167	224	156	120K	8.36K	5.81x
Signal Generator	T	T	M	M	M	M	T	313	370	453	190K	13.0K	9.03x
Trial 3													
All Macro - 2	T	T	T	M	M	M	M	148	196	122	198K	1.76K	1x
Reference	T	T	T	T	M	M	M	215	251	171	325K	3.29K	1.87x
Power-on-Reset	T	T	T	M	T	M	M	330	354	415	187K	7.27K	4.13x
Driver	T	T	T	M	M	T	M	179	220	192	134K	10.0K	5.70x
Signal Generator	T	T	T	M	M	M	T	323	362	489	189K	13.8K	7.86x
Trial 4													
All Macro - 3	T	T	T	T	M	M	M	215	251	171	325K	3.29K	1x
Power-on-Reset	T	T	T	T	T	M	M	330	354	415	327K	7.18K	2.18x
Driver	T	T	T	T	M	T	M	246	274	241	276K	9.65K	2.93x
Signal Generator	T	T	T	T	M	M	T	390	416	538	425K	13.3K	4.04x
Trial 5													
All Macro - 4	T	T	T	T	T	M	M	330	354	415	327K	7.18K	1x
Driver	T	T	T	T	T	T	M	361	378	495	802K	18.1K	2.53x
Signal Generator	T	T	T	T	T	M	T	505	525	702	426K	19.8K	2.67x
Last Step													
All Macro - 5	T	T	T	T	T	T	M	361	378	495	802K	18.1K	1x
All Transistor	T	T	T	T	T	T	T	636	544	852	660K	30K	1.66x

Table 1. Case study results of the top-level replacement sequence for the proposed top-level verification strategy

The results of the study show that the transistor-level models of the signal generator and driver circuits account for approximately 60% of the total simulation time because of their high frequency glitch content, and this is in spite of the relative simplicity of the driver block, which has less transistors, nodes, and working equations than the reference and power-on-reset functions. The transistor-level models of the analog building blocks (that is, error amplifier, comparator, and reference) were only responsible for 11% of the total simulation time. Generally, linear analog blocks incur the least overhead, followed by nonlinear analog blocks like comparators and bi-stable bandgap references, low frequency digital circuits like power-on-reset functions, and finally high speed driver and signal generator circuits. Within these broad categories, computation time of course increases with the number of working nodes, that is to say, with the number of transistors and therefore number of equations. Although the optimum replacement order for this particular case study was found, the results can be extended to most switching DC-DC converters and generally to mixed-signal circuits.

Conclusions

Macro models are capable of predicting DC (power efficiency and load and line regulation performance) and transient response performance of switching regulators as accurately as all transistor-level models can, if the macro models are accurate behavioral depictions of their circuit equivalents. However, these macro models cannot verify other IC-related specifications like leakage, quiescent, and transient supply currents, all of which are sensitive to the individual junction diodes, loading capacitors, and input impedances present in the system. These parasitic devices load the various sub-blocks and sub-circuits of the system and consequently skew control and clocking signals, generating in the process undesired noise and short-circuit effects. Capturing and verifying that these real-life effects are within acceptable levels are the inspiration behind costly transistor-based, top-level simulations.

Unfortunately, a single, all transistor-level simulation in the case study presented took more than eight hours to complete, whereas the all macro-model counterpart took less than 15 minutes, which is why fault coverage is often sacrificed for shorter simulation times. However, by starting the top-level verification process with all macro-model simulations and replacing the least computationally intensive block with its transistor-level equivalent and performing another set of simulations, and replacing the next least time-consuming block, and so on, the computational time to fault coverage ratio is considerably reduced. That is to say, in the time that two or three errors are detected and their fixes confirmed with the traditional all transistor-based top-level simulation, the proposed macro-to-transistor simulation sequence can detect and confirm numerous errors and fixes.

For additional details, questions, and/or comments on this article, please contact us, the Georgia Tech Analog and Power IC Design Lab, at gtap@ece.gatech.edu. More information about our research can be found at http://www.rincon-mora.com/research.

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