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Can SoC switching regulators answer the challenge of their SiP counterparts?

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Inductor-based switching DC-DC converters are becoming increasingly important in the expanding world of battery-powered electronics. The driving advantage for this phenomenon is extended battery life, which results from high power efficiency. Switching noise, circuit complexity (i.e., silicon and board real estate, speed, and reliability), and integration of power passive devices, however, have limited their market penetration, especially when compared to linear low dropout (LDO) regulator topologies. Circuit designers, semiconductor manufacturers, and researchers are therefore working on reversing these trends, especially within the context of a single-chip solution, which is where power inductors and capacitors have the most impact.

In tackling the integration of power inductors, both system-on-chip (SoC) and system-in-package (SiP) approaches conform well to a single-chip environment, but will they yield similar performance at comparable costs? The fact is discrete, SiP-compatible power inductor technologies are relatively more mature than their SoC counterparts. Companies are therefore starting to co-package commercially available wound inductors that are on the order of micro-Henries and no wider or longer and only slightly taller than conventional power management dies [1-2]. The issue that remains is the relative electrical-cost performance of SiP and SoC solutions, the answer of which is shaping the nature and extent of current research efforts in SiP and SoC technologies.

SiP versus SoC

Today, it is common practice to integrate every active component in a switching regulator, including the power switches, on a single controller integrated circuit (IC), and the corresponding die need not be more than four or five square millimeters to efficiently deliver one to two amps of current. For the same range of currents, discrete inductors on the order of micro-Henries, as small as two millimeters on a side and one millimeter in height, are commercially available [3]. Co-packaging the controller and the inductor side-by-side can therefore have less than twice the dimensions of a package for the controller alone, as shown in Figure 1. This is significantly more compact than a printed-circuit board (PCB) realization of two discrete packages, where interconnect routing between the two also incurs additional overhead. The situation is further improved in smaller load-current applications, where power switches are smaller and switching at higher frequencies [4]. For these conditions, commercially available inductors with ferrite cores in traditional surface-mount packages have even smaller footprints [5].

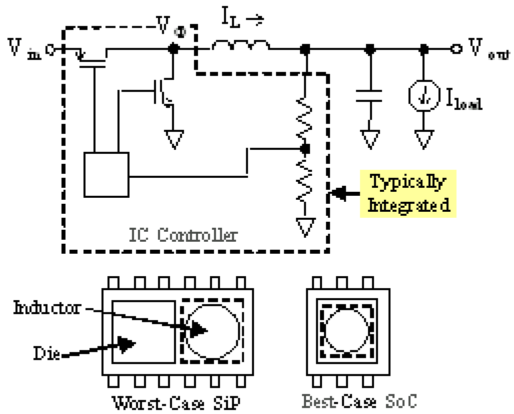

Figure 1. (a) Typical IC controller and accompanying power passives, (b) system-in-package (SiP), and (c) system-on-chip (SoC) switching regulator solutions.

The fact that only a few products thus far feature co-packaged inductors is no indication that co-packaging costs are prohibitive. In fact, no additional fabrication step is required that is more complicated than the stacked die memory solution already in volume production for cellular handsets [6], only a few more bond-wires to an adjacent inductor are necessary. As it turns out, power management companies have a growing interest in stacked die integration because integrating the power switches in different process technologies can potentially decrease noise injection and the loading capacitances of the noise-sensitive controller, thereby improving its noise, bandwidth, and transient-response performance. In a die-stack environment, the height of the in-package inductor, which can be as low as one millimeter, would actually be shorter than the die stack.

SoC inductors have, on the other hand, found a niche in RF applications, but not so in power ICs. The two major drawbacks are (1) the lack or use of a poor electromagnetic core and (2) the limited thickness and dimensions of the copper material used to build it. The end result is a less than 100 nH inductor with a low saturation threshold and poor Q performance, all of which fall short of the stringent filter, load-current range, and efficiency demands of emerging battery-powered devices. The fact is any processing step and material available for SoC integration is also available for manufacturing a discrete, SiP-compatible inductor. Consequently, SoC inductors can by no means outperform their SiP counterparts. They can, however, reduce the footprint of the package, but by at most a factor of two, as shown in Figure 1(c). It is difficult to argue against the merits of SiP inductors, except to say that complex, functionally dense systems may require several switching regulators, in which case the SiP approach may be limited to only a few.

SoC inductors may, however, present unique opportunities in the form of *custom, application-specific* devices. While discrete inductors are built to perform at acceptable levels for a wide range of currents and frequencies and presumed useless beyond the onset of saturation, integrated inductors can be tuned and their corresponding inductances, resistances, and frequency ranges balanced according to the particular needs of a given application, much like speed and power are balanced in an operational amplifier. Even more appealing is the possibility of intentionally incorporating saturation effects into the design for flexibility, speed enhancements, and tunability, a region that is seldom characterized or even reported in literature and datasheets.

Recent work on integrated inductors reveal a strong dependence on frequency and current over their entire practical range, as shown in Figs. 2(a) and 2(b), where inductance decreases with increasing operating frequencies and increasing currents. With the electrical characteristics in the hands of circuit designers, these saturation effects can be adapted to enable new features. A single inductor that decreases rapidly with frequency, for instance, can be used as a large inductor as well as a small inductor by simply changing the switching frequency of the converter. It can also hold the ripple current low during steady-state conditions and saturate (i.e., decrease to a lower inductance value) in response to fast load-dump events, in which case the LC complex-conjugate pole-pair and therefore the system bandwidth shift to higher frequencies, as illustrated in Fig. 2(c). Finally, just to cite another example, current-sensing techniques that were previously flawed by their dependence on unpredictable inductance and/or resistance values might be revisited in light of a tunable inductor.

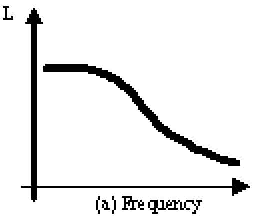

Figure 2a. Saturation effects of an SoC inductor with respect to frequency

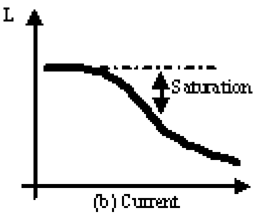

Figure 2b. Saturation effects of an SoC inductor with respect to current

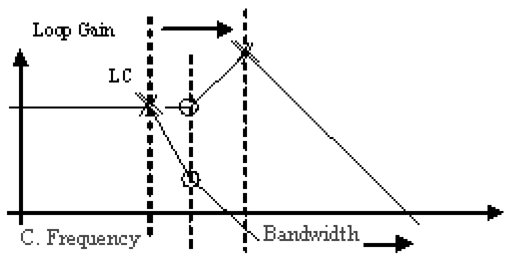

Figure 2c. Saturation effects of SoC inductor in the context of a buck DC-DC converter, where LC and bandwidth shift to higher frequencies during load-dump events

Custom, *saturable* SoC inductors offer interesting opportunities for the IC designer, but when it comes to sheer inductance and Q performance, SiP solutions will continue to outperform them. The fact is SiP-compatible technologies are mature and cost-effective today, unlike SoC power passive devices. The custom features of integrated inductors will more than likely, if anything will, distinguish SoC regulators from their SiP counterparts. For now, however, with only integration and power as criteria, the form-factor, performance, maturity, and cost of SiP inductors overshadow the promises of SoC solutions.

For additional details, questions, and/or comments on this article, please contact us, the Georgia Tech Analog and Power IC Design Laboratory, at gtap@ece.gatech.edu. More information about our research can be found at www.rincon-mora.com/research.

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