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# Fooling Faraday: On-chip capacitor multipliers

**Capacitor-enhancing circuits may be what you need as an alternative for your designs because their complexity is low, saving precious real estate.**

By *Gabriel A. Rincón-Mora, Senior Member, IEEE, and Justin Vogt, Student Member, IEEE, The Georgia Tech Analog and Power IC Design Laboratory*

One of the most, if not the most, basic component of any power management system is the capacitor. It serves three functions:

1. Shape frequency response
2. Store energy
3. Deliver current instantaneously

While the first two functions are essential to switching power supplies, the latter has universal applications. Mixed-signal circuits, for instance, typically incur clock-synchronized load-current events that are faster than any active power supply circuit can supply, and do so while only surviving small variations in voltage. The result of these transient current excursions is noisy voltages, be they supply lines or data links. Capacitors are used to mitigate these effects, to supply and/or shunt the transient currents the power supply circuit is not quick enough to deliver, which is why a typical high performance system is sprinkled with many nano- and micro-Farad capacitors.

The demand for many capacitors is not necessarily prohibitive, but each capacitor incurs cost and printed-circuit board (PCB) real estate. System-on-chip (SoC) integration alleviates this overhead by absorbing the capacitors and a significant portion of the system into a single chip. Unfortunately, however, on-chip capacitors also occupy silicon real estate, and implementing nano- and micro-Farad capacitors is more often than not unaffordable and impractical, especially when considering the number of capacitors required in a high performance microelectronic system. The filter density of a typical sub-micron CMOS process, for example, is on the order of 1 fF/$\mu m^2$, yielding a practical capacitance ceiling of approximately 100 pF and occupying 0.1 $mm^2$ of silicon die area. The problem is not only that 100 pF is impractically low for many supply circuits but it also requires a significant fraction of the overall silicon die -- the same area could maybe fit 100 uncompensated operational amplifiers. Increasing filter density, that is to say, capacitance per unit area, requires the use of exotic dielectric materials, which are too expensive for volume, cost-effective solutions.

The designer is consequently left with only a few choices:

1. Use and pay for external capacitors and limit the overall foot-print of the system,
2. Use and pay for exotic process technologies
3. Mitigate the need for capacitors.

Although deceptively simple and obviously attractive, the third option is difficult to realize. Circuits, and in the case of power management, regulators must be designed to respond quickly to offset the need for fast responding capacitors, but they can only do so much. A 25 mA load dump, for instance, in the presence of a 10 MHz supply circuit, which takes 100 ns to respond, in combination with a 1 nF capacitor can incur up to 2.5 V of variation, if unclamped. The fact is that speeding up a supply feedback circuit comprised of many ac nodes, as is the case for most supply circuits, is not trivial, and doing so requires current, which cannot be freely afforded in battery-powered devices. Capacitor-enhancing circuits

(that is, multipliers) have therefore emerged as working alternatives because their complexity is relatively low, in terms of AC nodes and compensation requirements, and speed consequently high.

**Capacitor Multipliers**

Capacitor multipliers essentially enhance the capabilities of on-chip capacitors with active components (that is, transistors). There are two fundamental limitations to this approach:

1. Energy storage cannot be improved and
2. Current cannot be supplied instantaneously.

With regard to the foregoing discussion of rapid load dumps and noise-shunting capabilities, and its system performance implications, the latter limitation is more limiting than the former. In other words, in the presence of fast changing currents, for which the regulator is already too slow, the capacitor multiplier requires finite time to react. If, for instance, an instantaneous 25 mA load dump were to be presented to a 10 MHz supply circuit, like before, except the 100 pF output capacitor is multiplied 100 times with a 1 GHz circuit, the initial 1 ns voltage incursion would be about 250 mV and the 100 ns response an additional 0.25 mV, which is an order of magnitude better than the scenario presented earlier, which had no capacitor multiplier. In practice, however, the load dump is not instantaneous but on the order of 10 to 100 ns, which relaxes the 1 GHz multiplier requirement. In the end, the key performance parameters of a capacitor multiplier are bandwidth and multiplication factor.

As with most circuits, capacitor multiplication can also generally fall into three categories: voltage-, current-, and mixed-mode circuits. If for instance, the voltage at the low impedance terminal of a capacitor opposes the direction (for example, increases) of its input terminal (for example, decreases) in the presence of a load dump, the capacitor can discharge (that is, slew) without significantly changing its input voltage (that is, $\partial vi/\partial t$ is lower than $\partial vC/\partial t$), when referenced to ground. This is the well-known Miller effect, where an inverting voltage amplifier is connected across the terminals of a capacitor, as shown in Figure 1. The slewing voltage at the low impedance terminal of the capacitor (output of the voltage amplifier) therefore opposes input terminal vi, but with a gain:

$$I_{LD} = C\frac{\partial v_c}{\partial t} = C\frac{\partial\left(v_i - \left[-Av_i\right]\right)}{\partial t} = C(1+A)\frac{\partial v_i}{\partial t} = C_{eff}\frac{\partial v_i}{\partial t} \quad \textbf{(1)}$$

where $I_{LD}$ is the transient load current, $v_c$ the voltage across capacitor C, A the gain of the operational amplifier, and $C_{eff}$ is the effective capacitance seen at vi when referenced to ground, which in this case is equivalent to C(1+A), an amplified version of C. Two key features to this scheme are high gain (100-$10^3$) and low equivalent series resistance (ESR). Its drawback, however, is limited dynamic range because the amplified voltage cuts into the available headroom of the circuit. For instance, a switching converter with a systematic 25 mV ripple that is loaded with a 40 dB multiplier incurs a 2.5 V systematic ripple at the output of the amplifier, which leaves little headroom for load-current events (e.g., the amplifier may saturate and yield little gain when supplied from a close-to-drained lithium-ion battery, whose voltage can be 2.7-3 V).

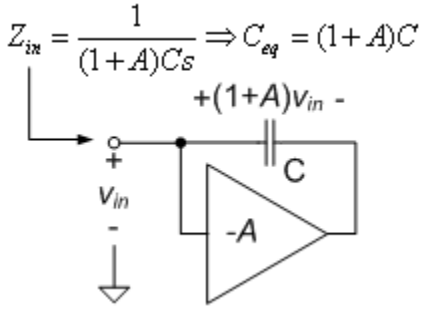


*Figure 1. Voltage-mode (Miller) capacitor multiplier*

The key advantages of current-mode processing are dynamic range and speed because no voltage variations are needed and consequently no additional current is required to charge and discharge internal nodes. In essence, a current-mode multiplier senses the capacitor displacement current (ic), multiplies it with a current amplifier (by a factor B), and supplies or sinks it back to the input, as shown in Figure 2(a) [1]. While the voltage across the capacitor may slew with $i_c$, the total current supplied or sunk is $i_c(1+B)$, in other words, the voltage variation corresponds to a fraction of the current actually sourced or shunted:

$$C_{eff} = \frac{I_{LD}}{\left(\frac{\partial v_c}{\partial t}\right)} = \frac{I_{LD}}{\left(\frac{I_{LD}}{C(1+B)}\right)} = C(1+B) \quad \textbf{(2)}$$

The main drawback to this circuit is moderate gain because currents are not as easily multiplied in current-mode fashion and moderate power efficiency because multiplied currents are drawn from the power supplies.

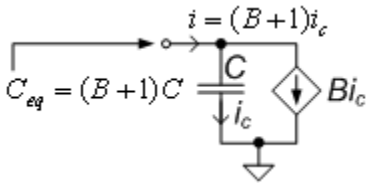


*Figure 2. (a) General circuit implementation of a current-mode capacitor multiplier*

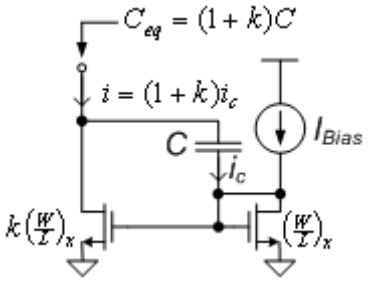


*Figure 2. (b) Current-mirror based circuit implementation of a current-mode capacitor multiplier*

Figure 2(b) shows a simple embodiment of how the capacitor displacement current can be sensed via a diode-connected transistor and amplified by a matching mirroring device with an aspect ratio that is k times larger. Bias current $I_{Bias}$ is used to bias the MOSFETs and allow the circuit to freely source or sink ac currents. Without $I_{Bias}$, the circuit would only be able to sink ac current and would do so only when enough gate-drive is at the gates of the mirroring devices, causing a non-linearity in its response in the form of a sharp voltage incursion equal to an overdrive voltage above the threshold voltage. Increasing the gain, unfortunately, incurs additional power losses because the bias current is also multiplied by the amplifying mirror. The ac sourcing capability of the circuit is determined by the bias current, when the input current channels away $I_{Bias}$ from the diode-connected device and whatever current was biasing the output of the mirror is available for the load. A complementary p-type version of the multiplier can be implemented to offset this limitation. As a side note, the diode-connected device introduces an ESR equal to its transconductance. The ESR value can be decreased by inserting a gain in the negative feedback loop connecting the gate and the drain of the diode-connected device, which of course increases circuit complexity and power requirements.

Figure 3 shows an improved implementation of the current-mode capacitor multiplier whereby a voltage gain transformation is inserted into the current-multiplying path [2] in such a way that some of the non-idealities of the previous circuit are circumvented. Transistors M1 and M2 comprise the diode-connected device (M1 is simply a source-follower transistor). The ac input current is therefore displaced through M1 to high impedance point $R_y$, transforming the current into a voltage that is then converted back into a current by transconductor $G_m$. Devices C, M1, and Gm comprise a negative feedback loop that does whatever is necessary to ensure the voltage at the drain of M1 is equal to $V_{Bias1}$ ("virtual" short), to ensure M1 is well within its saturation region. This implementation, unlike its simpler predecessor, decouples $I_{Bias}$ from the sourcing and sinking capabilities of the overall circuit, without having to build a p-type complementary circuit. Gain, which is the product of $R_y$ and $G_m$, is also decoupled from power through $R_y$, since it can be increased by decreasing the bias current flowing through M1, which is set by $V_{Bias3}$. In summary, this circuit enjoys bidirectional linearity because the output current is linearly proportional to the sourcing or sinking input current. The drawback of the circuit is relative speed, when compared to the simpler circuit shown in Figure 2(b), because there are more AC nodes and consequently more poles and delays across the current-amplifying path.

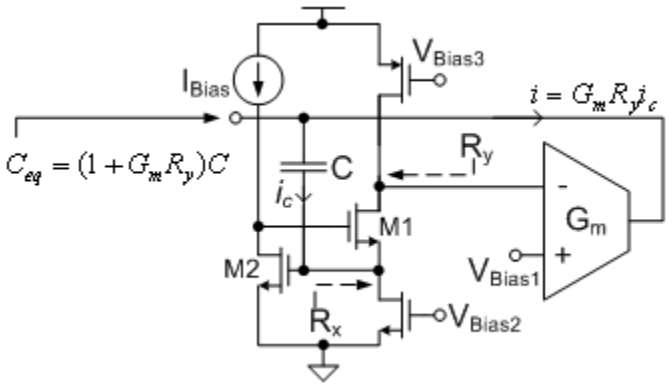


*Figure 3. Linearly bidirectional current-mode capacitor multiplier*

The current-mode circuit, in basic terms, senses a current and feeds back a current while the voltage-mode counterpart senses a voltage and feeds back a voltage. The mixed-mode circuit, on the other hand, senses a voltage and feeds back a current, much like the current-mode circuit, except the sensing element is a voltage. This is readily implemented with a current conveyor, which, in practical terms, is nothing more than a zero-threshold MOS transistor (Figure 4) [3]. Like the gate and source of a MOSFET, input terminals Y and X are high and low impedance, respectively, and like the drain, output terminal Z is high impedance. As a source voltage follows its gate's, the voltage at X follows that of Y, except there is no threshold voltage overhead across the two terminals, and the current flowing through Z (that is, drain) is equal to that of X (that is, source). In general terms, however, a current conveyor may also amplify the Y terminal voltage by a factor A before superimposing it to X and multiply the X current by B before sourcing or sinking it into Z.

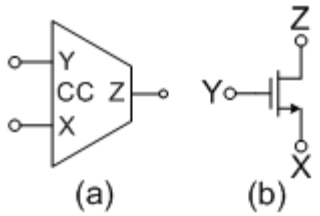


*Figure 4. (a) Current conveyor and (b) its simplest transistor embodiment*

Muck like the current-mode circuit, capacitor multiplication is achieved by pulling an amplified version of the capacitor displacement current, except in this case the capacitor is not directly connected to the input, but its voltage does follow the input, as shown in Figure 5(a) [4]:

$$C_{eff} = \frac{I_Z}{\left(\frac{\partial v_Y}{\partial t}\right)} = \frac{BI_X}{\left(\frac{\partial v_X}{A\partial t}\right)} = (AB)C \quad \textbf{(3)}$$

where $C_{eff}$ is the effective capacitance of the multiplier, $I_Z$ the output current of the conveyor and the total current flowing into and out of the multiplier, $v_Y$ and $v_X$ the Y and X voltages, respectively, and A and B the voltage and current gains of the current conveyor. Figure 5(b) is a simple extension of 5(a) using two current conveyors with unity voltage and current gains (that is, A and B are 1) to define an overall ratio-metric voltage gain, that is to say, a ratio-metric capacitor multiplication factor:

$$C_{eff} = \frac{I_{Z2}}{\left(\frac{\partial v_{Y1}}{\partial t}\right)} = \frac{I_{X2}}{\left(\frac{\partial v_{X1}}{\partial t}\right)} = \frac{I_{X2}}{\left(\frac{R_1 \partial v_{Y2}}{R_2 \partial t}\right)} = \frac{I_{X2}}{\left(\frac{R_1 \partial v_{X2}}{R_2 \partial t}\right)} = \frac{R_2}{R_1}C \quad \textbf{(4)}$$

where $R_2/R_1$ is the voltage gain from $v_{X1}$ to $v_{Y2}$. The key advantages of this type of circuit are low ESR and high overall gain, on the order of 100[3] for the circuit shown in Figure 5(b), especially when current gains are introduced into the current conveyors (i.e., $C_{eff} = C[B_1B_2R_2/R_1]$). Gain and power are decoupled by adjusting $R_2$.

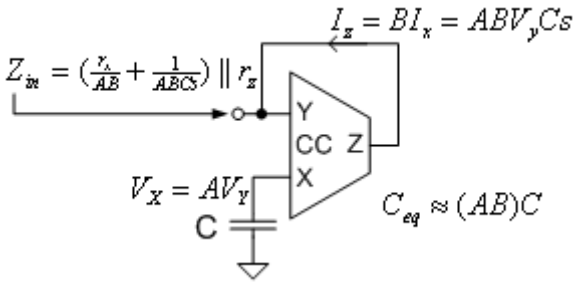


*Figure 5. (a) One-stage current-conveyor capacitor multipliers*

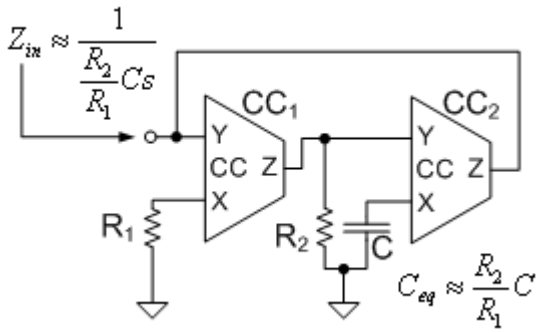


*Figure 5. (b) Two-stage current-conveyor capacitor multipliers*

**Summary**

The most important attributes of a capacitor multiplier are speed, gain, and the absence of parasitic devices, such as equivalent series resistances (ESRs). Although voltage-mode multipliers enjoy high multiplication factors ($1^3$ -$10^3$), low ESRs, and good power efficiencies, they suffer from dynamic-range limitations because input voltage variations are ultimately multiplied by a voltage gain. Current-mode circuits enjoy the benefits of high speed and extended dynamic range because they do not have to charge or discharge internal node voltages, but they suffer from limited gains (10-100), finite ESRs, and moderate efficiencies. Current-conveyor-based mixed-mode circuits, like their voltage-mode predecessors, have low ESRs, and like their current-mode predecessors, high speed and high dynamic range, if no voltage gain is included. In practice, current-conveyors do not necessarily outperform their predecessors, but rather give the designer more design tradeoffs to play with. A current-conveyor multiplier can be simple and therefore high speed, with low ESR and moderate gain, or multi-stage and consequently low speed with moderate-to-low power efficiency and low ESR, but high gain.

For additional details, questions, and/or comments on this article, please contact us, the Georgia Tech Analog and Power IC Design Laboratory, at gtap@ece.gatech.edu. More information about our research can be found at http://www.rincon-mora.com/research.

**References:**

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