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A fast, accurate, LC compliant DC-DC boost regulator…Is it possible?

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With an ever-rising demand for portable and compact electronics, circuit integration has become the key trend in the electronics industry. From the power management standpoint, the frequency compensation circuit is a critical roadblock, since its design is based on off-chip LC filter components [1]. Since the values of these LC filter parameters can vary significantly because of various performance requirements, manufacturer tolerances, and/or parameter drift issues, integration of a fixed compensation circuit implies low bandwidth, in other words, poor load transient response, which is vital in portable applications with fast switching loads like microprocessors, motors, and the like. And in boosting supply applications, because of their special frequency compensation needs (for example, right-half plane (RHP) zero in boost DC-DC converters), the limitations set to enhance LC-filter compliance are even more pronounced. A user-friendly, accurate, fast, highly LC-tolerant supply circuit is therefore in high demand.

Sliding-mode or single-loop sigma-delta (ΣΔ) control mixes the inductor current and output voltage information in a single loop, almost like a current-mode converter, giving stable, widely LC-compliant operation without using a frequency compensation circuit because the inherent current loop makes the inductor look like a current source and the LC complex-conjugate pole effectively disappears. However, for filter LC components potentially varying by orders of magnitude, the power path bandwidth is at its lowest point at the worst-case LC filter combination (i.e., highest L and highest C). As a result, the control path must be low bandwidth, deteriorating the circuit's ability to respond quickly to transient loads [2].

A dual-loop ΣΔ technique that controls the inductor current and output voltage using independent ΣΔ loops was reported earlier in [3]. The circuit responded within one clock cycle, which is why it was fast, but the switching of the main loop had to be slower than the internal loop and the slower loop forced the output voltage ripple to be relatively high, in the order of 100 mV. The circuit did achieve wide LC compliance and fast transient response, but at the cost of steady-state accuracy (i.e., higher ripple voltage) and reduced high-load efficiency. A single loop is consequently attractive for steady-state accuracy but unappealing for speed.

A Bypass ΣΔ Approach…

To combine the positive attributes of both single- and dual-loop solutions, a hybrid approach is proposed, whereby a single ΣΔ loop is used for steady-state operation (good steady-state accuracy), bypassing it via a fast-responding ΣΔ path only when the load demands it, during fast transient events, achieving both LC compliance and high effective bandwidth (Figs. 1(a) and (b)). The main loop has high gain and low bandwidth and its function is to achieve high steady-state accuracy under widely variable LC conditions. The bypass path, on the other hand, has low gain and high bandwidth and its function is to respond quickly to fast-moving loads under widely variable LC conditions. This bypass path is threshold-based, set by Q_1 in Fig. 1(b), actuating only when the output voltage surpasses passable window limits. The proposed solution is effectively a sliding-mode ΣΔ controller during steady state and a dual-loop ΣΔ controller during fast transient load conditions.

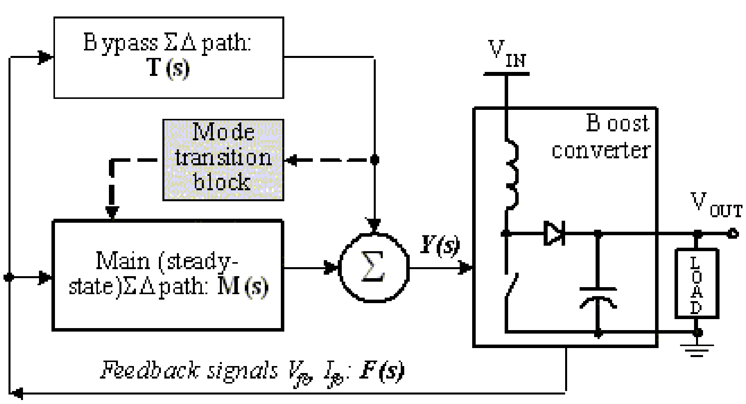

Figure 1a. Proposed accurate, fast, LC compliant boost converter:- block

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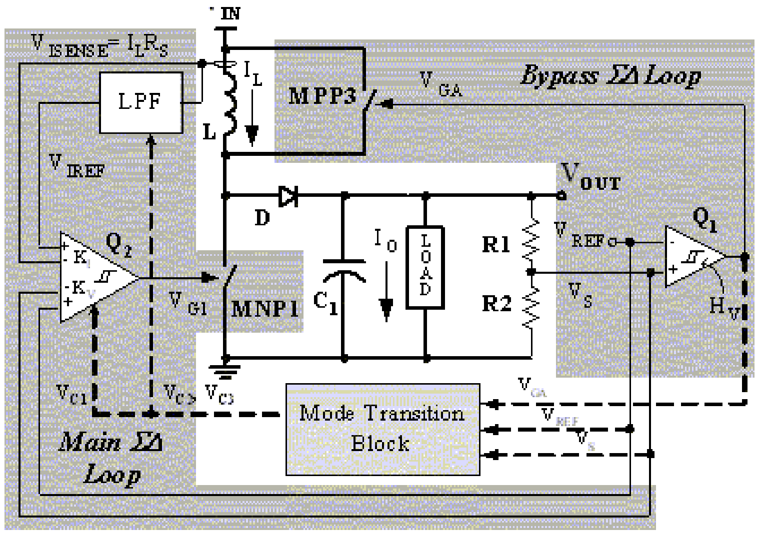

Figure 1b. Proposed accurate, fast, LC compliant boost converter - circuit level schematics

The main ΣΔloop, which again operates in steady state, is fully controlled by summing comparator Q_2, which amplifies the ripples of the sensed inductor current and output voltage by gains K_I and K_V, respectively, to generate an internal variable σ. This variable σ , is regulated to zero by the feedback control action of Q_2, as in conventional sliding-mode control. In steady state, auxiliary switch MPP3 is always open and the bypass ΣΔ block containing comparator Q_1 is inactive. The main loop gives wide LC filter compliance and low output voltage ripple since it adheres to the teachings of sliding-mode ΣΔ control. However, the transient response is slow because it is defined to meet the requirements of the worst-case LC specifications. This slow response is corrected using the fast bypass ΣΔ loop during transient events.

The bypass ΣΔ loop, operating during transient events only, is controlled by comparator Q_1, which senses and controls the output voltage through the duty-cycle of switch MPP3. During bypass conditions, when the output voltage drops below the predefined window limit set by Q_1, the bypass loop regulates the output voltage (V_S) to V_{REF}, irrespective of the inductor current, forcing the average inductor current to increase, since its dI_L/dt is now mostly unidirectional. This current consequently increases beyond its minimum average value I_{LMIN} (inductor current I_L equals I_{LMIN} during steady-state conditions) and only drops back down when the output voltage again reaches its prescribed window limits, at which point MPP3 is disabled. Comparator Q_2 only regulates the sensed inductor current to its reference value, which is the DC value of the sensed current. This current loop is therefore independent and self-sustaining and the inductor current, as it is, is regulated and constant. A higher-than-minimum inductor current leads to increased power losses and a higher output voltage ripple, which is why the inductor current must be ultimately reduced to I_{LMIN}.

The mode transition block manages the transitions between the steady-state and bypass modes. It senses the excess inductor current (I_L–I_{LMIN}) when the circuit operates in the bypass ΣΔ mode and gradually reduces its current reference (V_{IREF}) until the inductor current equals its minimum value. Sensing the excess current is achieved by way of MPP3's duty cycle; since the excess current is re-circulated through MPP3 when it conducts, MPP3 being off indicates all the available current flows to the output and no excess current exists. To adjust V_{IREF}, from Figure 2, a current I_1 is pulled from the resistive ladder comprising V_{IREF} whenever switch MPP3 is closed (R_{F2} is much smaller than R_{F1}). This reference offset causes a reduction in the duty cycle of switch MNP1 and therefore a reduction in inductor current I_L until switch MPP3 stops switching, i.e., inductor current I_L equals I_{LMIN}. In case of sustained load transitions, when a 2% output voltage drop occurs, the average inductor current is increased in a single step by means of comparator Q_3, increasing the value of current reference V_{IREF} to a level required to support the maximum designed load current. The resulting operation guarantees natural and smooth transitions between steady-state and bypass modes.

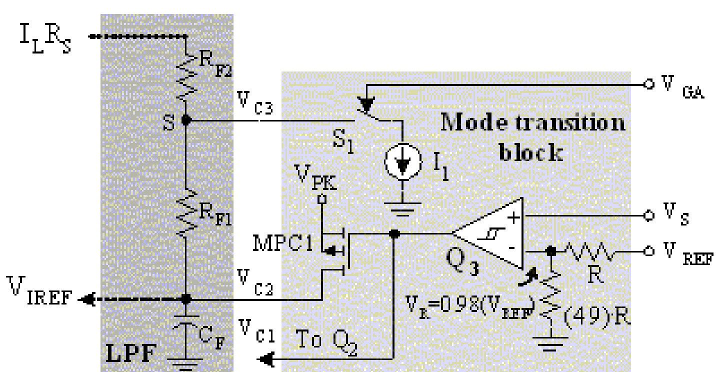

Figure 2. Schematic of the mode transition block and low pass filter LPF

The simulation results of the proposed topology during start-up and transient load conditions are illustrated in Figs. 3 and 4, respectively, and the parameter values used in the design are shown in Table 1. During start-up, the circuit behaves as a dual ΣΔ loop converter with an output voltage ripple of ±100 mV (±2 % of VOUT). As the excess inductor current gradually decreases and finally disappears, the circuit transitions to single ΣΔ loop control, which occurs when switch MPP3 stops switching, in other words, when its gate voltage V_{GA} remains high. The steady-state ripple voltage of the single ΣΔ loop is approximately ±0.2 % (±10 mV). In response to a fast load-current dump, the inductor current rises to 1.7 A in a single switching cycle, which is why the proposed converter is fast, resulting in a transient voltage drop of 250 mV (Fig. 4(a)) when its state-of-the-art single ΣΔ loop equivalent designed to operate within the same LC filter range specified in Table 1 had a 396 mV variation (Fig. 4(b)), which is about 37% improvement in accuracy. The proposed bypass scheme therefore boasts high LC-compliance, low voltage ripple, fast response, and high power efficiency, outperforming both the single- and dual-ΣΔ-loop strategies reported. These benefits are achieved, of course, at the cost of complexity. We are currently working to design, implement, and test an integrated circuit prototype of this proposed scheme.

Parameter	Value	Parameter	Value
V_{IN}	3.3 V	V_O	5 ±5%
IO	0.1-1 A	L	1-30 µH
C	20-350 µF	D (P-ch) R_{ON}	0.15 Ω
R_{ONMNP1}	0.1 Ω	R_{ONMNP3}	0.5 Ω
K_I	4	K_V	1
C_1	200 pF	I_1	5 µA
Q_1, Q_3 hysteresis H_V	24 mV	Q_2 hysteresis H_S	100 mV
M	0.24	R_S	0.5 Ω
Simulator	Spectre	CMOS Tech	0.5 Ω

Table I. Simulation parameters and operating conditions

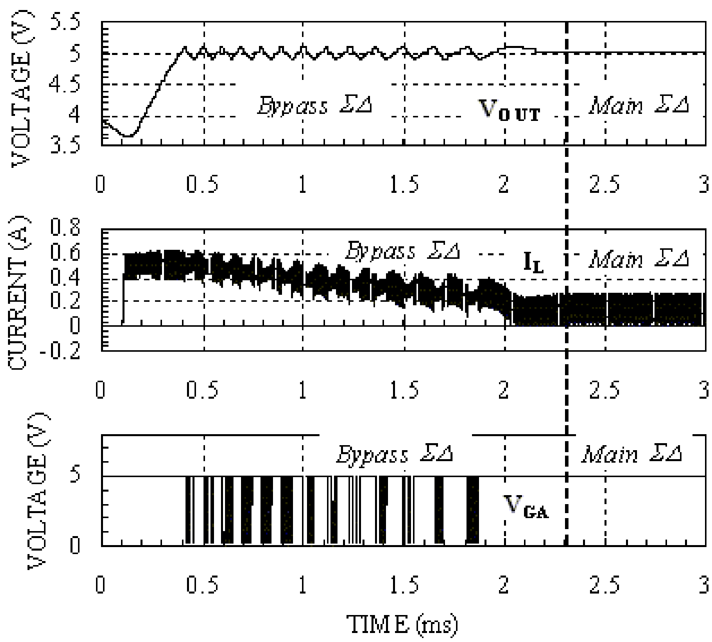

Figure 3. Start-up (±100 mV ripple) and steady-state (±10 mV ripple) waveforms of the proposed Σ Δ converter (L = 5 µH, C = 47 µF, and I_O = 0.1 A)

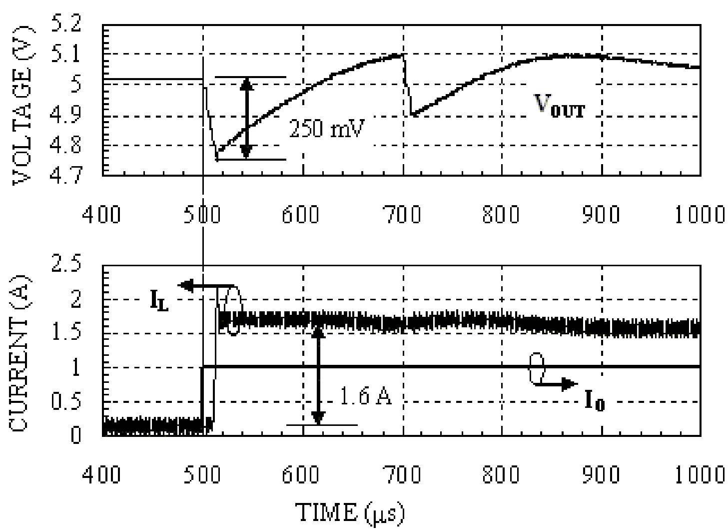

Figure 4a. Load-step transient waveforms at L = 5 μH, C = 47 μF, and I_O = 0.1 - 1 A for the proposed circuit

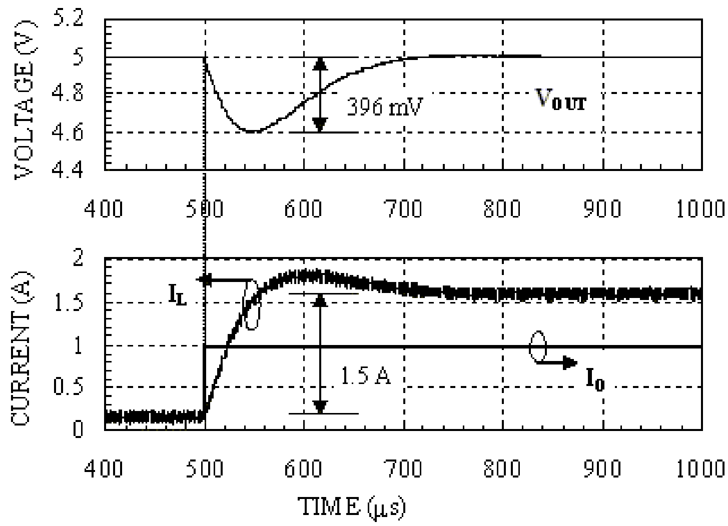

Figure 4b. Load-step transient waveforms at L = 5 μH, C = 47 μF, and I_O = 0.1 - 1 A for the single-loop ΣΔ control

References

[1] B. Schaffer, "Internal compensation – boon or bane?," Unitrode Design Seminar SEM 1400, Texas Instruments, Dallas, TX, 2001.
[2] N. Keskar and G.A. Rincón-Mora, "A high bandwidth, bypass, transient-mode sigma-delta dc-dc switching boost regulator with wide LC compliance," accepted for publication at The 31st Annual Conference of the IEEE Industrial Electronics Society, IECON 2005, Nov 2005.
[3] N. Keskar and G.A. Rincón-Mora, "A user-friendly boost DC-DC converter topology - it's fast and widely stable," Power Management Design Line, Jan 2005, online publication at: http://www.powermanagementdesignline.com/showArticle.jhtml?articleID=57703109.

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