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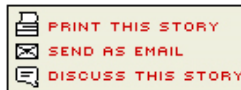
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Self-learning switching DC-DC converters meet smart power

By Gabriel A. Rincón-Mora, Senior Member, IEEE, and H. Pooya Forghani-zadeh, Student Member, IEEE; Georgia Tech Analog and Power IC Design Lab

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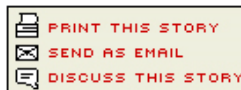
High-performance, state-of-the-art applications demand smart power supplies to be adaptive, power efficient, and reliably accurate, which is why monitoring inductor current flow in a lossless fashion is desirable and critical for protection, power-moding, and feedback control [1-2]. A handful of lossless current-sensing techniques are available today but their accuracies still do not compete with the traditional series sense-resistor schemes, and that is, for the most part, because the current is sensed by *estimating* the impedance of some series element and extrapolating the value of the current from the voltage across it, as Ohm's law dictates [3].

Estimating the power MOSFET's turn-on resistance R_{on} , for instance, is inherently inaccurate because of its wide process, supply voltage, and temperature dependence, varying from approximately 50% to 200%. Additionally, the measured current only flows within a portion of the period, which requires a switched sample-and-hold circuit, another noise-generating device. Using an embedded current-sensing MOSFET, a power transistor's sister mirroring device sourcing a small fraction of the current (i.e., mirror ratio of typically over 1,000), is better with regard to accuracy but still inaccurate and also discontinuous, and only practical for on-chip power devices. Although accuracies of $\pm 4\%$ are reported [4], mismatch and process sigma variations across such a large spread of mirroring devices can reach $\pm 20\%$ [5].

The only continuous and therefore less noisy and more useful scheme for current-mode switching supplies is the matched-filter method [6]. In this scheme, the series impedance of the inductor and its equivalent series resistor (ESR) (that is, $L_s + ESR$) is matched against the series impedance of an RC network (for example, $R + 1/Cs$). Since both impedances are equal and they are subjected to the same voltage, their currents are also equal, which is why the displacement current through the RC filter is a direct measure of the inductor current. The accuracy of this technique, however, depends on how well matched the RC network is to the inductor-ESR combination, and that can lead up to $\pm 28\%$ error, given $\pm 15\%$ inductance, $\pm 11\%$ ESR, and temperature (for example, 70 °C) variations, and more if extended to commercial and military temperature ranges. The RC filter is therefore external to the controller IC and typically custom-designed.

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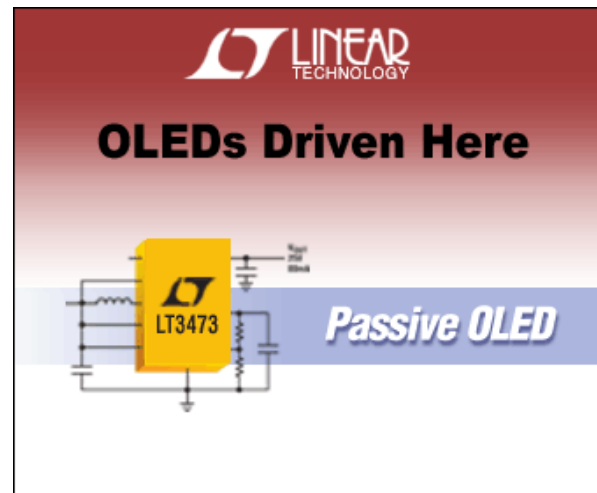
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Knowing the inductance

How can IC designers know the impedance? They can't...but the circuit can learn it during start-up and/or through power-on reset events; in other words, the system can measure the inductance-ESR impedance during down-times. Figure 1 illustrates how this approach can be applied to a buck (step-down) DC-DC converter using the above-described continuous filter scheme, where V_{Sense} is directly proportional and calibrated against inductor current I_L . The shaded block is the G_m -C filter whose gain-bandwidth product is *tuned* with transconductor g_{m1} and DC gain *calibrated* with resistor R_2 during a system down-time, aided by transistors M_a and M_b , both of which are off during normal operating conditions. The rest of the circuit is simply the power train of the switching supply, comprised of inductor L and its ESR R_L , output capacitor C_o , and high and low power MOS transistors M_H and M_L . Once the gain-bandwidth product and DC gain are properly adjusted (that is, filters are matched), the values are digitally stored and the DC-DC converter is allowed to power up and operate normally. Since the learning cycle only affects start-up, their associated power losses are non-existent during normal operating conditions, which is why this scheme is considered lossless.

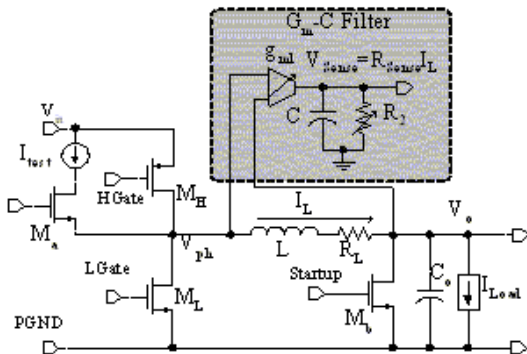


Figure 1. Self-learning current-sensing G_m -C filter

The design and self-learning goal of the filter scheme is to match the series impedance of the inductor- R_L combination with the R_2C filter during the learning cycle. Following Ohm's law, inductor current I_L is inversely proportional to its series impedance and directly proportional to the voltage across it (V_L):

$$I_L = V_L \left(\frac{1}{R_L + sL} \right) = \frac{V_L}{R_L} \left(\frac{1}{1 + sL/R_L} \right) \quad (1)$$

The R_2C network, in this case, is a G_m -C filter with output voltage V_{Sense} equal to:

$$V_{Sense} = V_L g_{m1} R_2 \left(\frac{1}{1 + sR_2 C} \right) \quad (2)$$

Consequently, adjusting R_2 to ensure inductor current bandwidth RL/L equals filter bandwidth $1/R_2C$ sets V_{Sense} to:

$$V_{Sense} = (g_{m1} R_2 R_L) I_L \text{ how does this look?}$$

$$V_{Sense} = (g_{m1} R_2 R_L) I_L \quad (3)$$

and if $g_{m1} R_2 R_L$ is tuned to a known constant R_{Sense} , V_{Sense} is a direct measure of inductor current I_L ,

$$V_{Sense} = R_{Sense} I_L \quad (4)$$

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Set the conditions

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To set these conditions, the circuit is subjected to a programming sequence during its down-time, but only after all start-up and power-on-reset functions are asserted and stabilized. First, a triangular current with a frequency significantly higher than inductor and G_m -C bandwidths R_L/L and $1/R_2C$, respectively, is injected into the inductor- R_L network to ensure resistances R_L and R_2 are negligibly smaller and larger than the inductor and capacitor's impedances, respectively (Figure 2). Consequently, a mostly square waveform appears across the inductor (that is, $V_L L \, dI/dt$), which the g_{m1}/C filter integrates back into a triangle (that is, $dV_{Sense}/dt \, I_{gm1}/C$),

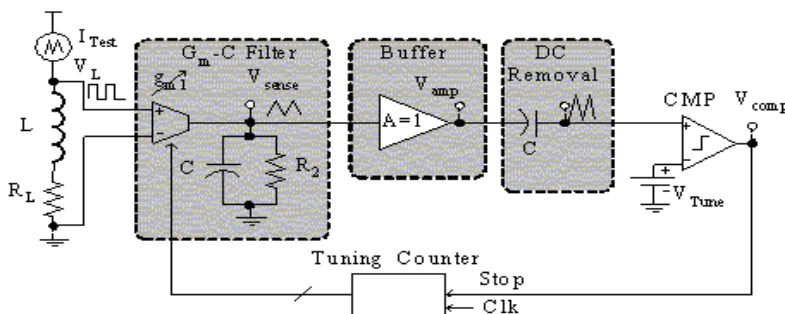
$$V_{Sense} = I_{gm1} Z_C = (V_L g_{m1}) \left(\frac{1}{C s} \right) = (I_L [L s] g_{m1}) \left(\frac{1}{C s} \right) = \left(\frac{g_{m1} L}{C} \right) I_L$$

(5)

The ac portion of V_{Sense} is compared against V_{Tune} and the counter gradually tunes g_{m1} until the peak of V_{Sense} equals V_{Tune} , at which point the filter gain-bandwidth product (that is, g_{m1}/C) is set, setting and storing g_{m1} to:

$$g_{m1} = \frac{C V_{Tune}}{L I_{Peak}} \quad (6)$$

where I_{Peak} is the peak value of the triangular input test current.



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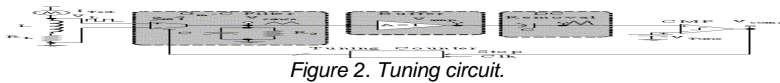
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The end of the tuning cycle marks the onset of the calibration phase, at which point a DC test input current equal to I_{Peak} is injected into the inductor- R_L network, as shown in Figure 3. The impedance across inductor L and capacitor C at DC are significantly smaller than R_L and larger than R_2 , respectively. The resulting sense voltage is therefore:

$$V_{Sense} = (I_{Peak} R_L) (g_{m1} R_2) \quad (7)$$

which is subsequently compared against V_{Tune} . Like before, the counter cycles and adjusts R_2 until V_{Sense} is equal to V_{Tune} , setting the DC transimpedance gain (that is, $R_{Lg_{m1}R_2}$) of the network, or:

$$R_2 = \frac{V_{Tune}}{I_{Peak} R_L g_{m1}} = \left(\frac{V_{Tune}}{I_{Peak} R_L} \right) \cdot \left(\frac{L I_{Peak}}{C V_{Tune}} \right) = \frac{L}{R_L C} \quad (8)$$

where the previously set g_{m1} (Equation. 6) is substituted in. The new relation satisfies the original intent of equating inductor current bandwidth R_L/L to filter bandwidth $1/R_{sub} > 2C$, and by setting V_{Tune}/I_{Peak} to known constant R_{Sense} , $g_{m1}R_2R_L$ is similarly defined to R_{Sense} :

$$g_{m1} R_2 R_L = \left(\frac{C V_{Tune}}{L I_{Peak}} \right) \cdot \left(\frac{L}{R_L C} \right) \cdot R_L = \frac{V_{Tune}}{I_{Peak}} \equiv R_{Sense} \quad (9)$$

and Equation. 4 is satisfied.

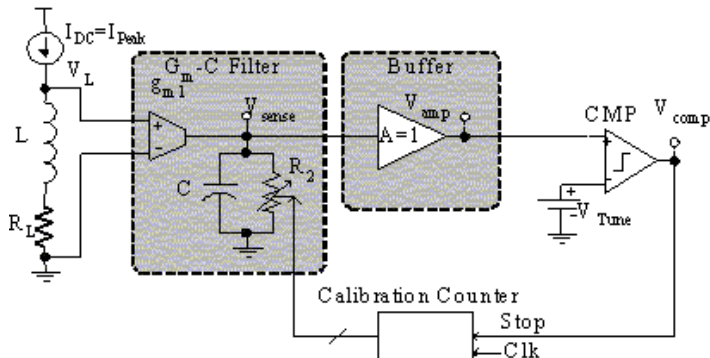


Figure 3. Calibration circuit.

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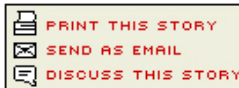
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In spite of self-learning, bias-induced and trimming accuracy errors still exist in the system. Current density and temperature settings, for instance, change from the self-learning sequence to the normal operating mode (the test current is for the most part smaller than the load current because of power and associated on-board real-estate concerns). These errors can be adjusted empirically, but not exactly. A first-order temperature dependence, for example, can be superimposed onto R_{Sense} . The input-referred offset and linearity of the transconductor across its wide input-common mode range (ICMR) will also impose errors. A linear, low offset transconductor with wide ICMR limits is therefore required. Nevertheless, a PCB prototype implementation of the technique presented exhibited overall full-load DC and AC gain errors of less than 2.3% and 5%, respectively, which is significantly better than previously reported lossless techniques [7]. A complete on-chip prototype is currently under development [8].

For additional details, questions, and/or comments on this article, please contact us, the Georgia Tech Analog and Power IC Design Lab, at gtap@ece.gatech.edu. More information about our research can be found at <http://www.rincon-mora.com/research>.

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