A Trimless, Package-Shift Compensated, High PSR, Low Dropout CMOS Regulated Reference

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Abstract

• An accurate, package-shift compensated, high PSR, low dropout, CMOS regulated reference is presented.
• High accuracy has been achieved through the use of lateral PNP devices, available in standard CMOS.
• Package-shift has been studied to compensate it by “averaging” its effects across the die.
• High PSR has been obtained through the use of a simple NMOS cascoding technique.

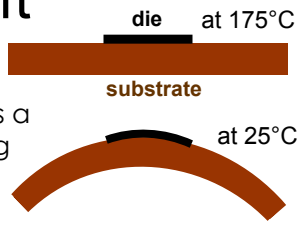
Motivation

- Trimming “bandgaps” adds manufacturing cost and, hence, time.
- Package-shift is an important source of error since it requires post-package trimming, which is expensive and often unreliable.
- High PSR is crucial in a linear regulator, whether it is powered off a switching-converter, or is placed in a proximity of digital circuits, which generate switching noise.

Error Sources in CMOS Bandgap References

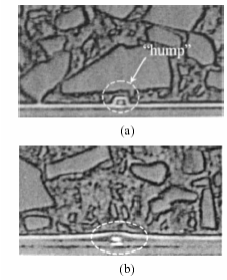
ERROR	TYPICAL 3-σ VALUE	RELATIVE MAGNITUDE	CAN BE TRIMMED?
Opamp offset	± 10 mV	Very Large	No
Package-Shift	± 7 mV	Large	No
V_{BE} spread	± 24 mV	Very Large	Yes
Current-mirror mismatch	± 10%	Large	Yes
Resistor mismatch	± 1%	Large	Yes
Transistor mismatch	± 1%	Small	Yes
Resistor tolerance	± 20%	Small	Yes

Package-Shift



Systematic

- Difference in thermal coefficient of expansion of package and silicon causes a strain on die as system cools from molding temperature.
- Can be accounted for in design phase.



Random

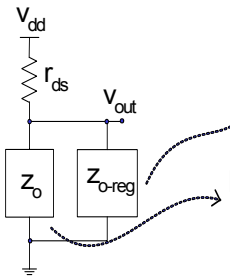
- Presence of filler in plastic packages produces intense vertical stress due to the pressure of filler particles on die surface.
- **Is a random variation that varies with location on the die**.

PSR in Linear Regulators

$$PSR = \frac{v_{out}}{v_{dd}} = \frac{(z_o \parallel z_{o-reg})}{r_{ds} + (z_o \parallel z_{o-reg})}$$

$$z_o = (z_{Cout} + R_{ESR}) \parallel (R_1 + R_2)$$

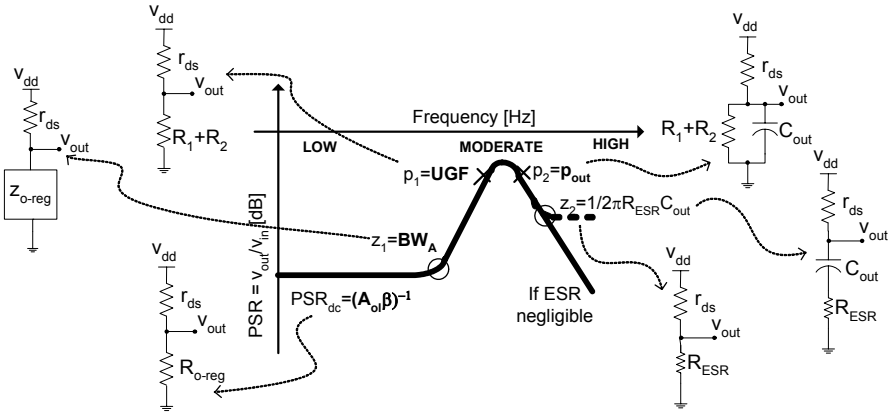
$$z_{o-reg} = \frac{z_o \parallel r_{ds}}{A_{ol}\beta}$$



Effective when loop gain high (low to moderate frequencies)

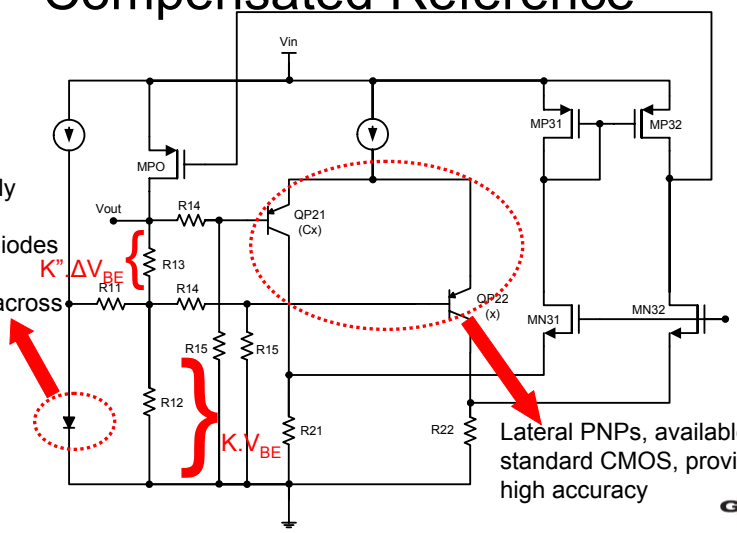
Effective when loop gain low (moderate to high frequencies)

PSR in Linear Regulators



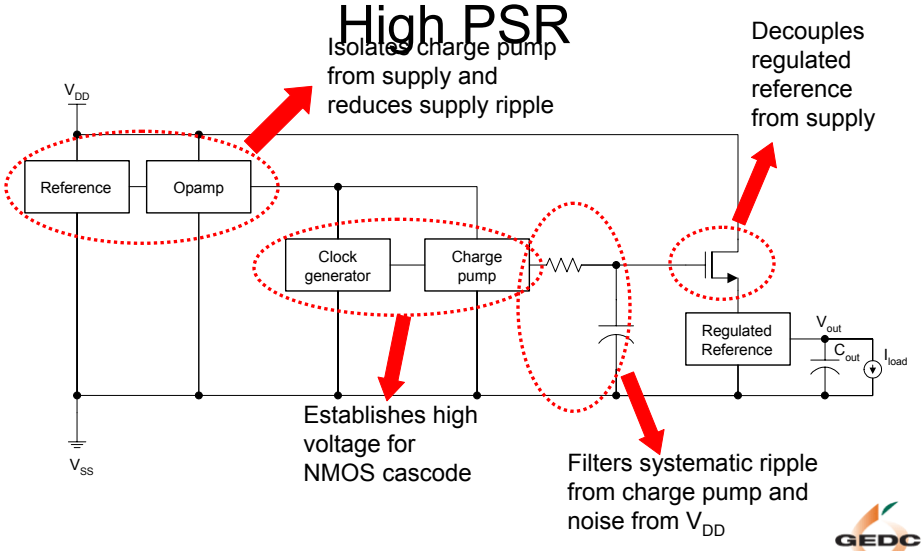
Accurate, Package-Shift Compensated Reference

Will be dynamically switched between diodes at various locations across die



Lateral PNPs, available in standard CMOS, provide high accuracy

Block Diagram of System for High PSR



Conclusions

- A high accuracy in CMOS bandgaps can be achieved by using lateral PNP devices as opamps.
- Package-shift can possibly be compensated by averaging out its random effects across the die.
- A high PSR regulator can be obtained by using a simple NMOS cascoding scheme.