# FULLY INTEGRATED REGULATORS WITH ULTRA-FAST TRANSIENT RESPONSE

by

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2002



## Abstract

As the speed, complexity, and performance of modern systems increase, their dynamic loading requirements on voltage regulators become even harsher. The solution to meet the ever-increasing demand for future systems is fully integrated regulator with ultra-fast transient response. The different techniques for fast transient response voltage regulators are illustrated and their performances are compared and evaluated. Based on these techniques, the best topology for fully integrated regulators with ultra-fast transient response is proposed.

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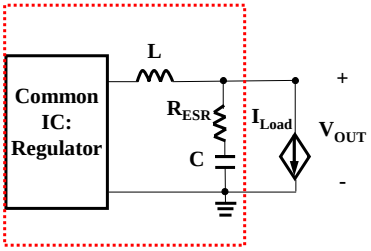
## Motivation — Fully Integrated Regulators

Fully Integrated Regulator




Simplified Regulator Structure

→ **Using large output filter capacitance of C increases the overall cost and board area required.**

→ **Reducing the output filter capacitance C will degrade the transient response, which is a dominant factor to the accuracy of the regulators.**

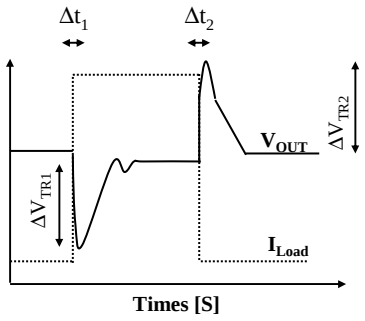
→ **Challenge: system-on-chip (SOC) solutions for linear or switching regulators with ultra-fast transient response used in mobile/battery operated applications.**

| On-chip Inductor | On-chip Capacitor |
|---|---|
| ≈ 20 nH | 100~500 pF |



## Goals — Improve Transient Response

**Typically 3~4% of the accuracy is allocated to transient response. Therefore, to improve accuracy, transient response must be reduced.**




**Typical Transient Response To Sudden Load-current Changes**

→ Reduce $\Delta V_{TR1}$ and $\Delta V_{TR2}$

Add an fast parallel loop at the output of the regulator to help source the load current.

→ Minimize $\Delta t_1$ and $\Delta t2$

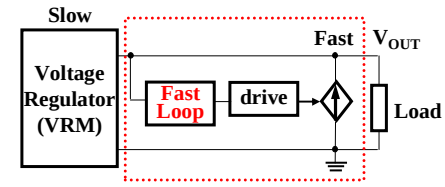
Increase the closed-loop bandwidth of the regulator.

**Target operating conditions (battery):**

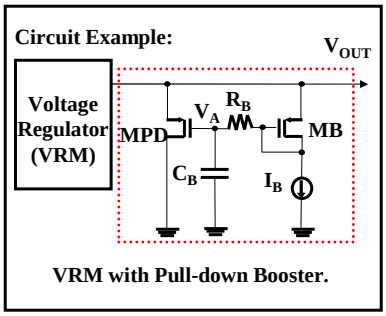
| | |
|---|---|
| Output Voltage: | 0.9 ~ 1.8 V |
| Load Current: | < 2 A |
| Total Output Voltage Tolerance | ± 2% |

## Technique 1 — Fast Parallel Loop

**Advantages:** It is independent of VRM and provides fast transient response, before the VRM reacts
**Disadvantages:** More power dissipation during transient and steady-state conditions
**Requirements:** The fast parallel loop does not affect the stability




Fast Loops
- Sensing $V_{OUT}$
- $\partial V_{OUT} / \partial t$ (voltage rate of change)
- HPF, $\partial I_{LOAD} / \partial t$ (current rate of change)




VRM with Pull-down Booster.

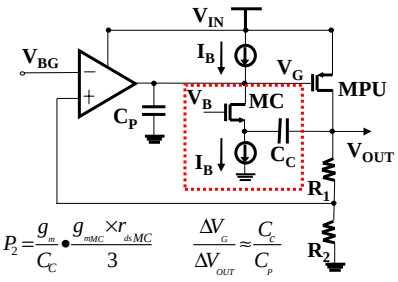
$V_A \approx$ dc bias node, not change with $V_{OUT}$



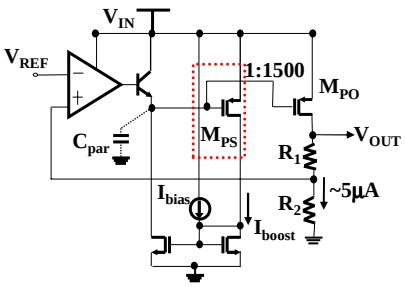
## Technique 2 — Wide Bandwidth Regulators

**Advantages:** Eliminate RHP zero using internally Miller-compensated LDOs & efficiently bias the LDO as a function of load current
**Disadvantages:** Have current sensing issues for LDO
**Requirements:** Increase the closed-loop bandwidth without affecting the stability

**Miller Compensation**

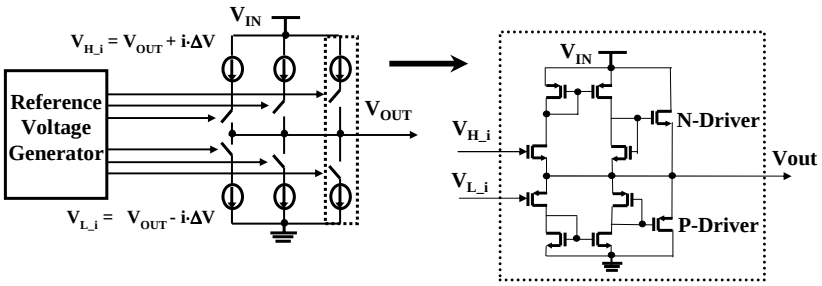



**Load-dependant Current Efficient Buffer**



## Technique 3 — Dynamically Adjustable Regulator

**Advantages:** Localized feedback loops make the closed-loop bandwidth high
**Disadvantages:** Use cascode structure in the reference voltage generator so that area is large and power dissipation is high
**Requirements:** Accurate reference voltage generator is required

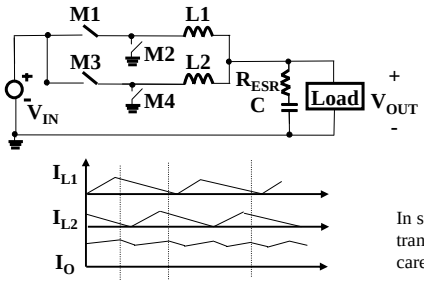




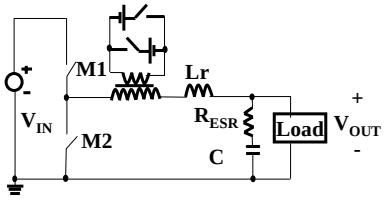

## Technique 4 — Interleaved and Stepping Converters

**Advantages:** Reduce the effective output filter inductance so that the closed-loop bandwidth is increased by paralleling feedback paths or stepping the inductor
**Disadvantages:** Extensive use of inductors and more power dissipation
**Requirements:** Need multiple-phase DC-DC converter for the parallel paths and additional control circuit for the stepping converter

**Interleaved Parallel Converter**




**Stepping Inductance Converter**




In steady state, the output inductance is large and, during transient event, the large output inductor is shorted by carefully selecting the size of the transformer.

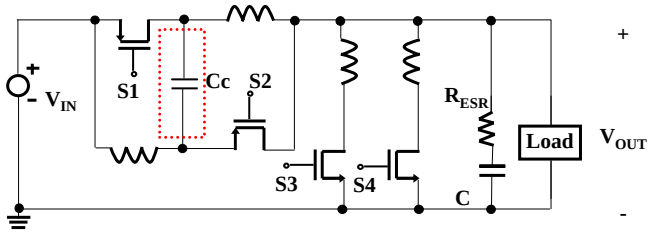
## Technique 5 — Push Pull Converter

**Advantages:** Add additional ac signal path for DC-DC converter to introduce a left-half plane zero at low frequency so that the closed-loop bandwidth and the phase margin are increased.

**Disadvantages:** Extensive use of inductor and high power dissipation.

**Requirements:** For multiple phase DC-DC converter only.

**Push Pull Buck Converter**





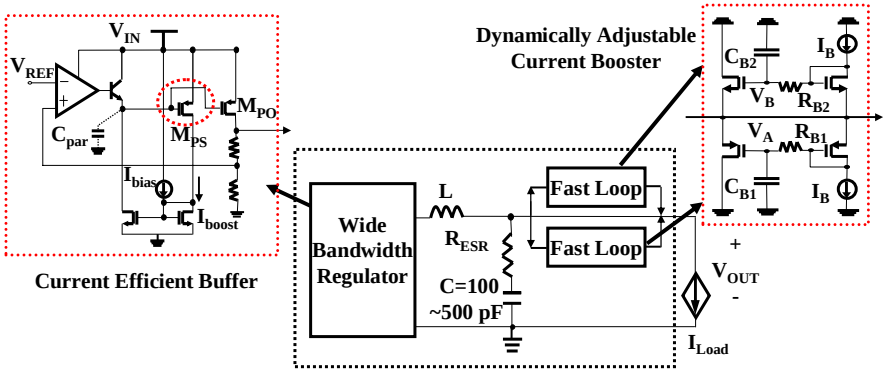

## Evaluation

**The Performance Comparison Between Different Techniques**

| | Parallel AC Paths | | | Wide Closed-loop Bandwidth | | |
|---|---|---|---|---|---|---|
| | **Pull-down booster** | **Interleaved** | **Push-pull** | **Current efficient buffer** | **Dynamically Adjustable** | **Stepping Inductor** |
| **Transient Response** | Fast | Fast | Slow | Moderate | Fast | Fast |
| **Area** | Small | Large | Large | Small | Moderate | Large |
| **Power** | Moderate | High | High | Low | High | Low |
| **Complexity** | Low | High | High | Low | Moderate | Moderate |
| **Output Capacitor** | Moderate | Small | Large | Small | Moderate | Moderate |
| **System-on-chip** | Yes | No | No | Yes | Yes | No |

# Proposal and Future Work

**From the above analysis and evaluation, we can see the best topology for fully-integrated regulators with ultra-fast transient response should contain a wide bandwidth regulator with a fast loop at its output as shown in the figure.**




**Fully Integrated Regulator For Linear or Switching Regulators**