A High Efficiency, Soft Switching DC-DC Converter with Adaptive Current Ripple Control for Mobile, Battery-Powered Applications

GTAC Research Review

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Abstract

- **Motivation for Improving Efficiency in Mobile Applications**
  - Portable application ➡ Compact, low power, low cost, SOC
  - Process technology advancement
Single battery operation } ➡ Low voltage circuits
  - Extension of battery life ➡ Highly power efficient DC-DC converter
  - Portable devices operate in stand-by mode most of the time ➡ Light-load efficiency is crucial for extending battery life

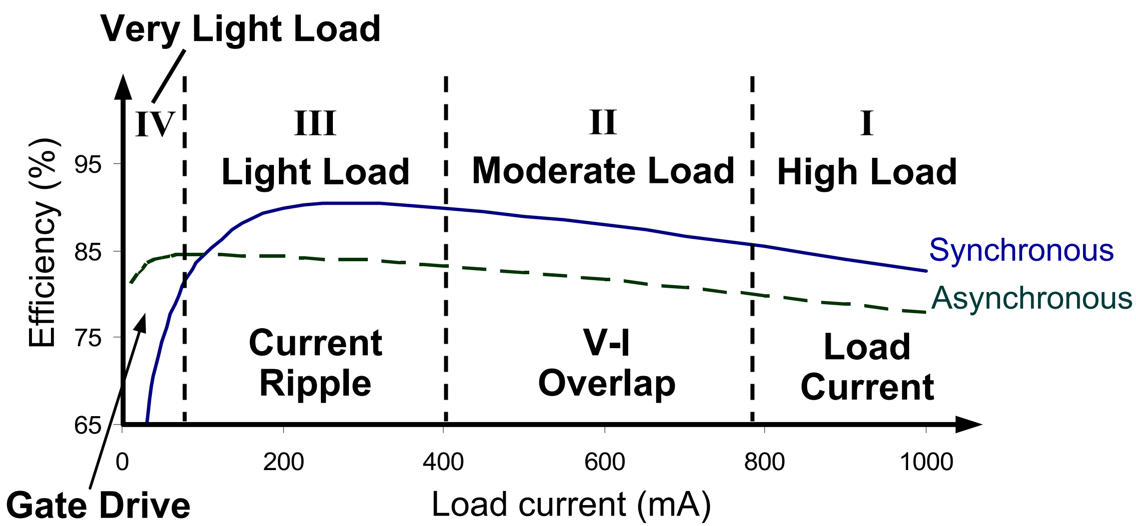
- **Research Goal**

  Improve *power efficiency*, especially at *light loads*, of integrated DC-DC converters for *portable, battery-powered* applications.

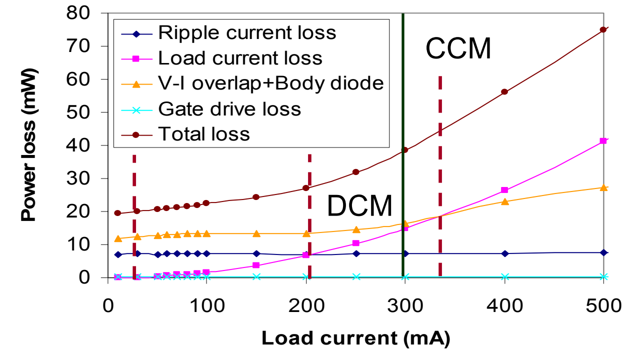
- **Background: power losses**
  - Conduction losses
    - Load current (DC) loss
    - Current ripple (AC) loss
  - Switching losses
    - V-I overlap loss
    - Gate-drive loss

Classification of Power Losses

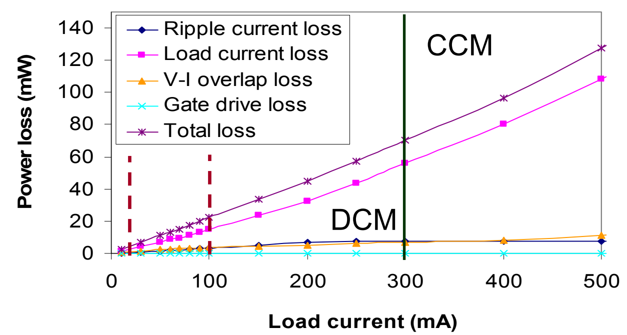
- **Partition of Efficiency Curves**



Power Loss Curves



(a) Synchronous



(b) Asynchronous

  - **Current Ripple: systematic, steady-state (large) ripple**

- **Conclusions**

  - **For region I: Synchronous mode is the best**
  - **For region II: *Soft switching* or decrease the frequency is the best**
  - **For region III: *Reduce the current ripple* is the best**
  - **For region IV: Decrease the frequency is the best**

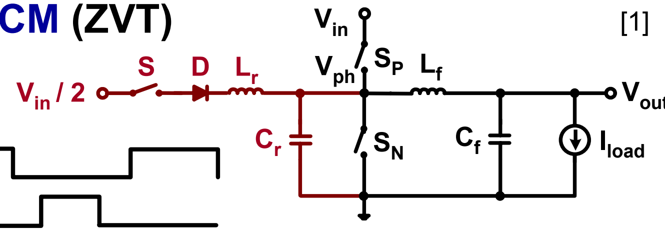
➡ **Soft switching + Reduce current ripple to optimize the efficiency !**

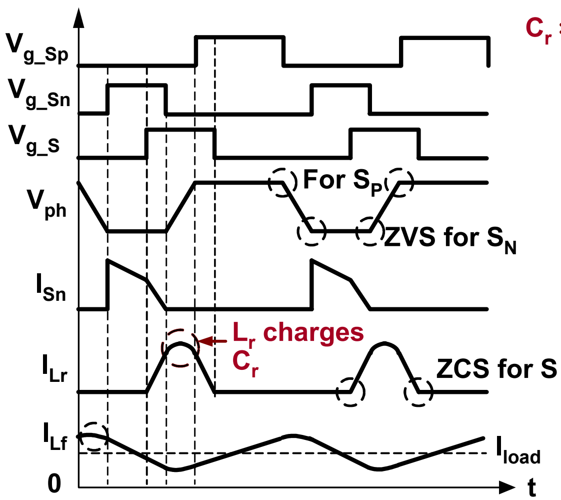
Existing Soft Switching Techniques

- **Soft switching:** Turn on/off MOS switches when $V_{ds} = 0$ or $I_{ds} = 0$

Option 1: CCM (ZVT)

[1]





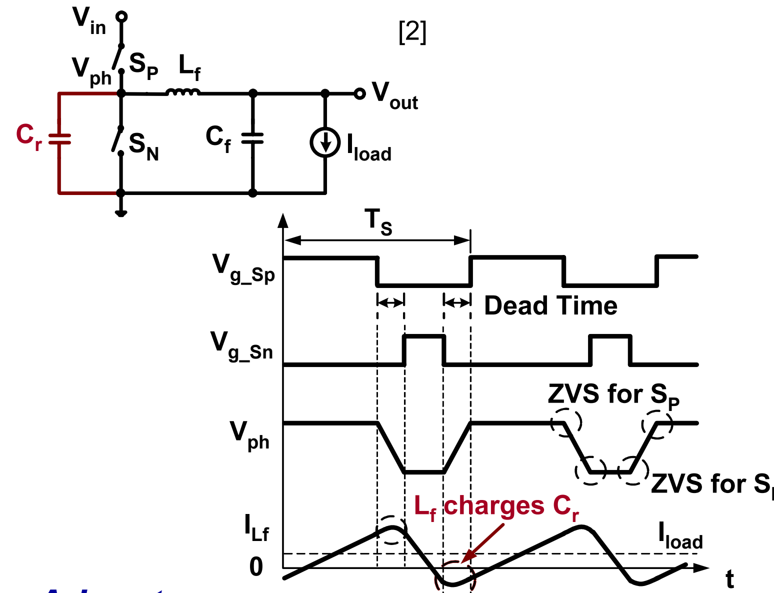
- ***Advantage:***

  Small current ripple in L_f, good accuracy
- ***Disadvantage:***
  - Diode: voltage drop and more losses
  - Fixed losses in S, D, L_r, C_r degrade light-load efficiency
- ***Conclusion:***

  Not suitable for low voltage and light loads

Option 2: Synchronous DCM (QSW)

[2]



- ***Advantage:***

  Only 1 additional off-chip component, 1 cell
- ***Disadvantage:***

  Large and constant current ripple losses
- ***Conclusion:***

  Suitable for light loads, but needs modification

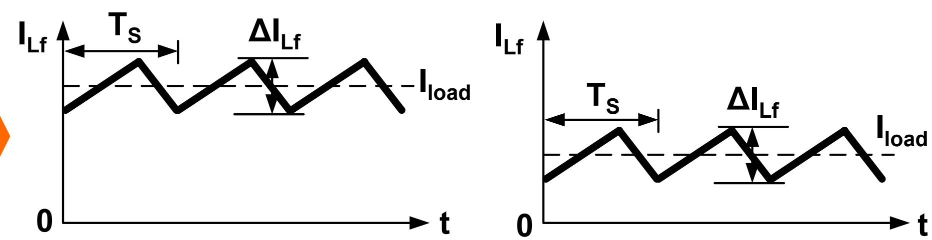
[1] R.N. Prado, "A New ZVT PWM Converter Family: Analysis, Simulation and Experimental Results," *9 th Annual Applied Power Electronics Conference and Exposition*, Vol. 2, 1994, pp. 978–983.

[2] A.J. Stratakos, S.R. Sanders and R. Brodersen, "A Low-Voltage CMOS DC-DC Converter for a Portable Battery-Operated System," *25th Annual IEEE Power Electronics Specialists Conference*, Vol. 1, 1994, pp. 619–626.

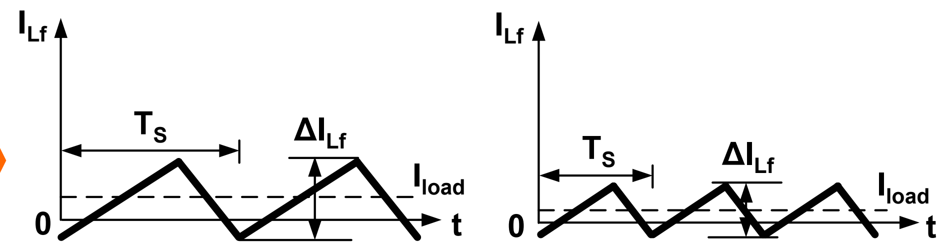
Proposed Technique - Control Strategy

- **Idea:**
  - **Soft switching** over wide load range while **adaptively controlling current ripple**
  - **Mode hopping** to the most efficient mode depending on the load current

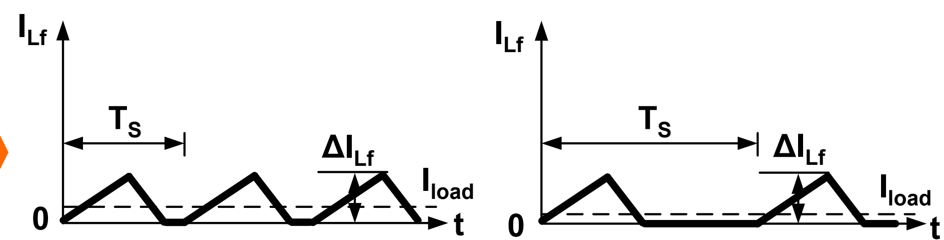
- **Control Strategy:**
  - ***Mode 1* (high and moderate loads):**
    - Soft switching in **CCM**
    - **Minimum current ripple**
    - ➡ ***Highest f_S*** (e.g. 2 MHz)



  - ***Mode 2* (light loads):**
    - Soft switching in **synchronous DCM**
    - **Current ripple proportional to I_{load}**
    - ➡ ***f_S is first lowered*** (e.g. 430 kHz), then ***$f_S \uparrow$ with $I_{load} \downarrow$*** (e.g. 430 kHz to 1 MHz)



  - ***Mode 3* (very light loads):** [1]
    - Hard switching in **asynchronous DCM**
    - **Constant current ripple** (constant t_{on})
    - ➡ ***$f_S \downarrow$ with $I_{load} \downarrow$***, $\eta \neq f(I_{load})$

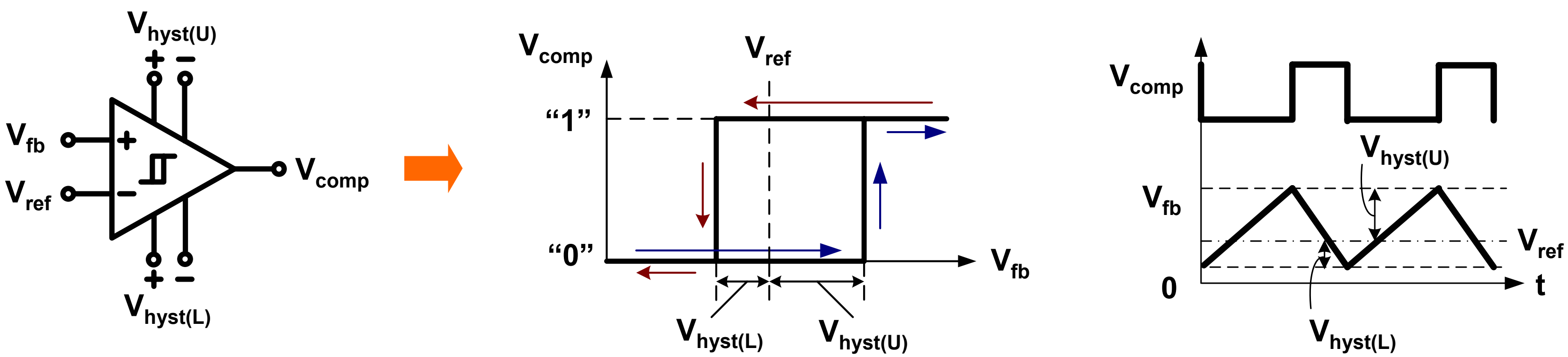


[1] B. Arbetter, R. Erickson and D. Maksimovic, "DC-DC Converter Design for Battery-Operated Systems," *26th Annual IEEE Power Electronics Specialists Conference*, Vol 1, 1995, pp. 103–109.

Proposed Technique - Implementation

- **Assumption:** Output voltage ripple is dominated by the ESR of the filter capacitor
- **Hysteretic Control – Why?**
  - Simple topology, low cost
  - Inherently stable (no compensation)
  - Fast transient response
  - Programmable hysteresis (V_{hyst}) [1]
  - Self oscillating, $f_S = f(V_{hyst})$
- **The User-Programmable Hysteretic Comparator** [1]

$$\Delta I_{Lf} = \frac{\Delta V_{out}}{R_{Cf\_ESR}} = \frac{V_{hyst(U)} + V_{hyst(L)}}{R_{Cf\_ESR}}$$

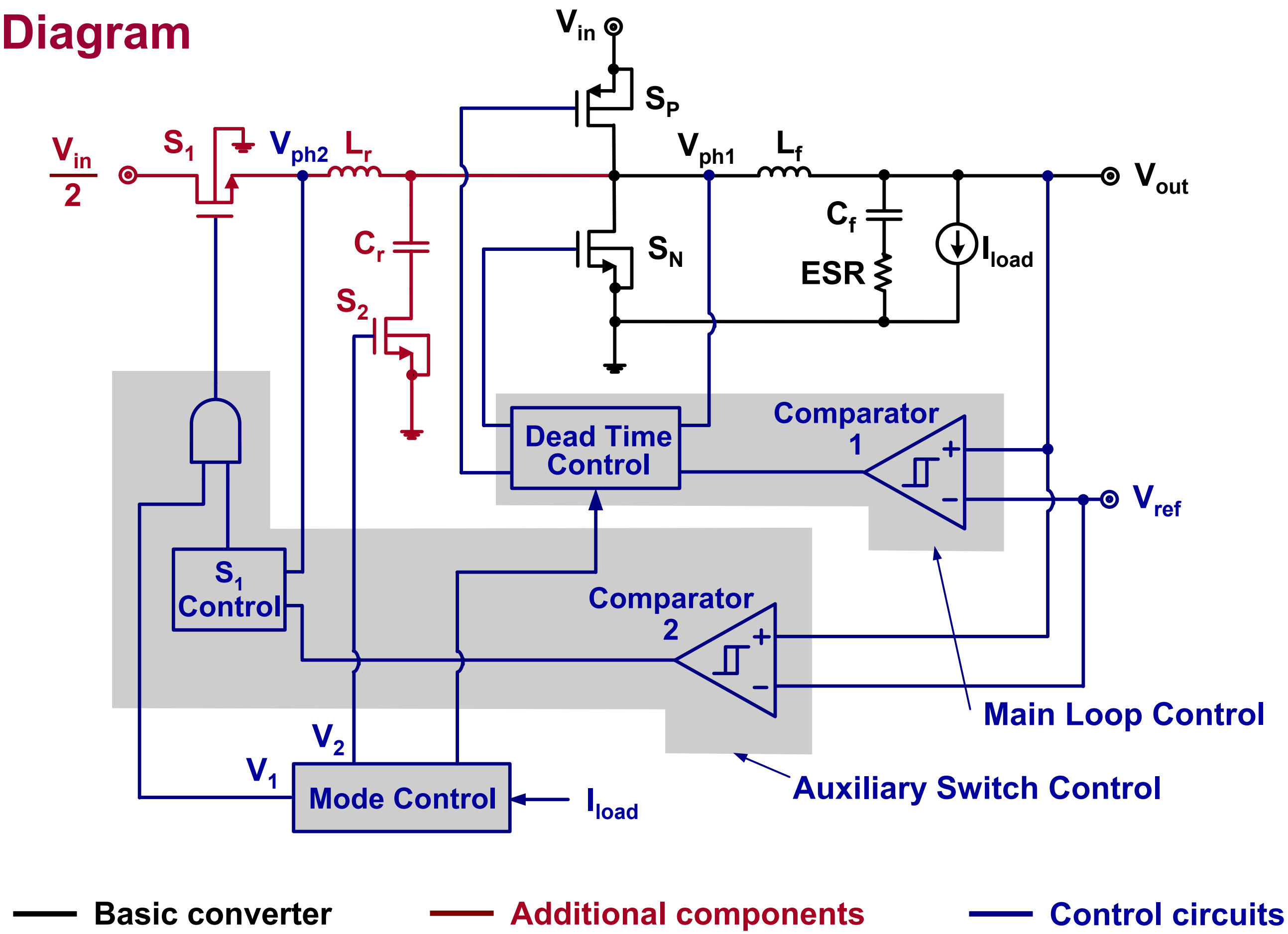


- Asymmetrical hysteresis is set to control asynchronous DCM *(Mode 3)*

[1] G.A. Rincón-Mora, "Accurate, fast, and user programmable hysteretic comparator," United States Patent, No. US 6,229,350 B1, May 8, 2001

Proposed Technique - Implementation

- **Circuit Diagram**



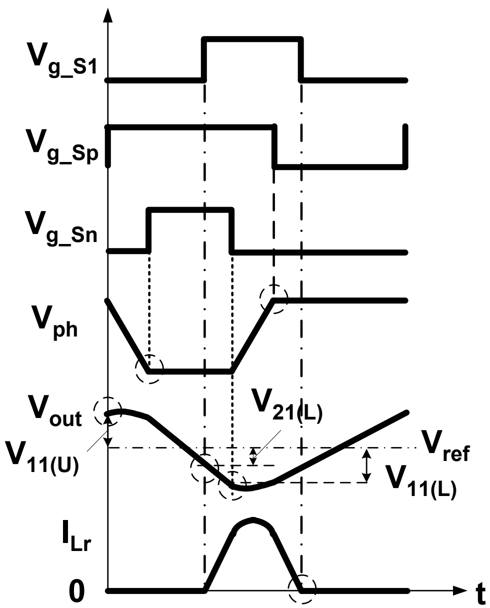
- **Comments**
  - Adaptively program (reduce) the hysteresis of comparator 1 in *Mode 2* as I_{load} decreases
  - No diode used for ZVS in CCM (*Mode 1*) ➡ Need precise zero-crossing detection circuit

Proposed Technique - Implementation

- **Detailed Waveforms of the Proposed Converter**

Mode 1

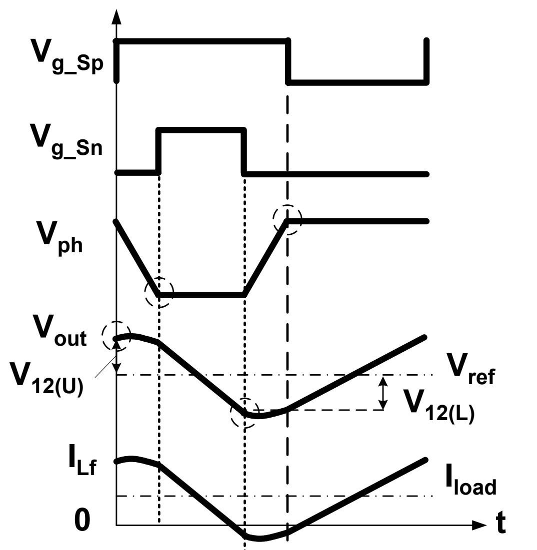
V_1 = "1", connect L_r
V_2 = "1", connect C_r



$V_{11(U)} = V_{11(L)} = 2\ V_{21(U)} = 2\ V_{21(L)}$
ΔI_{Lf} = minimum and constant

Mode 2

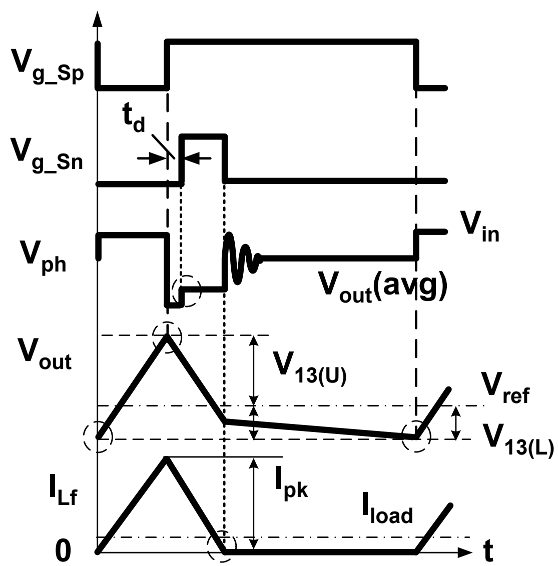
V_1 = "0", disconnect L_r
V_2 = "1", connect C_r



$V_{12(U)} = V_{12(L)} = 1.25\ R_{Cf\_ESR} \times I_{load}$
$\Delta I_{Lf} = 2.5\ I_{load}$

Mode 3

V_1 = "0", disconnect L_r
V_2 = "0", disconnect C_r



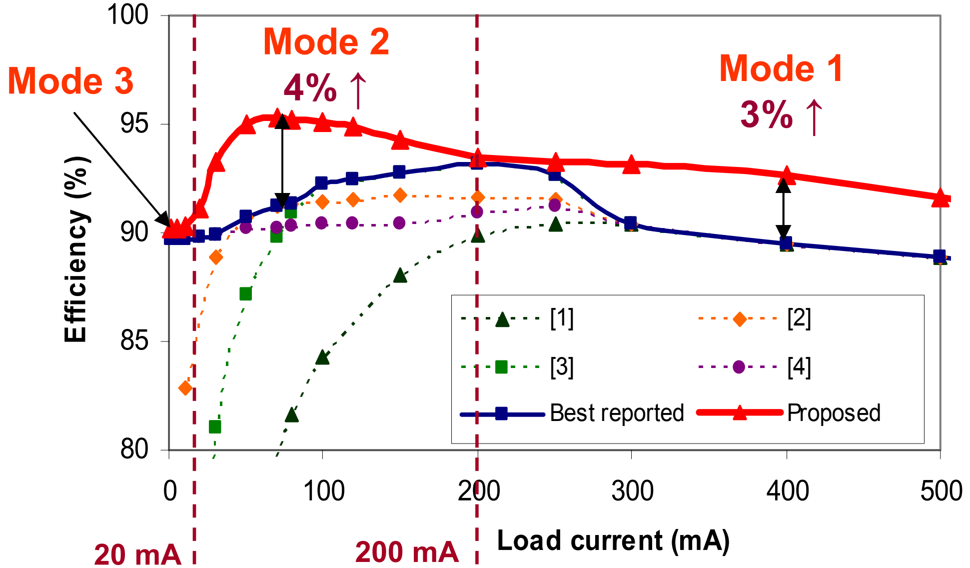
$V_{13(U)} > V_{13(L)} = f(I_{pk}, ESR, L_f, C_f, V_{in}, V_{out})$
$\Delta I_{Lf} = I_{pk}$ = preset and constant

Simulation Results

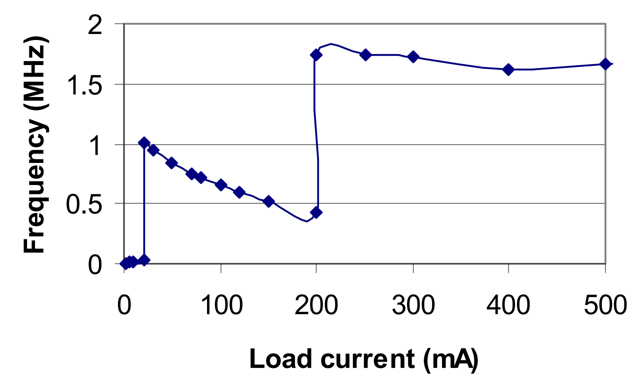
$$V_{in} = 2.4V, V_{out} = 1.2V;\ L_f = 2\mu H, C_f = 47\mu F, L_r = 150nH, C_r = 10nF;$$

$$R_{ON\_Sp} = 200m\Omega, R_{ON\_Sn} = R_{ON\_S1} = R_{ON\_S2} = 80m\Omega, R_{L\_ESR} = 10m\Omega, R_{C\_ESR} = 75m\Omega;$$

Efficiency of the buck converter



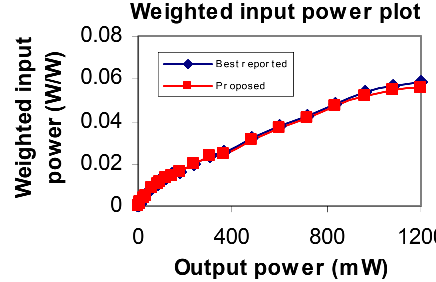
- **"Best reported":**
  Combination of [1] to [4]
- **Switching Frequency**



- **Estimated Battery Life Improvement**

$$\eta_{avg} = \frac{\int_0^{P_{out\_max}} P_{out} \times \Pr ob(P_{out}) dP_{out}}{\int_0^{P_{out\_max}} P_{in}(P_{out}) \times \Pr ob(P_{out}) dP_{out}}$$

Weighted input power plot



3 % improvement in battery life for CDMA cell phone application

[1] Synchronous CCM, f_S = 500kHz

[2] S.H. Jung 1999, Asynchronous DCM using NMOS, PWM, f_S = 500kHz

[3] A.J. Stratakos 1994, Synchronous DCM ZVS, f_S = 500kHz

[4] B. Arbetter 1995, Asynchronous DCM, constant on time, variable f_S

Conclusion and Future Work

- **Advantages:**
  - At high/moderate loads *(Mode 1)*: soft switching in CCM, minimum ΔI_{Lf}
  - At light loads *(Mode 2)*: soft switching in synchronous DCM, *ΔI_{Lf} proportional to I_{load}*
  - At very light loads *(Mode 3)*: constant ΔI_{Lf} in asynchronous DCM, so $\eta \neq f(I_{load})$
  - Use hysteretic control in all three modes: simple, fast, and adaptive

- **Disadvantages and Problems:**
  - Variable frequency leads to EMI problem. But at light loads, the power is small and spread.
  - For very small filter capacitor ESR (ceramic capacitor), ΔI_{Lf} and ΔV_{out} are orthogonal.
  - Internal delay and resonance at light loads make the actual ripple larger than designed.

- **Conclusion:**
  - The proposed control strategy significantly improves *light-load efficiency* of DC-DC converters by *adaptively controlling the current ripple*.
  - The proposed circuit implementation is suitable for *low voltage* DC-DC converters in *portable, battery-powered applications*.

- **Future Work:** Prove the concept by prototyping on a PCB and integrated circuit.