Circuit Design for Accurate and Lossless Current-Sensing in DC-DC Converters

H. Pooya Forghani-zadeh
Advisor: Prof. Gabriel Rincón-Mora
Georgia Tech Analog and Power IC Lab
Georgia Institute of Technology
April 2005

Abstract

Current-sensing circuits are essential for protection and control of the switching regulators. Our proposed technique estimates the inductor current by filtering the voltage across it. Furthermore, the inductor value and its ESR are measured during the startup to boost the accuracy. This poster focuses on the circuit design of proposed system main part- the current-sensing filter. The design challenges are independently programmable gain and bandwidth, high linearity to prevent the systematic offset, and continuous low-offset operation (input-referred offset<0.5mV) without transient spikes.

System – Normal Operation

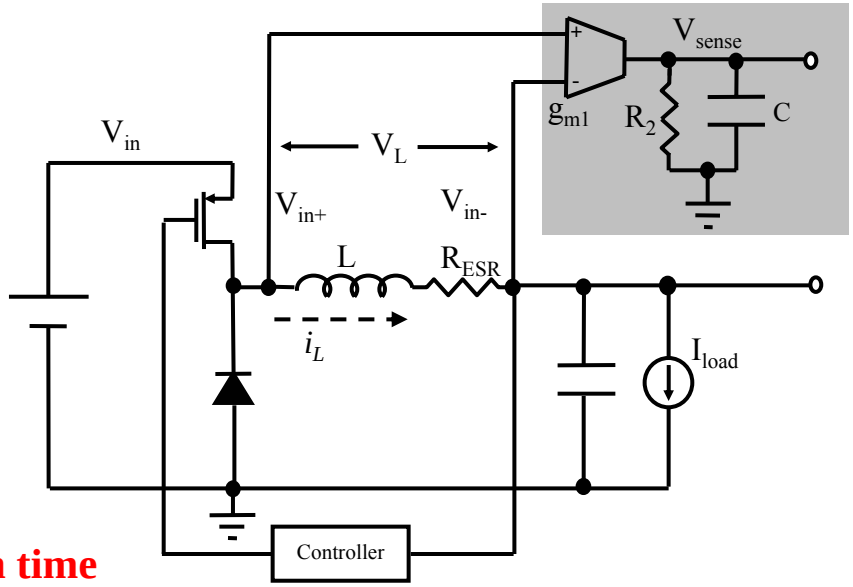
$$V_{sense} = g_{m1}R_2\left(\frac{1}{1+sR_2C}\right)V_L$$

$$I_L = \frac{1}{(R_{ESR}+sL)}V_L$$

If R_2 is tuned such that $L/R_{ESR}=R_2C$,

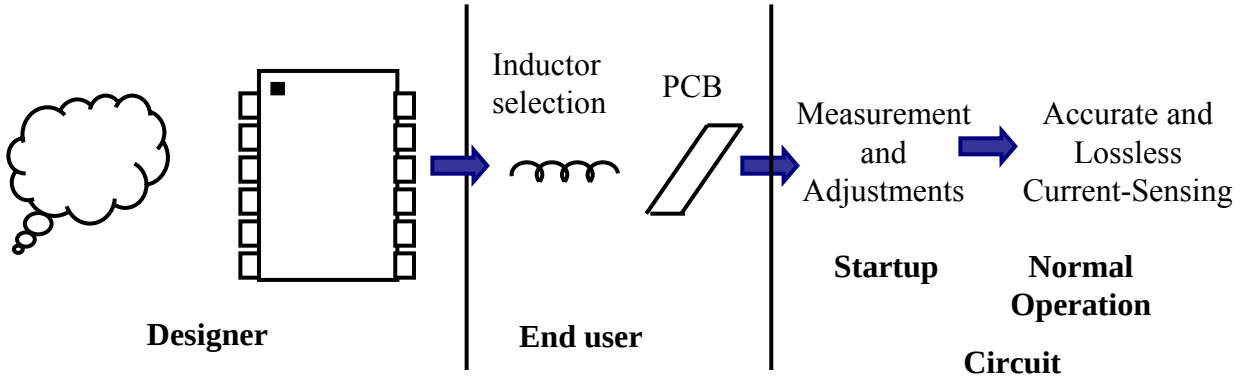
$$V_{sense} = (g_{m1}R_2)R_{ESR} \times I_L$$

If $(g_{m1}R_2)R_{ESR}=1\Omega$ $\rightarrow$ $V_{sense} = 1\Omega \times I_L$



Problem: L and R_{ESR} are not known at the design time

Solution: Measure them at the startup



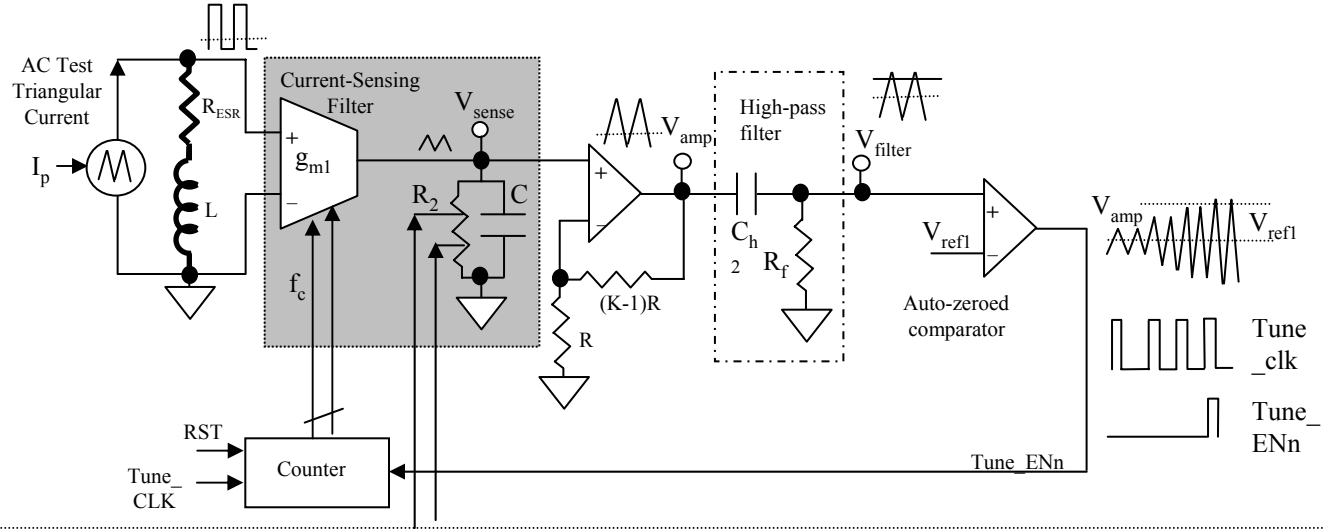
System - Startup

1. Tuning:

- Adjust the high frequency gain

Loop Forces: $K\frac{g_{m1}}{C}LI_p = V_{ref1}$

$$\frac{g_{m1}}{C}L = \frac{V_{ref1}}{KI_p}$$

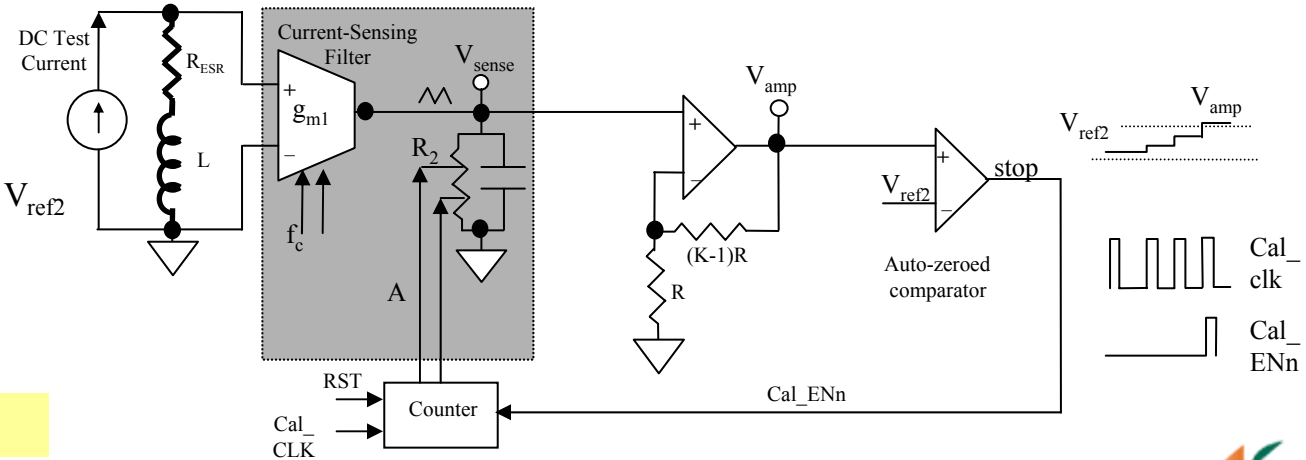


2. Calibration:

- Adjust the low frequency gain

Loop Forces: $K(g_{m1}R_2)R_{ESR}I_{test} = V_{ref2}$

If $\frac{V_{ref1}}{I_p} = \frac{V_{ref2}}{I_{test}}$

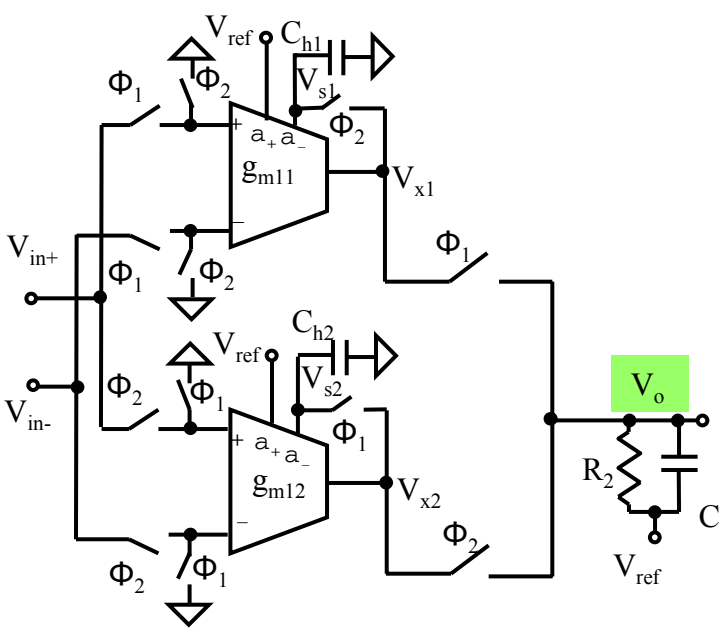


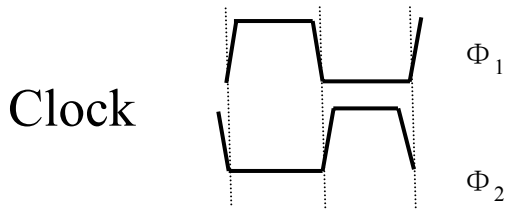
Matched BW: $L/R_{ESR}=R_2C$

Current-sensing gain: $gain = \frac{V_{ref2}}{KI_{test}} = \frac{V_{ref1}}{KI_p}$

GEDC Industry Advisory Board, April 2005.

Ping-Pong Operation - Offset Reduction

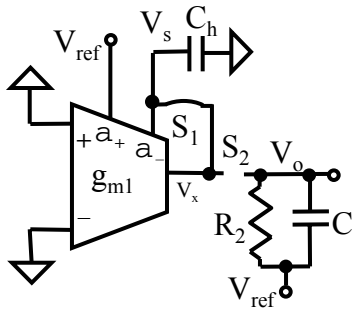




Auto zeroing phase

Offsets are stored at the hold capacitor

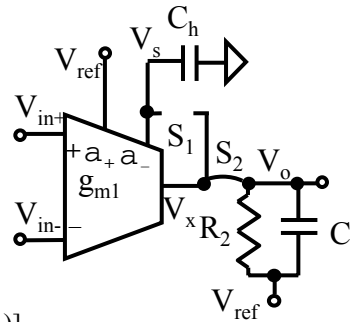
$$V_s = \left(\frac{g_{m1} R_o V_{os1} + g_{ma} R_o V_{os2} + g_{ma} R_o V_{ref}}{1 + g_{ma} R_o} \right) + V_{error}$$



Normal operation

Output voltage is

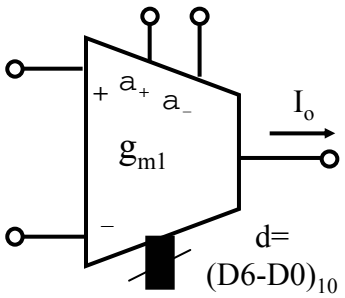
$$V_o = g_{m1} V_{in} (R_o \parallel R_2) + V_{os1} \frac{g_{m1} (R_o \parallel R_2)}{1 + g_{ma} R_o} + V_{os2} \frac{g_{ma} (R_o \parallel R_2)}{1 + g_{ma} R_o} - g_{ma} (R_o \parallel R_2) V_{error} + V_{ref} \left[1 - \left(\frac{1}{1 + g_{ma} R_o} \frac{R_2}{R_o + R_2} \right) \right]$$

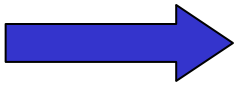


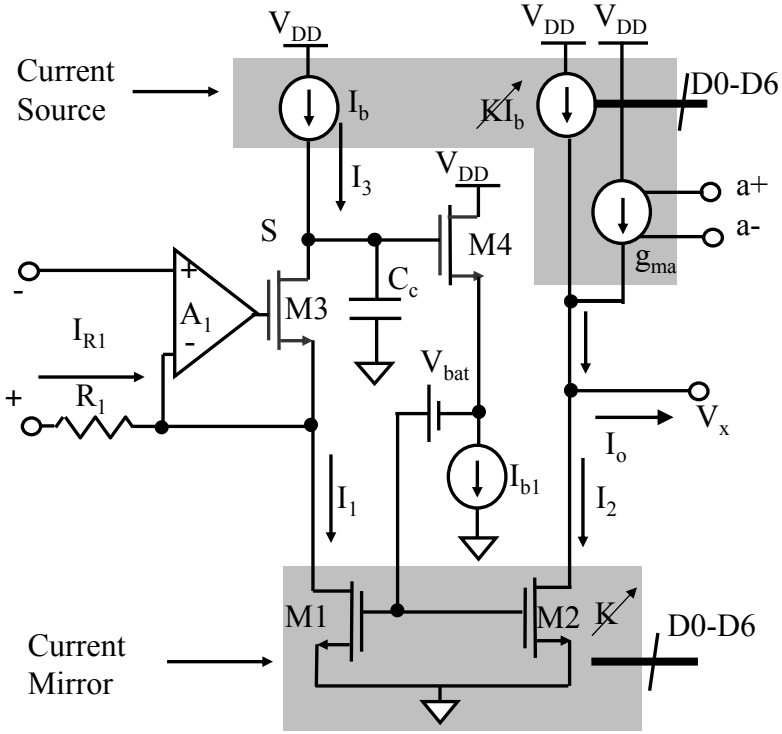
V_{os1}: main input offset
V_{os2}: auxiliary input offset
V_{error}: charge injection voltage error
g_{ma}: auxiliary path transconductance
R_o: g_{m1} output resistance
V_s: hold capacitor stored voltage
g_m: main path transconductance

GEDC Industry Advisory Board, April 2005.

G_{m1} Implementation(1)







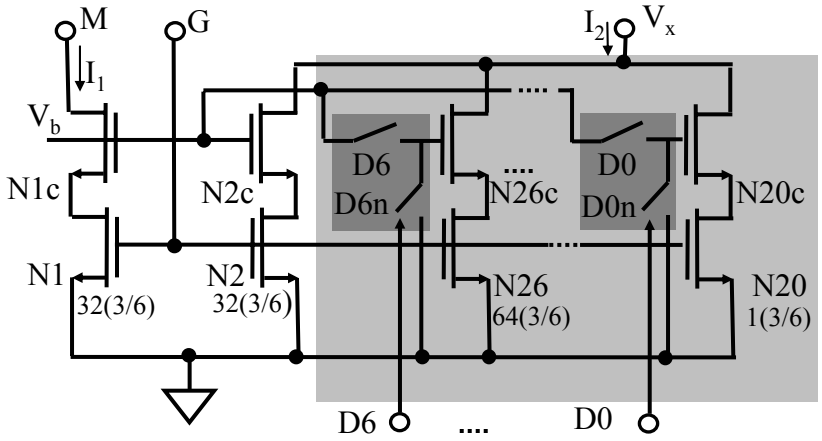
$$I_o = g_{m1}(V_+ - V_-) + g_{ma}(V_{a+} - V_{a-})$$

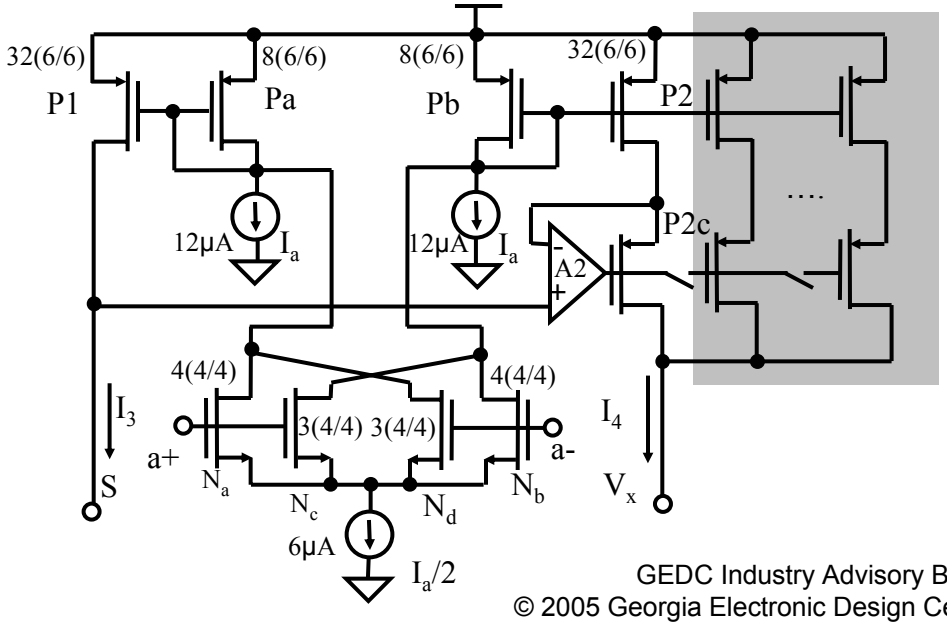
$$g_{m1} = f(d) = g_{m10} + g_{m11}\, d/128$$

+ and – : Main inputs
a+ and a-: Auxiliary path inputs
K is the current mirror gain

$$I_o = \frac{K}{R_1}(V_+ - V_-) + g_{ma}(V_{a+} - V_{a-})$$

G_{m1} Implementation(2)





Current Mirror

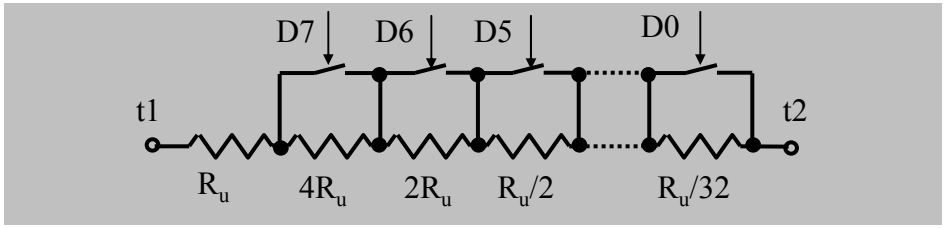
- Current mirror gain is adjusted digitally
- The switches are not in the signal path and do not effect the AC response

Current Source

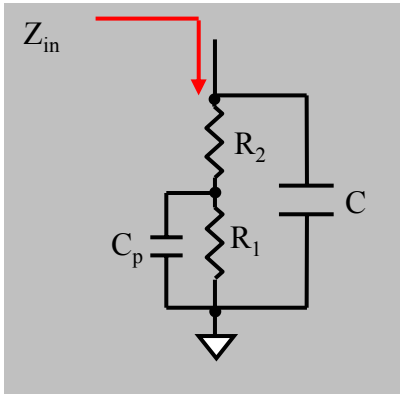
- Current source I_4 is adjusted digitally
- Transistors N_a- N_d form a current canceling differential pair with lower transconductance compared to simple differential pair
- Auxiliary offset path is formed in current sources

R_2-C

Digitally tunable resistor:



A large output capacitor (C) relative to the switch parasitic capacitance ensures that switch parasitic capacitance does not alter the ideal first order AC response



$$Z_{in} = \frac{R_1 + R_2}{1 + (R_1 + R_2)Cs} \left(\frac{1 + s(R_1 \| R_2)C_p}{1 + s(R_1 \| R_2)C_p \dfrac{C}{C + \dfrac{R_1}{R_1 + R_2} C_p}} \right)$$

Since $C >> C_p$ $\quad Z_{in} = \dfrac{R_1 + R_2}{1 + (R_1 + R_2)Cs}$

Simulation Results

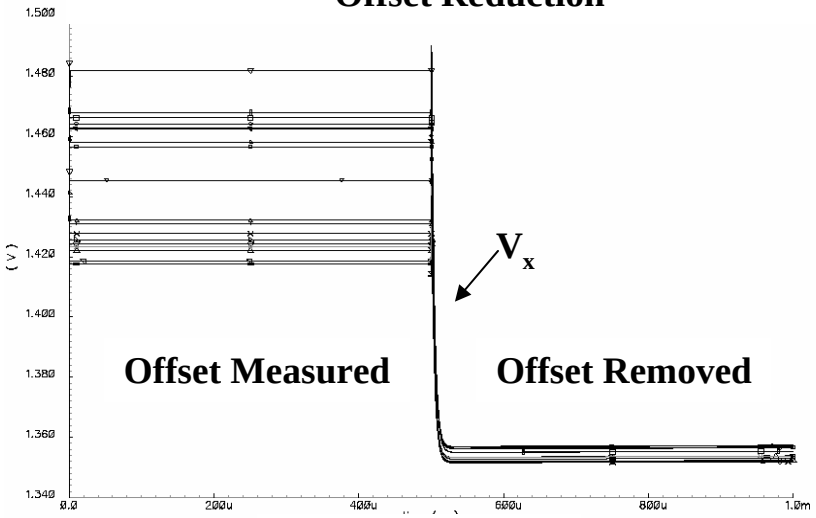
Important design values

L spread	2-6µH	R_2	325-2900KΩ
ESR spread	12-188mΩ	R_2 No. bits	8
R1 in g_{m1}	250KΩ	C	60pF
g_{m1} mirror ratio	1-5	C_{h1}, C_{h2}	6pF
Mirror No. bits	7	Clock freq.	1KHz

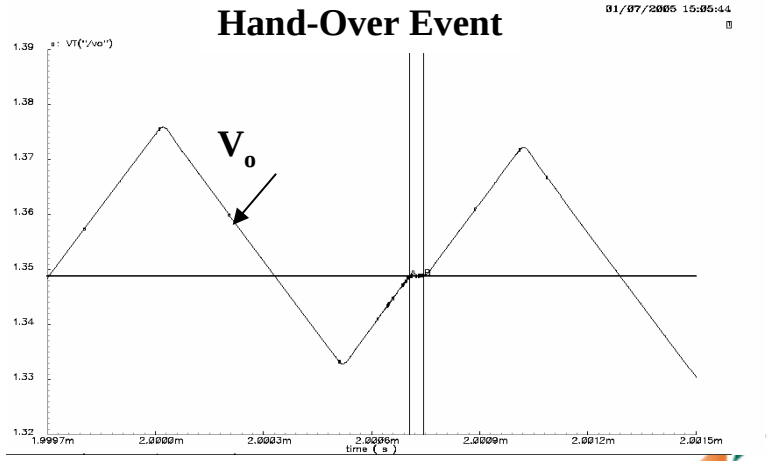
Summary of circuit performance and specifications

Technology	0.5µm CMOS
Supply Voltage	2.7-4.2V (Li-Ion)
Temperature range	-40° C to 125° C
Switching input (V_{in+}) CMR	0-V_{DD} (rail to rail)
Non-switching input CMR	0.8V-V_{DD}-1V (Nom: 1.5V)
Output-referred offset	<5mV
Nonlinearity ($\Delta g_{m1}/g_{m1}$)	<-67dB (for rail to rail ICMR)
BW programmability	1-5KHz, 30Hz steps
Gain programmability (V_o/V_{in})	2.5-40, 0.075 steps

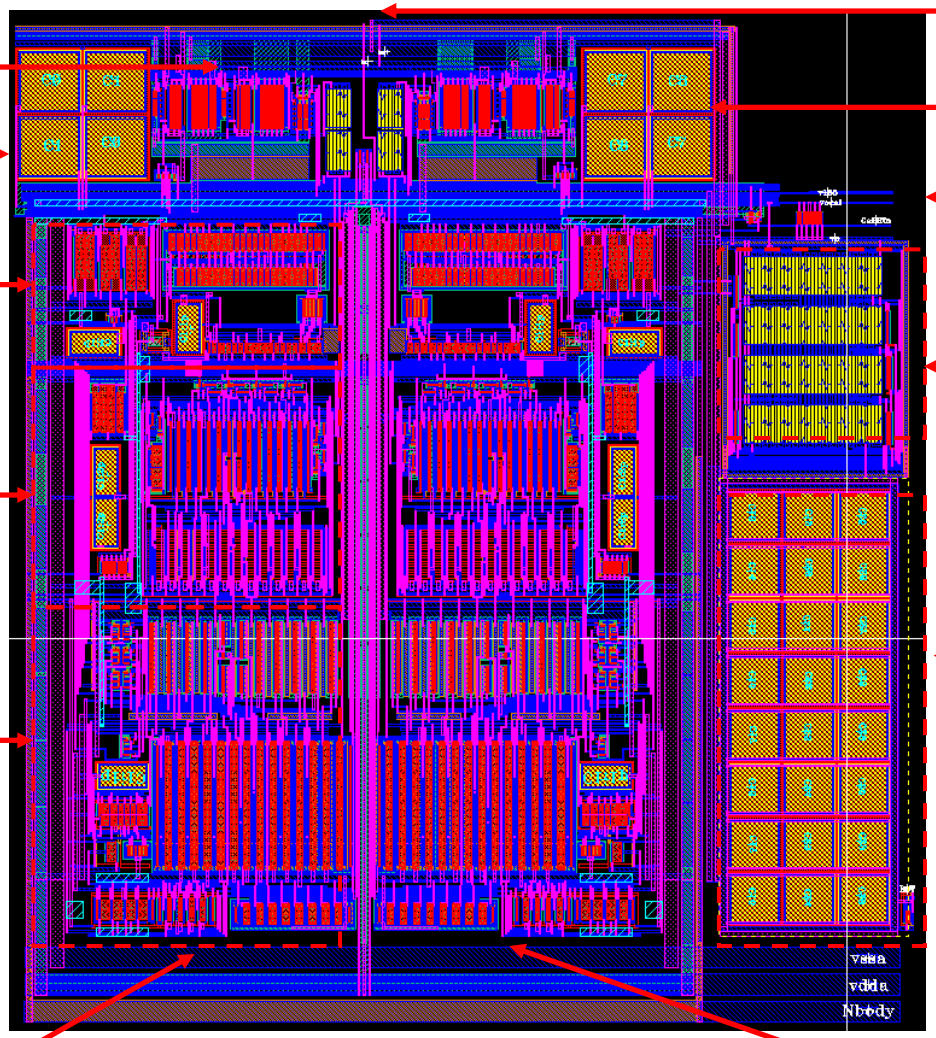
Offset Reduction



Hand-Over Event



Layout



Switches

C_h for g_{m11}

Amplifier A_1

Current Mirror

Current Source

g_{m11}

Input (V_{in+}, V_{in-})

C_h for g_{m12}

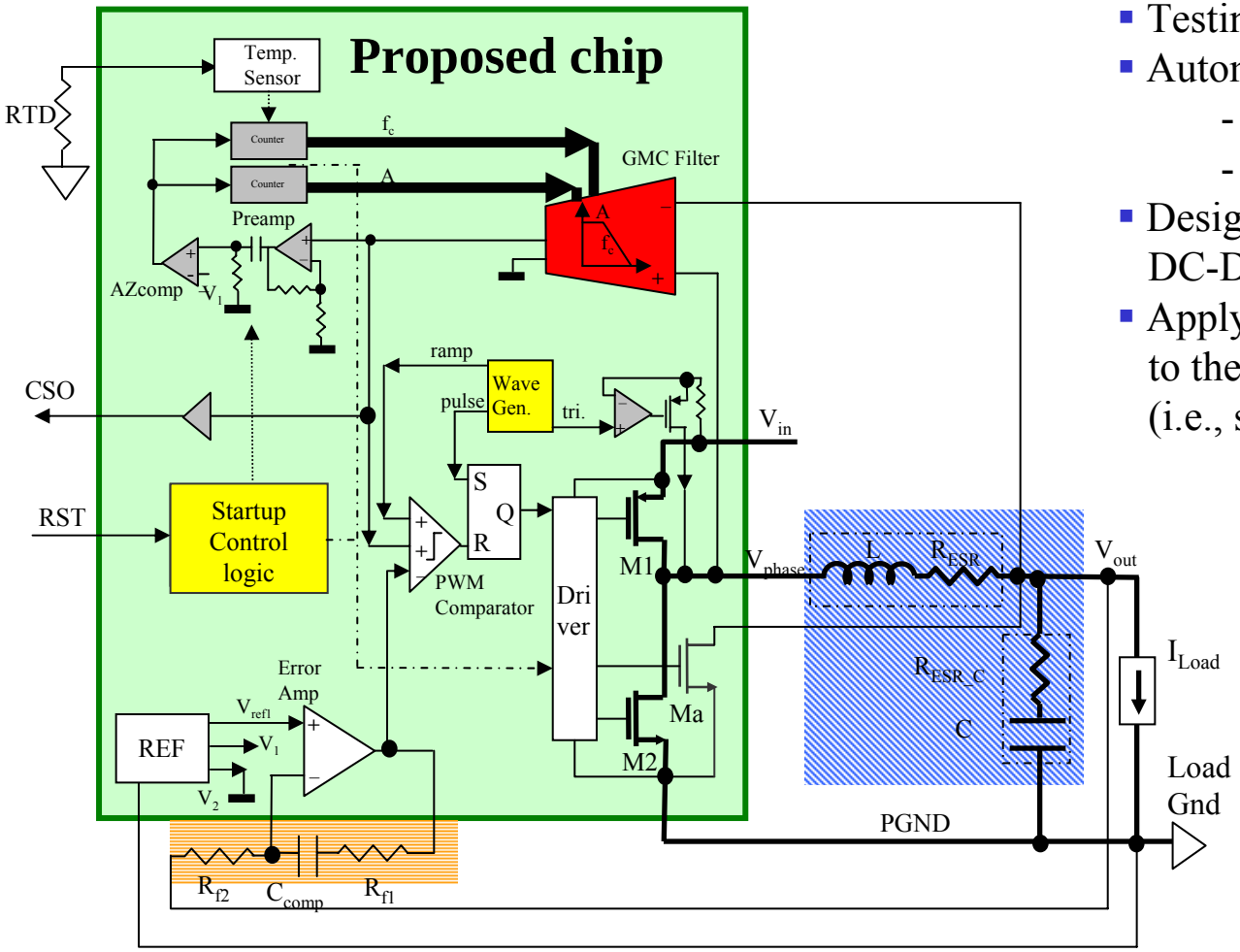
Output (V_o)

Output Resistor (R_2)

Output Capacitor (C)

g_{m12}

Future Work



- Testing g_m-C filter fabricated circuit
- Automatic programming circuit
  - Gain Calibration
  - Bandwidth Tuning
- Design of a current-mode buck DC-DC controller
- Applying the current-sensing filter to the switching regulator (i.e., startup control logic)