Fully Integrated Power-Saving Solutions for DC-DC Converters Targeted for the Mobile, Battery-Powered Applications

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Abstract

- **Motivation for Improving Efficiency in Mobile Applications**

  System-On-Chip (SOC)

  Low power demands, low cost, and compactness make SOC suitable for *portable, battery-powered applications*, like cellular phones, pagers, laptop computers, MP3 players, PDAs, etc.

  Low-voltage circuits

  Required to satisfy the demand for single battery operation and the ever decreasing breakdown voltages of state-of-the-art technologies

  Highly efficient, totally integrated DC-DC converters ***are strongly desired!***

  High Efficiency ➡ Low current drain ➡ Maximum battery life

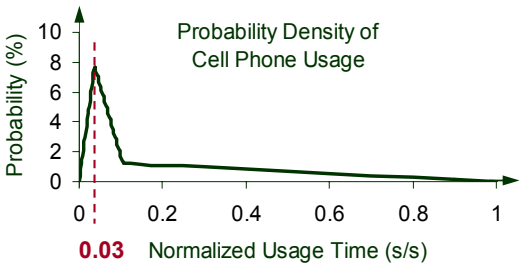
  Total integration ➡ Small size and weight ➡ Optimum portability

- **Research Focus**

  Develop ***power-saving techniques*** for ***low voltage*** DC-DC converters suitable for ***integrated solutions***.

Light load efficiency – Why is it important?

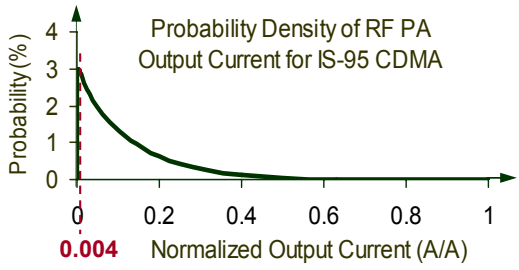
Cell phone usage survey [1]



Peak usage time (normalized) =
0.03 (s/s) or 300 min/month

Most people use the cell phone for small amounts of time

CDMA RF PA Output Characteristic [2]



Peak usage current (normalized) =
0.005 (A/A) or 7 dBm output power

Most of the time, the PA operates with small current

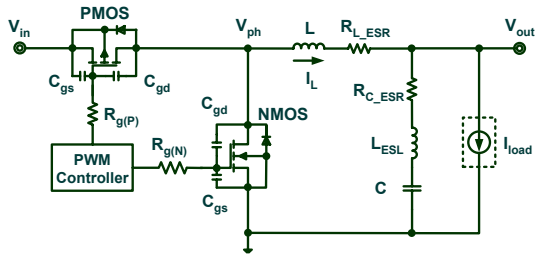
Improving ***light load efficiency is important*** for extending battery life**!**

[1] http://www.frs.org/headlines/SurveyPressRelease.doc

[2] J. Staudinger, et. al. "High efficiency CDMA RF power amplifier using dynamic envelope tracking technique," *IEEE International Symposium on Microwave Theory and Techniques*, Digest, 2000, pp. 873–876.

Power Losses – Where do they come from?

Synchronous buck converter with all the parasitic elements



Conduction Losses

(through resistive elements)

- PMOS on-resistance
- NMOS on-resistance
- Body diodes
- Inductor Equivalent Series Resistance (ESR)
- Capacitor ESR
- Gate resistances

Thermal Losses

- Cooling devices
- As T increases, R_{ON} thus conduction losses increase.

Efficiency

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}$$

Switching Losses

- **V-I overlap loss**
  Voltage falling and current rising overlap *vice versa* during MOSFET turn on/off.
- **Gate drive loss**
  Charging and discharging of gate capacitances during switching.

General Power Equations: [1]

- Load current: $P_{cond\_load} = D \times {I_{load}}^2 \times R_{eq}$
- RMS current: $P_{cond\_RMS} = D \times \frac{(\Delta I)^2}{12} \times R_{eq}$
- Body diodes: $P_{cond\_D} = t_D \times V_D \times \left(I_{load} + \Delta I / \sqrt{12}\right) \times f_S$
- V-I overlap loss: $P_{V-I} \approx t_x \times V_{in} \times I_{load} \times f_S$
- Gate drive loss: $P_{GD} \approx (16/3) \times C_{gs} \times {V_{in}}^2 \times f_S$

[1] M. Gildersleeve, H. P. Forghani-zadeh, and G.A. Rincón-Mora, "A Comprehensive Power Analysis and a Highly Efficient, Mode-Hopping DC-DC Converter," *IEEE Asia-Pacific Conference on ASIC*, 2002, pp. 153–156.

How to improve efficiency? – Existing techniques

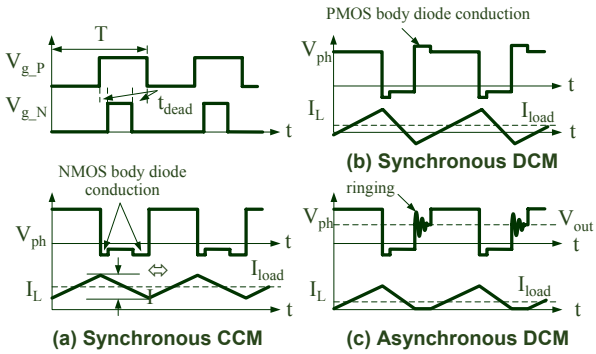
① Mode Hopping: Hop to most efficient mode based on operating conditions

-At high load:

Syn. CCM: Smaller ⇔I, thus
smaller conduction losses
➡ More efficient than DCM

-At light load:

Asyn. DCM: Smaller ⇔I, thus
smaller conduction losses
Also may decrease f_S, thus
smaller switching losses
➡ More efficient than Syn. DCM



➡ Load dependent ***Mode Hopping*** to keep high efficiency over wide load range

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Challenge: Need to sense I_L to determine the correct operation mode

One solution [1]: Disable NMOS periodically to force Asyn. DCM without current sensing
But converter latches in DCM even after enabling NMOS

➡ *Improvement* [2]: Disable NMOS after sensing ringing at V_{ph} to save *gate drive loss*

[1] T.G. Wang, X. Zhou, and F.C. Lee, "A Low Voltage High Efficiency and High Power Density DC/DC Converter," *28th Annual IEEE Power Electronics Specialists Conference*, Vol. 1, 1997, pp. 240–245.

[2] M. Gildersleeve, G.A. Rincón-Mora, Internal research report, Analog Integrated Circuit Laboratory, Georgia Institute of Technology, 02/2003

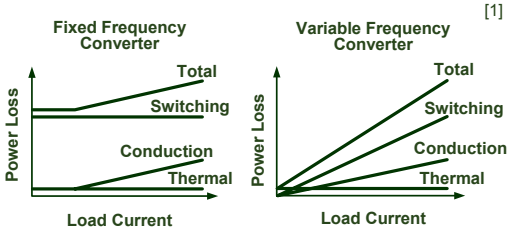
How to improve efficiency? – Existing techniques

② Variable Frequency

- Switching losses (✪ f_S) dominate at light loads

➡ Reduce f_S in proportional to I_{load}

[1]

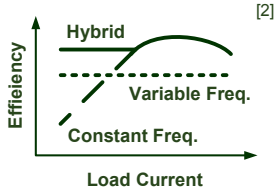


- Light load efficiency is significantly improved
- At heavy loads, switching losses are still high

③ Hybrid Control

- *Mode Hopping* + *Variable Frequency*
- Constant f_S at heavy loads
  Reduced f_S at light loads

[2]



- High efficiency over wide load range
- Complicated controller design

[1] B. Arbetter, R. Erickson and D. Maksimovic, "DC-DC Converter Design for Battery-Operated Systems," *26th Annual IEEE Power Electronics Specialists Conference*, Vol 1, 1995, pp. 103–109.

[2] T.G. Wang, X. Zhou, and F.C. Lee, "A Low Voltage High Efficiency and High Power Density DC/DC Converter," *28th Annual IEEE Power Electronics Specialists Conference*, Vol. 1, 1997, pp. 240–245.

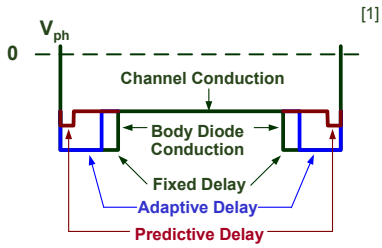
How to improve efficiency? – Existing techniques

④ Predictive Gate Drive (PGD) ™

- ***Fixed:***
  Preset the dead time and doesn't change
  ➡ Body diode conduction loss and reverse recovery loss

- ***Adaptive:***
  - Detect the body diode conduction and control the dead time in the *current* cycle accordingly
  - Internal logic delay

  ➡ Body diode conduction is minimized but still existent



- ***Predictive:***
  - Sense the body diode conduction in the *current* cycle and progressively reduce the dead time in the *next* cycle until no body diode conduction is detected

  ➡ • Virtually ***eliminate*** the NMOS Body diode conduction and reverse recovery losses
  Also help reduce the PMOS V-I overlap loss

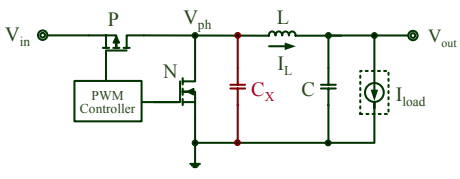
  - Extremely precise gate timing is crucial!

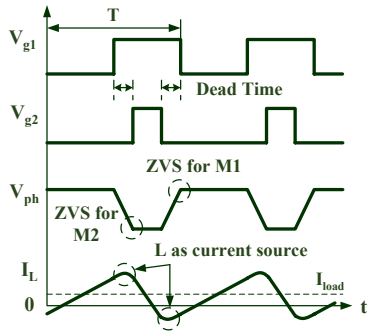
[1] Steve Mappus "Predictive Gate Drive™ Frequently Asked Questions," Application Report SLUA285, Texas Instruments, Feb. 2003

How to improve efficiency? – Existing techniques

⑤ Zero-Voltage Switching (ZVS): switch transistors when $V_{ds} = 0$

Synchronous buck converter with ZVS [1]





- ***Operation:***
  - Snubber capacitor C_x added at V_{ph} to slow down the voltage transition
  - Inductor L acts as a current source during dead time to charge/discharge V_{ph}
  - Both PMOS and NMOS are turned on when their $V_{ds} = 0$ ➡ *zero-voltage switching*

- ***Pros:*** • Virtually eliminate V-I overlap loss and body diode losses
  • Good for high f_S ➡ Small size and weight

- ***Cons:*** • Additional off-chip component
  • Charge/discharge C_x ➡ more switching loss
  • Operate in Syn. DCM ➡ more conduction loss
  ➡ Only suitable for light loads

- ***Challenges:***
  - Adaptive dead time control
  - Fast gate drive

[1] A.J. Stratakos, S.R. Sanders and R. Brodersen, "A Low-Voltage CMOS DC-DC Converter for a Portable Battery-Operated System," *25th Annual IEEE Power Electronics Specialists Conference*, Vol. 1, 1994, pp. 619–626.

Comparative Evaluation of Power Saving Techniques

Power Losses (mW)	Operation Condition (V_{in}=3.3V)				Power Saving Techniques				
	I_{load} = 1 A (CCM)		I_{load} = 500 mA (DCM)		①	②	③	④	⑤
	f_S= 1 MHz	f_S= 500 kHz	f_S= 1 MHz	f_S= 500 kHz	Mode Hop	Vari. Freq.	Hybrid Ctrl.	PGD™	ZVS
R_{PMOS}	**80 (35%)**	**79 (45%)**	**24 (21%)**	**30 (40%)**	✓		✓		
R_{NMOS}	28 (12%)	29 (17%)	5 (4%)	7 (9%)	✓		✓		
V_{Diode}	22 (10%)	9 (5%)	14 (13%)	7 (9%)	Good	Good	*Better*	***Best***	*Better*
R_{L_ESR}	12 (5%)	12 (7%)	4 (4%)	4 (5%)	✓		✓		
R_{C_ESR}	7 (3%)	8 (5%)	5 (4%)	5 (7%)	✓		✓		
R_{Gate}	3 (1%)	2 (1%)	3 (3%)	1 (1%)	✓		✓		
V-I Ov.	**73 (32%)**	**33 (19%)**	**52 (47%)**	**19 (26%)**		*Better*	*Better*	Good	***Best***
Gate Dr.	5 (2%)	2 (1%)	5 (4%)	2 (3%)		✓	✓		
Tot. Cond.	**152(66%)**	**139(80%)**	55 (49%)	**55 (73%)**	***Best***	OK	***Best***	*Better*	Good
Tot. Sw.	78 (34%)	35 (20%)	**57 (51%)**	20 (27%)	OK	*Better*	*Better*	Good	***Best***
Total Loss	230	174	112	75					
η	86.4%	90%	89.4%	92.6%					

Summary

- **Rank of Losses:**
  - **#1 Loss: PMOS Conduction Loss ➡ Reduce R_{PMOS}**
  - **#2 Loss: V-I Overlap Loss ➡ Zero-Voltage Switching**
  - **#3 Loss: NMOS Conduction Loss ➡ Reduce R_{NMOS}**
  - **#4 Loss: Body Diode Losses ➡ Novel gate drive / dead time control**
  - **#5 Loss: ESR Conduction Losses ➡ Reduce R_{ESR}**
  - **#6 Loss: Gate Drive Loss ➡ Reduce parasitic C and/or f_S**
- **To improve *overall efficiency* ➡ Improve *light load efficiency!***
- **At heavy loads: Conduction Losses ↻ f (current , …) dominate**
  At light loads: Switching Losses ↻ f (frequency , …) dominate
- ***Hybrid Control* : best for reducing conduction losses**
  ZVS* : best for reducing switching losses** } ➡ ***Combine?