A High Efficiency, Linear RF PA with a Power-Tracking, Dynamically Adaptive Buck-Boost Supply

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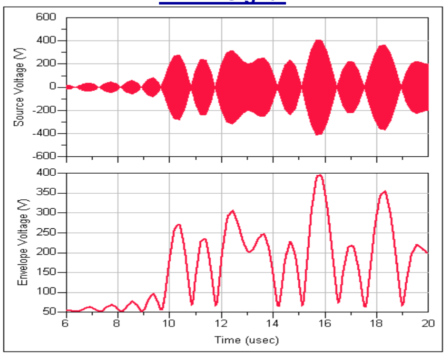
Abstract

- **Battery-operated portable devices, e.g., cell phones, pagers, PDAs demand energy-efficient linear power amplifiers (PAs):**
  - **Increases battery life**
  - **Decreases cost (e.g., smaller heat sinks, less PCB real estate)**
- **PA efficiency is enhanced by dynamically changing both the bias current and supply voltage, *on-the-fly*:**
  ⇒ **Dynamically adaptive DC-DC converter**
- **The required PA supply voltage at any time can be higher or lower than the battery voltage (Li-ion: 2.7-4.2 V):**
  ⇒ **Non-inverting, buck-boost converter**
- **Experimental results of a prototype PA:**
  - **Meets CDMA IS-95 ACPR requirements with 27 dBm maximum output power.**
  - ***Five times increase in battery life.***

CDMA PA Requirements

CDMA Signal



- Power control is essential to CDMA systems.
- Maximum use with output power of about 5 dBm.
  - PA designed for peak power is inefficient at back-off.
  - Optimize in the vicinity of the peak.
- For longer battery life, PA must be efficient across wide loading conditions.

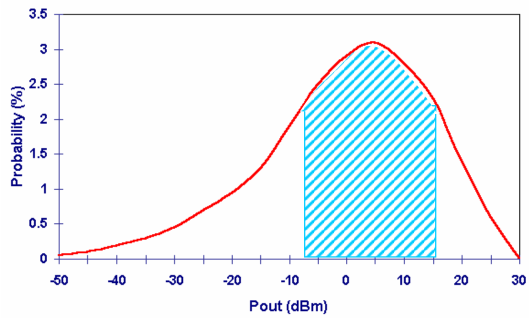
- Large peak to average ratio.

→ PA designed for the peaks will be inefficient at the valleys.

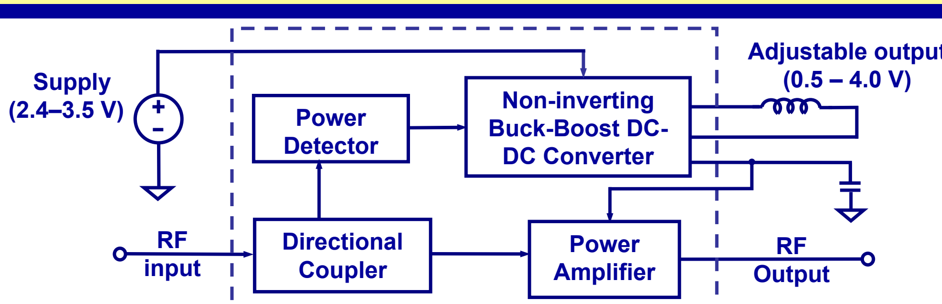
→ Intuitively, goal should be to maintain high efficiency throughout.

⇒ Control the operation of the PA by following the envelope for all power levels.

PA output power distribution profile



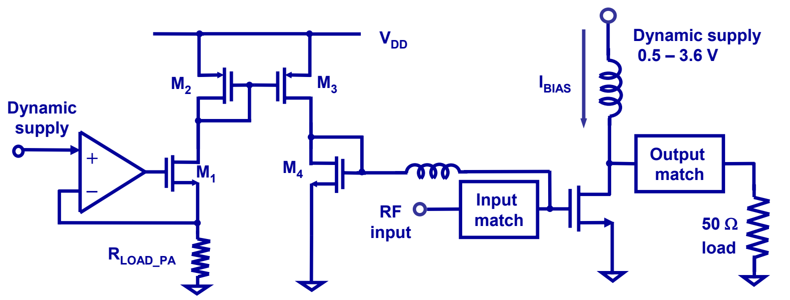
Power-Tracking, Efficient Linear PA



- Why power-tracking?
  - It requires smaller converter bandwidth, therefore lower switching frequency, hence incurs lower switching losses which extends battery life.
- Operation
  - The RF signal is split between the PA and the power detector via the directional coupler.
  - The detector generates a DC voltage proportional to the RF power.
    - Control signal for the converter which defines the PA supply voltage and bias current.
  - As input power varies, the converter control signal changes, ultimately adjusting the PA supply voltage and bias current.

Prototype System Implementation

- Discrete non-inverting, synchronous, buck-boost converter.
- Branch-line, micro-strip, directional coupler: 5 dB coupling coefficient.
- Commercial RF power detector: LTC 5505-2.
- RF PA evaluation module: NEC 55020279A LDMOS Transistor.



Dynamic gate bias generation circuit

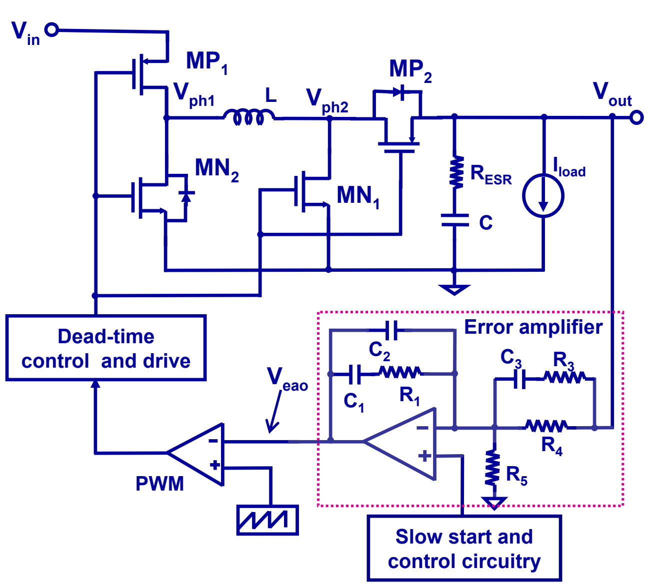
Single ended Class-A Amplifier

- Class AB and B modes of operation are not linear enough to meet the ACPR requirements for CDMA.
  - ACPR performance of class AB experimental PA is found to be 5 dB greater than the desired value (-40 dBc).
- Maximum efficiency (with desired linearity) is achieved by operating the PA on the boundary of class A and AB.

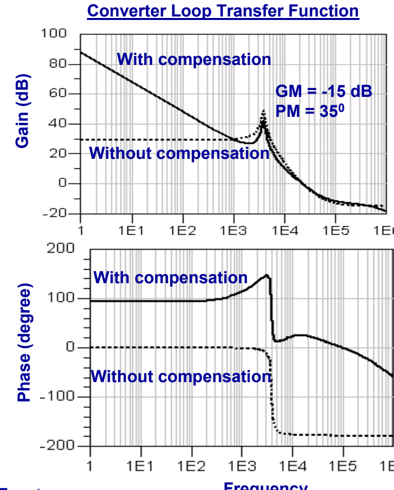
Non-inverting Buck-Boost Converter

Converter Design Considerations:

- Small output ripple to reduce PA output distortion.
- Fast response to track power change.
- High efficiency to increase battery life.



Converter Loop Transfer Function

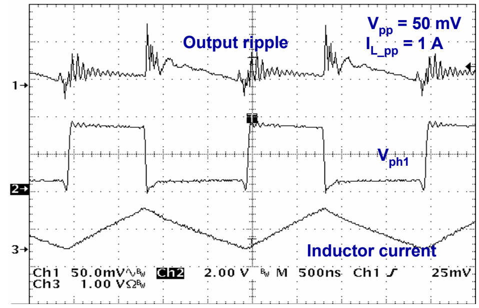


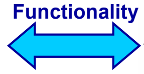
Salient Features:

- Type–III network (three poles and two zeros) for compensation.
- Dead-time control scheme to prevent *shoot-through* current.
- Duty-cycle is limited to less than unity to prevent catastrophic failure (shorting V_{in} to ground via MP_1, MN_1 and L).

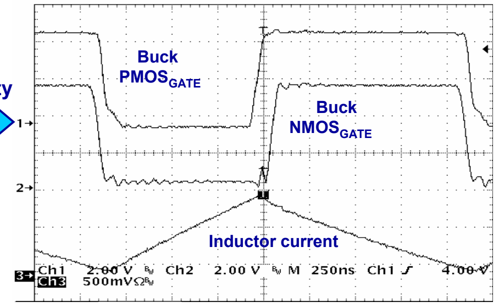
Experimental Results – Converter

Converter Waveforms

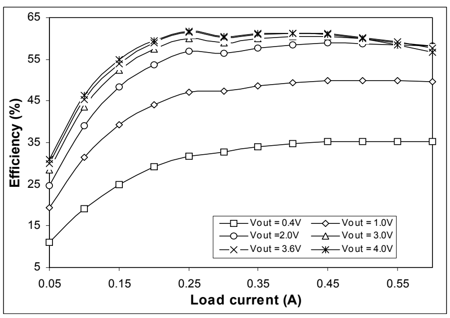




Dead-Time Control



Efficiency for Various Output Voltages

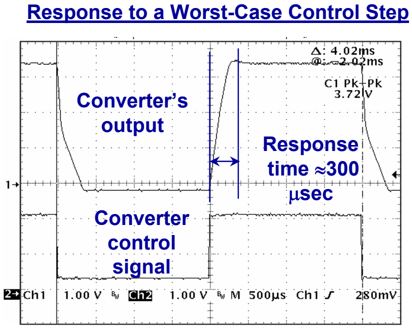


⇒ Most of the output ripple is due to the ESR of the output capacitor.
- Reduce ESR to decrease the output ripple.

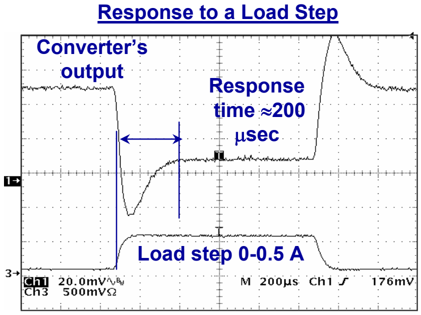
⇒ Efficiency can be further improved with
- Switches of lower ON resistance.
- Advanced dead-time control techniques.
- Zero-voltage switching during light loads.

Experimental Results – Converter

Response to a Worst-Case Control Step



Response to a Load Step



⇒ Converter responds to worst-case control reference within 300 μsec

⇒ Converter responds to a load step of 0-0.5 A within 200 μsec having only 40 mV transient error in the output voltage

Summary of prototype converter results

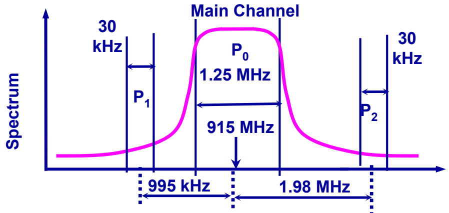
Specifications	*Target*	*Expt.*
Input voltage	2.4-3.5 V	2.4-3.5 V
Output voltage	0.4-4.0 V	0.4-4.0 V
Output voltage accuracy	–	0.5–3 %
Peak-to-peak ripple	≤ 100 mV	≤ 100 mV
LNR (2.4–3.4 V)	–	≤ 0.3 %
LDR (0.05–0.6 A)	–	≤ –1.0 %
Efficiency	–	10-62 %
Worst case control step	≤ 300 μsec	≤ 300 μsec
Response to load step	≤ 300 μsec	≤ 200 μsec

⇒ The error in low output voltages is due to the PCB parasitic resistance, offset voltage of the error amplifier and finite loop-gain of the feedback loop.

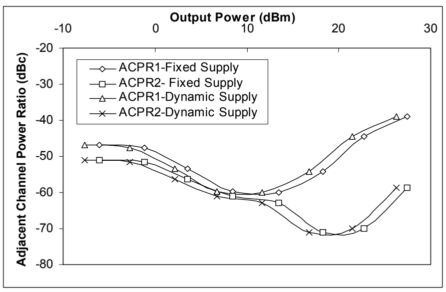
Experimental Results – PA System

ACPR: Measure of CDMA PA Linearity

ACPR is defined as the ratio of adjacent channel power to the main channel power: $ACPR_1 = P_1/P_0$, $ACPR_2 = P_2/P_0$.

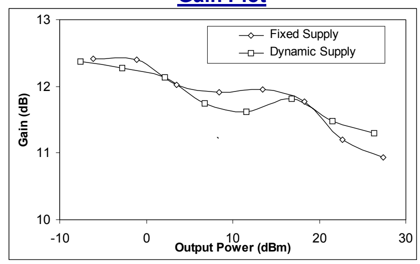


ACPR Plot



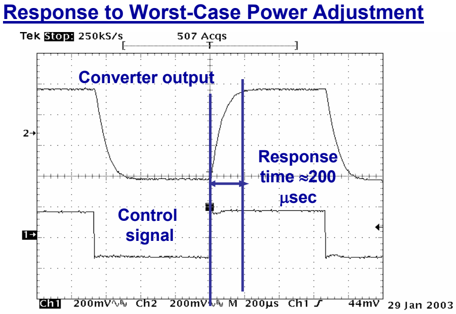
- ACPR degradation is marginal for the dynamic supply PA with respect to the fixed-supply PA

Gain Plot



- Gain degradation is marginal with dynamic supply

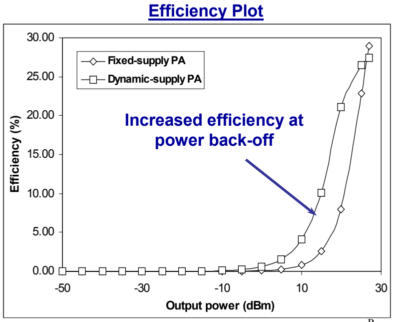
Response to Worst-Case Power Adjustment



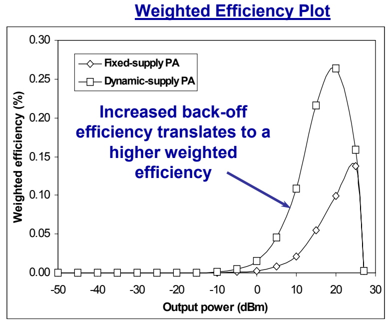
- Converter responds within 200 μsec

Experimental Results – PA System

Efficiency Plot

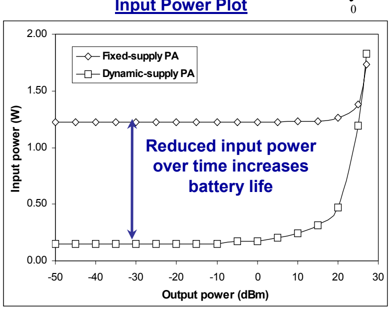


Weighted Efficiency Plot

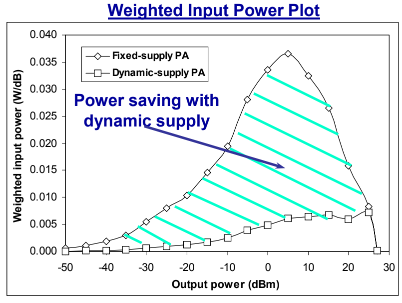


$$\text{Average Efficiency} = \frac{P_{out\_avg}}{P_{in\_avg}} = \frac{\int_0^{P_{out\_max}} P_{out}\, p(P_{out})\, dP_{out}}{\int_0^{P_{out\_max}} P_{DC\_IN}(P_{out})\, p(P_{out})\, dP_{out}}$$

Input Power Plot



Weighted Input Power Plot



⇒ Peak efficiencies of fixed-supply and dynamic-supply PA are 29 and 27.5 %, respectively.

⇒ At lower output power, the dynamic-supply PA operates with a reduced voltage and current, thereby decreasing the input power and consequently increases efficiency.

⇒ Further improvement in efficiency can be accomplished by increasing converter's efficiency and dynamic range of the power detector.

Conclusions

Efficiency improvement comparison

Schemes	η_{fixed_supply}	η_{dyn_supply}
AlGaAs/InGaAs PA with buck-converter	2.2 %	11.2 %
GaAs HBT PA with boost converter	3.89 %	6.38 %
LDMOS PA with buck-boost converter*	1.74 %	8.67 %

*This work

Fixed-Supply PA

Battery's low, Plug it back up!

Dynamic-Supply PA

Let's talk!

- Improvement in the average efficiency directly translates into *five times increase in battery life.*
- Power-tracking scheme requires a lower switching frequency converter.
  ⇒ Increased light load efficient, thereby longer battery life.
- Non-inverting, buck-boost converter is needed to operate the system at its peak performance independent of the battery state –freshly charged to close to fully-discharged condition–.
- *Future Work:* Monolithic solution of the efficient linear power amplifier system targeted for single-cell NiMH/NiCd battery (0.9 –1.8 V).