Integrated Linear Regulators: Design Recipes for High PSRR Performance

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Abstract

The **analytical expressions** that have been derived for the **power supply ripple rejection** (PSRR) of typical linear regulators show that the **PSRR is closely related** to the **open-loop gain** of the system – specifically, the dc gain, poles and unity gain frequency. The analysis reveals **important design principles for high PSRR** regarding the selection of the **optimal opamp** for a particular output device, size of the output device, size of the output capacitor and **placement of open-loop poles**.

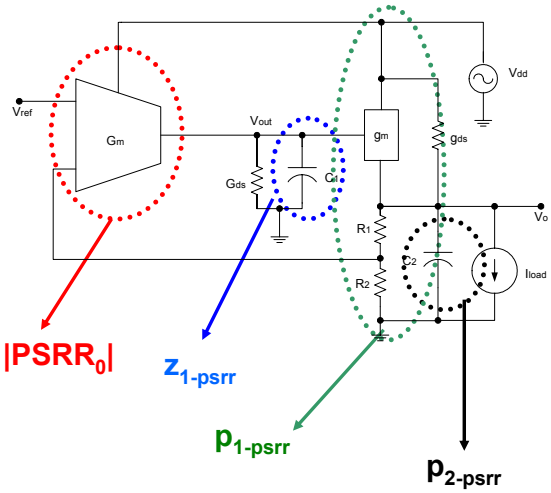
Introduction

Linear regulators are integral components of power management circuits.

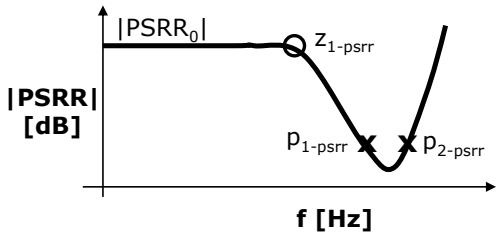
Rising market demand for portable products is pushing systems towards increasing integration, leading to the development of SoC (System-on-Chip) and SoP (System-on-Package) applications.

These SoC and SoP environments are inherently very noisy and hence require regulators that shield load circuit from power supply noise. This makes it imperative to study the PSRR of regulators.

Origin of PSRR in a Typical Linear Regulator



- $z_{1\text{-psrr}}$: As opamp gain degrades beyond it's dominant pole, the regulated output resistance increases, leading to a decrease in the PSRR.
- $p_{1\text{-psrr}}$: Increase in the output resistance ceases at the unity gain frequency (UGF) of the system, when the opamp can no longer regulate the loop.
- $p_{2\text{-psrr}}$: The output capacitor conducts the output ripple to ground, thereby enhancing the PSRR further.

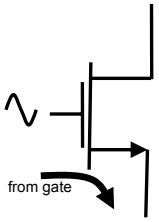


Output Device

The output of a linear regulator may consist of either an NMOS output stage (which affords unconditional stability due to it's low output impedance) or a PMOS output stage (which allows low voltage i.e. low drop-out, operation).

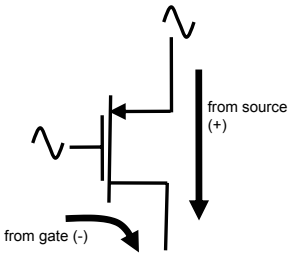
NMOS DEVICE

- voltage follower
- ripple feedthrough from gate to source (gain unity)
- **REDUCE RIPPLE AT GATE !!!**



Non-LDO topology

LDO topology

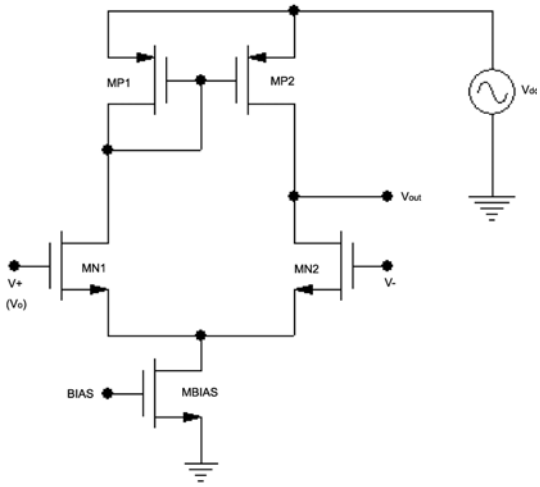


PMOS DEVICE

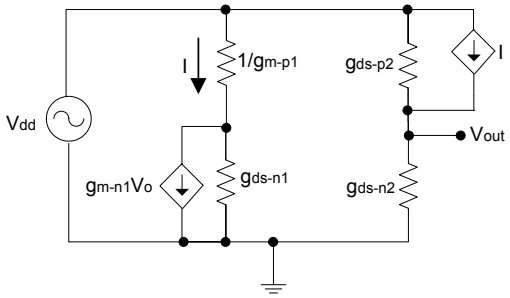
- two gain paths
- source directly connected to V_{dd}
- gain (source → drain) = - gain (gate → drain)
- **PRESENT CORRELATED AT GATE TO CANCEL OUT IT'S EFFECT !!!**

Conventional OTA

Schematic



Small Signal Model

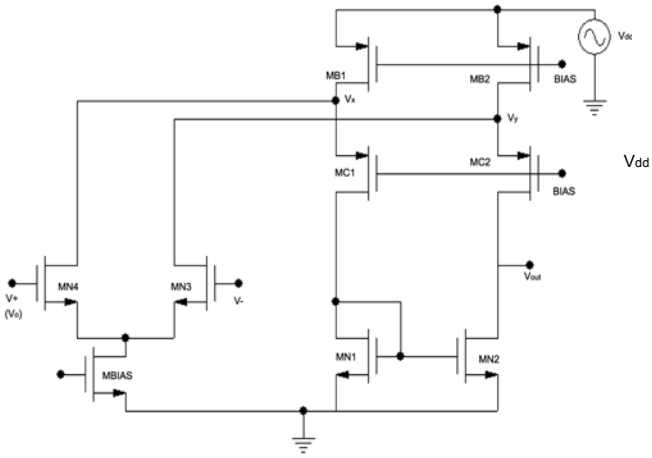


$$V_{out-amp} = V_{dd} \pm G_m R_{ds} V_o$$

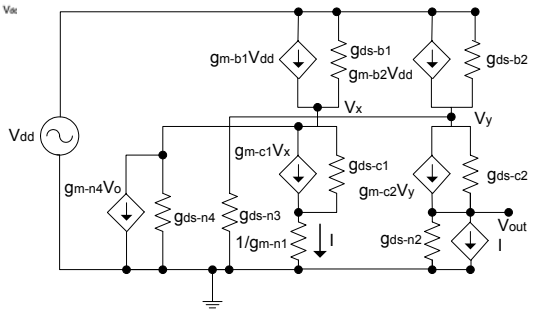
NOTE: The feedthrough of the supply ripple to the output is unity!

Folded OTA

Schematic



Small Signal Model



$$V_{out-amp} = \pm G_m R_{ds} V_o$$

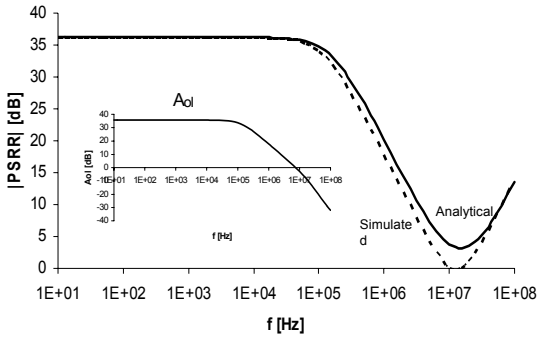
NOTE: There is no feedthrough from of the supply ripple to the output of the folded OTA!

Results of Analysis

Device	OTA	$\lvert PSRR_0 \rvert$	$z_{1\text{-psrr}}$	$p_{1\text{-psrr}}$	$p_{2\text{-psrr}}$
PFET	Conv.	$G_m R_{ds} g_m r_{ds}$	p_1	UGF	p_2
	Folded	$G_m R_{ds}$	$g_m r_{ds} p_1$	UGF	p_2
NFET	Conv.	$G_m R_{ds}$	$g_m r_{ds} p_1$	UGF	p_2
	Folded	$G_m R_{ds} g_m r_{ds}$	p_1	UGF	p_2

- p_1: dominant pole (bandwidth of opamp)
- p_2: output pole (due to C_2)
- UGF: Unity Gain Frequency of system

Simulated vs. analytical results of PFET + conventional OTA



Conclusion:

Use <u>conventional OTA for LDOs</u> (i.e. PMOS output stages) and <u>folded OTA for non-LDO</u> topologies (NMOS output stages) for high PSRR!!

Design Conclusions and Challenges

For LDOs, use an OTA that presents a ripple at the gate of the PMOS output device to cancel feedthrough from the supply. For a higher PSRR bandwidth, use a folded OTA, at the expense of dc PSRR.

Other design notes for high PSRR -

- Use an **OTA with high gain**.
- Try to keep **p_2 and UGF as close as possible**.
- **Increase C_{out} to shunt as much feed through signal to ground as possible.**

These requirements are **potentially dangerous to the stability** of the regulator.

Conclusions

- **Conventional OTAs** are provide higher PSRR in **LDOs** than folded topologies.
- The **dc PSRR** is determined by the **open-loop dc gain** of the system. The **PSRR zero** lies at the **dominant pole** of the system, while the **next two poles** lie at the **UGF and output pole** respectively.
- **Caution** needs to be exercised to maintain the **stability of the regulator** while designing the regulator for a high PSRR performance.