

PROCEDURES AND POLICIES FOR SUBMITTING CHIP DESIGNS TO MOSIS FOR FABRICATION

Prof. G.A. Rincón-Mora
Georgia Tech Analog & Power IC Design Lab

Step 1: Select desired process technology available through MOSIS (www.mosis.org).

Table 1. List of processes typically used.

Technology	Notes	Size (mm)	Area (mm ²)	Cost
0.50 μm AMI			5	\$3,250
			> 5	\$650 x area
1.50 μm AMI	NPN available	2.2 x 2.2		\$600
		4.6 x 4.7		\$2,300
		9.4 x 9.7		\$9,000
0.35 μm TSMC	Low threshold voltages	3 x 3	9	\$6,900
		4 x 4	16	\$11,040

Step 2: Submit 1 PDF Project Proposal for each chip design to MOSIS through the group's Technical Point of Contact (TPOC) at least 3 weeks prior to the desired fabrication run (sample proposal is appended). Use the following format:

- a. The account number must appear in the body of the e-mail message accompanying the proposal and not in the subject line/heading or anywhere in the proposal (not even on the cover sheet).
- b. Proposals are generally 3 pages in length, but may be longer.
- c. They should contain the following sections:
 - i. Project description.
 - ii. Fabrication process.
 - iii. Packaging requirements.
 - iv. Estimated project size (i.e., chip size: length and width).
 - v. Simulation plans.
 - vi. Test and characterization plans.
- d. Include a cover sheet (not part of the page count) with proposal stating:
 - i. Design for MOSIS Educational Program (Research)
 - ii. Project Title
 - iii. Prepared by: (list of students and faculty involved)
 - iv. Date of Submission: (Date proposal is sent to mep-research-proposal@mosis.org)

Step 3: If approved, MOSIS will send an e-mail notification with a Proposal ID to the TPOC with a carbon-copy to Prof. Rincón-Mora.

Step 4: Submit your design through the MOSIS website and include the Proposal ID in the submission form (www.mosis.org).

Step 5: MOSIS provides a number of packaging options – typically, open-cavity packages are used, either of SOIC or DIP type. To get MOSIS to package parts, send a purchase order (PO) through Prof. Rincón-Mora's administrative assistant for the appropriate amount to MOSIS using fax number +1-310-823-5624 (Attention: MOSIS Order Desk). Also, in the SPECIAL HANDLING field of the UPDATE web form specify the package name, quantity to be packaged, and the PO number. For example, SPECIAL HANDLING: DIP28, package 20 parts,

PO # 12345-r01. Table 2 presents a list of typically used packaging options provided by MOSIS along with their unit cost.

Table 2. Packages typically used.

Package	Part ID	Part Number	Discounted Cost
28-Lead SOIC	OCP_SOIC28A	3682	\$ 36
28-lead DIP	DIP28	2007	\$ 21
40-lead DIP	DIP40	2013	\$ 23

Step 6: As soon as you finish obtaining taking your measurements, submit a test report (or resulting publication) in PDF format through the TPOC for each chip design fabricated (sample report appended). This report is a minimum of 3 pages in length.

Please submit **ALL** designs through the **RESEARCH ACCOUNT** only and do not correspond with MOSIS customer support directly. Instead, consult with other group members for any questions relating a MOSIS submission. If dire circumstances prevail, before contacting any one else, ask the TPOC to consult with Georgia Tech's MOSIS Account Manager's representative for advice (usually a GRA reporting to Prof. Steve DeWeerth). This policy is in place to minimize the burden on MOSIS Customer Support, since they have been kind enough to allow Georgia Tech access to these process technologies and we are extremely grateful to them for this.

References

- <http://www.mosis.org/products/mep/mep-procedure-guide-research.html>
- <http://www.mosis.org/products/mep/mep-research-proposal.html>
- http://www.mosis.org/orders/purchase_orders/
- http://www.mosis.org/orders/prices/packaging/price_domestic_ceramic.html

**A Simple, Low-Voltage Scheme to Obtain High Power
Supply Ripple Rejection over Wideband Frequencies**

Prepared by: Vishal Gupta, Iván Alcón-Mora

Institute: Georgia Institute of Technology

Date Submitted: 10/04/2005

Sample Proposal

A SIMPLE, LOW-VOLTAGE SCHEME TO OBTAIN HIGH POWER SUPPLY RIPPLE REJECTION OVER WIDEBAND FREQUENCIES

This project aims to design and test a strategy to obtain high power supply ripple rejection (PSRR) performance from a conventional low-dropout regulator over a wide range of frequencies. A summary of the requirements of this project are presented in Table 1.

Table 1. Requirements for project.

PARAMETER	REQUIREMENT
Fabrication Process	AMI 0.5 μ m
Packaging Requirements	40 pin DIP
Project Size	1.5mm x 1.5mm
Project Description	Refer Section I.A, I. B
Simulation Results	Refer Section I. C
Test Plans and Procedure	Refer Section II

I. PROJECT DESCRIPTION

A. Motivation

The 21st century has witnessed an explosion in the demand for portable applications such as cellular phones and personal digital assistants (PDAs). The principal requirements for these applications are low cost, high integration, and small size [1]. These requirements are pushing the design of SoCs, where dense analog and digital circuits are fabricated on the same die. These SoC environments are plagued by noise, generated by the switching of digital circuits, RF blocks, and dc-dc converters, that can have amplitudes of the order of hundreds of millivolts and frequency components in the range of tens of kilohertz to hundreds of megahertz [2]. This noise, propagated onto the supplies through crosstalk, deteriorates the performance of sensitive analog blocks, like the synthesizer and VCO, and manifests itself as jitter in their outputs [4]. This jitter, in turn, deleteriously impacts critical system specifications like the selectivity of the receiver, spectral purity of the transmitter, and phase error tolerance of digital circuits [4]. In such an environment, a linear regulator is entrusted with the task of shielding noise-sensitive blocks from high frequency fluctuations in the power supply. This makes the design of linear regulators that have a high PSRR over a wide frequency range extremely critical for high system performance.

B. System Description

NMOS device M_{CAS} , shown in Fig. 1, decouples the entire linear regulator from fluctuations in the power supply through its cascoding effect (effective series resistance), thereby increasing PSRR over a wide range of frequencies [4]. The charge pump, described next, boosts the voltage at the gate of M_{CAS} to yield low dropout performance.

The charge pump boosts the voltage at the gate of the NMOS cascode to an optimal voltage level above the supply, to produce low dropout. The circuit has been optimized, using parasitic capacitors C_{par} and diodes D_{par} across the output switches and a very low current sink I_{sink} at the output, to produce a voltage lower than $2V_{DD}$ so that M_{CAS} is operating in saturation. The topology implemented is described in [5].

MCAS simply acts as a voltage follower for signals at its gate. Hence, it is absolutely critical to shield its gate from noise in the power supply, as this would be transferred without attenuation to the linear regulator at its source. This function is performed by the RC filter. The RC filter, comprising of R_F and C_F , filters out high frequency fluctuations in the power supply to attenuate power supply noise reaching the gate of the NMOS cascode and hence to the regulator through path 'a'. In other words, the RC filter adds a pole to the path 'a', affecting the PSRR curve in a manner similar to that of an RC filter in series with the supply. However, since this RC filter is placed in a path that does not carry any dc current, the resistor can be made as large as practically possible, to yield a pole extremely close to dominant zero (BWA) of the PSRR curve '1' in Fig. 2. Hence, the effective PSRR of the system follows that of a conventional regulator at low frequencies and that of a cascoded regulator at high frequencies. In this topology, the corner frequency of the RC filter is 20KHz, which has been obtained using a 700K Ω resistor and 15pF capacitor. The RC filter also suppresses the systematic ripple generated by the charge pump. Since the charge pump is connected to the gate of the NMOS cascode through this RC filter and is not supplying current to an active load, it does not exhibit any droop in output voltage and has not been regulated, leading to lower circuit complexity.

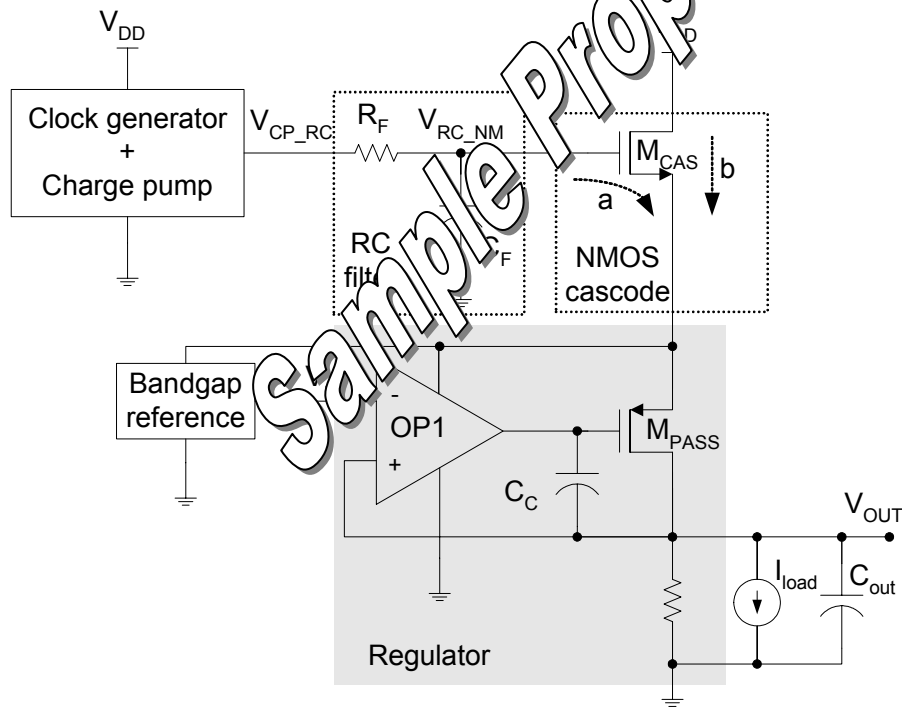


Fig. 1. Strategy to achieve high PSRR over wideband frequencies.

C. Simulation Results

This system was simulated using BSIM3 models of AMI 0.5 μ m CMOS process, obtained from MOSIS. The system was designed to source an output current of 2.5mA while maintaining an output voltage at 1.0V. Fig. 2(a) and Fig. 2(b) present the output voltage as a function of temperature and load current for various supply voltages. Fig. 2(c) and Fig. 2(d) show that a 10MHz, 200mVpp ripple at the power supply produces a 1mVpp ripple at V_{OUT} . This simulation shows that the worst-case PSRR of the system is -40dB.

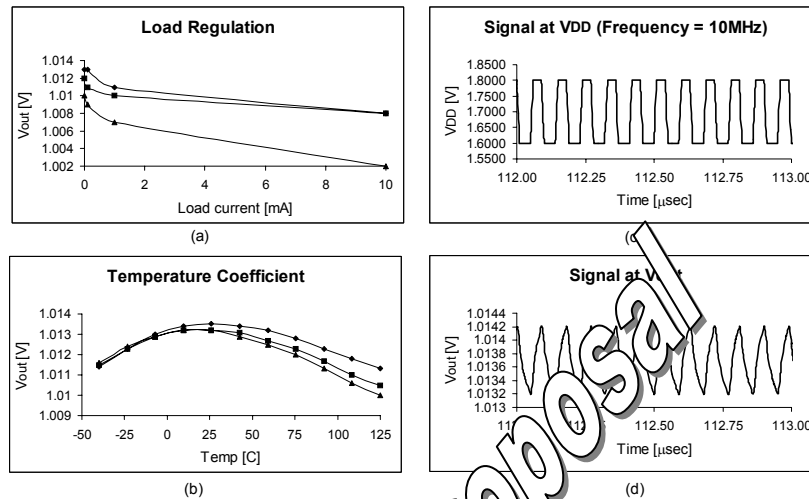


Fig. 2. (a) Temperature coefficient, (b) load regulation, (c) ripple at power supply, and (d) ripple at output of regulator showing PSRR of -40dB.

II. TEST PLAN

A. Testing Functionality

Even though every block of the system (i.e., the charge pump, RC filter, cascode, reference, and regulator, is fabricated on the same die, isolation between blocks shall be achieved by connecting them only via external pins. This shall allow the each block to be tested for functionality before the entire system is tested for performance. The following functionality shall be tested for each block:

(a) Regulator:

- Load Regulation (variation of output with load current)
- Line Regulation (variation of output with line voltage)

(b) Reference:

- Line Regulation
- Temperature coefficient (variation of output with temperature)

(c) Charge Pump:

- Line Regulation
- Load Regulation

B. Testing PSRR Performance

The PSRR performance of the regulator shall be tested without the cascode so that the performance

improvement with the cascode can be measured. After that, the entire scheme shall be connected using external pins and the PSRR performance shall be measured over the following ranges:

- Frequency: 10 – 100MHz
- Load current: 0 – 2.5mA
- Line voltage: 2.0 – 2.5V

PSRR performance shall be measured by introducing a known ripple in the supply using a pulse generator and measuring the magnitude of the ripple produced at the output of the regulator.

NOTE: In order to reduce the effect of the parasitic inductance of the bondwire, the V_{DD} and V_{SS} nodes are connected to 10 pins each so that the parasitic inductance is reduce by a factor of 10.

III. PACKAGING REQUIREMENTS, ESTIMATED SIZE, AND REQUIRED PROCESS

The design submitted requires a conventional 40 pin DIP ceramic package. The design shall require an area of 1.5mm x 1.5mm. The chip has been designed to be fabricated in the AMI 0.5 μm process.

REFERENCES

- [1] K. R. Volk (2002, July 09), "Dealing with noise when powering RF sections in cellular systems" [Online] Available: http://www.commsdesign.com/design_corner/showArticle.jhtml?articleID=16505374
- [2] Dallas Semiconductor/Maxim, Appl. Note 898, "Selecting LDO linear regulators for low noise designs." [Online] Available: http://www.maxim-ic.com/appnotes.cfm/appnote_number/898
- [3] C. Lee, K. McClellan, and J. Choma Jr., "A supply-noise-insensitive CMOS floating-gate voltage regulator using dc-dc capacitive converter," *IEEE Jour. of Solid-State Circuits*, vol. 36, pp. 1453-1463, Oct. 2001
- [4] V. Gupta, G. A. Rincón-Mora, "A low dropout, CMOS regulator with gain over wideband frequencies," *Proc. IEEE Intl. Symp. Circuits and Sys.*, Kobe, Japan, 2005.
- [5] P. Favrat, P. Deval, and M. J. Declercq, "A high-efficiency CMOS voltage doubler," *IEEE Jour. Solid-State Circuits*, vol. 33, pp. 410-416, March 1998.

Sample Proposal

An Accurate, Low-Voltage CMOS Bandgap Reference Circuit

Vishal Gupta, Gabriel A. Rincón-Mora
Email: vishalg@ece.gatech.edu, rincon-mora@ece.gatech.edu

Georgia Tech Analog and Power IC Design Lab
School of Electrical and Computer Engineering
Georgia Institute of Technology

I. AIM

The general goal of these measurements was to characterize a CMOS bandgap reference circuit. The following lists the particular tests that were carried out.

1. Startup of circuit
2. Temperature coefficient of V_{REF}
3. Line regulation of circuit
4. Load regulation of circuit

II. APPARATUS

The following lists the apparatus used for each of the tests.

1. Startup of circuit
 - a. Oscilloscope (TDS3054)
 - b. Voltage source (HP6237B)
 - c. Signal generator (HP33120)
2. Temperature coefficient of V_{REF}
 - a. Voltage source (HP6237B)
 - b. Multimeter (Keithley 2000)
 - c. Temperature chamber (Delta Design)
3. Line regulation
 - a. Voltage source (HP6237B)
 - b. Parameter Analyzer (HP4145)
 - c. Multimeter (Keithley 2000)
4. Load regulation
 - a. Voltage source (HP6237B)
 - b. Parameter Analyzer (HP4145)

III. PROCEDURE

Each of the tests required a different procedure and had unique precautions to be observed. The tests were carried out on 20 samples. The supply voltage at the V_{DD} pin was set to 1.5V and the load current was zero (unless otherwise stated).

1. Startup of circuit
 - a. A startup ramp was applied to the ENABLE pin and V_{REF} was monitored.
 - b. The oscilloscope was configured to measure the difference between the rise of the enable signal and the rise of the reference voltage to measure the startup time.
 - c. The startup time was noted.

- d. The procedure was repeated for different samples.
2. Temperature coefficient of V_{REF}
 - a. The magic voltage of the circuit was determined. This step involved the following procedure:
 - i. All the trim bits were opened.
 - ii. The DUT was placed in the temperature chamber and the reference voltage was measured as a function of temperature for a range of -40°C to 125°C (V_{REF} at room temperature 25°C was noted in particular).
 - iii. All the trim bits were opened.
 - iv. The reference voltage was measured as a function of temperature for a range of -40°C to 125°C .
 - v. MS Excel was used to fit regression lines to compute the slopes (β) of the least-square-fit lines passing through both the curves.
 - vi. The procedure was repeated for different samples.
 - vii. A plot of reference voltage vs. temperature vs. β was obtained.
 - viii. The y-intercept of least-square fit line ($\beta = 0$) for the obtained data points was calculated – this was the magic voltage to which all samples were to be trimmed.
 - b. A sample was placed in the temperature chamber and trimmed to the magic voltage at room temperature.
 - c. The trim code required was noted.
 - d. The value of the reference voltage before and after trimming was noted.
 - e. The output was measured as a function of temperature for a range of -40°C to 125°C .
 3. Line regulation
 - a. The sample was trimmed to the magic voltage using its unique trim code (noted earlier).
 - b. To measure the minimum supply voltage required by the circuit, the voltage at pin V_{DD} was ramped from 0 to 2.5V using the parameter analyzer.
 - c. The output voltage was measured at each point.
 - d. Since the HP4145 had limited resolution (1mV), line regulation was determined by measuring V_{REF} when V_{DD} was held at 1.5V and 2.5V using the voltage source.
 - e. The procedure was repeated for different samples.
 4. Load regulation
 - a. The sample was trimmed to the magic voltage using its unique trim code (noted earlier).
 - b. The HP4145 was used to ramp the load current from 0 to 5mA in steps of 0.5mA.
 - c. The output of the circuit was measured at each load current.
 - d. The procedure was repeated for different samples.

IV. OBSERVATIONS

1. Startup of circuit

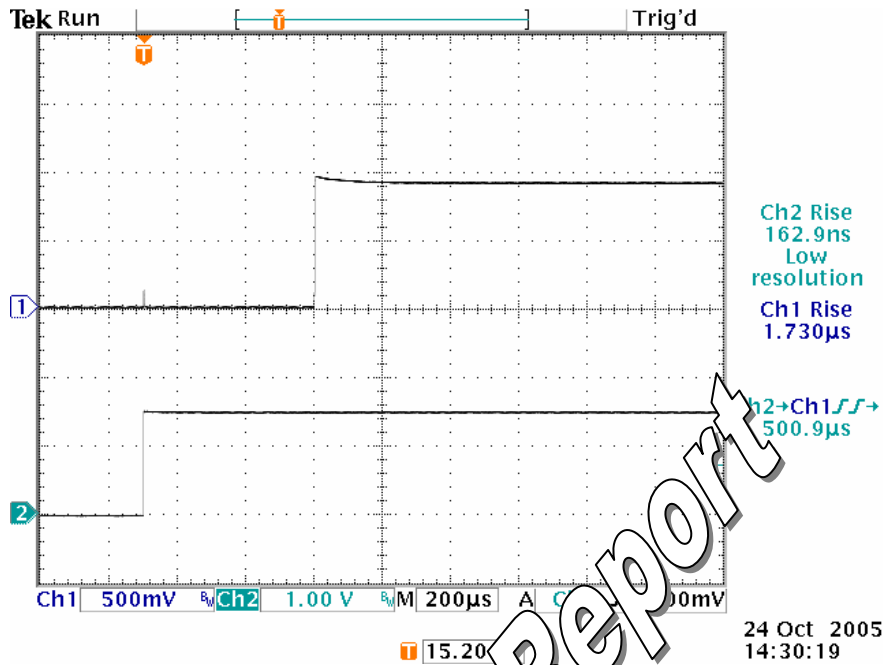


Fig. 3. Startup of circuit – measured data for 1 sample.

2. Temperature coefficient of V_{REF}

Table 2. V_{REF} vs. temperature - measured data for 5 samples.

Temperature [°C]	V_{REF} [mV]				
	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5
-40	889.0	888.9	891.8	892.4	889.5
-25	889.0	889.0	891.6	892.2	889.9
0	889.3	889.3	891.3	891.9	890.4
25	889.6	889.7	890.9	891.4	890.9
50	889.8	890.0	890.5	890.8	891.2
75	890.0	890.3	890.1	890.3	891.5
100	890.1	890.6	889.9	889.9	891.9
125	890.2	890.9	889.7	889.5	892.1
V_{REF} (untrimmed)	908.4	906.1	912.2	915.2	907.5
trim code	01000	01001	00111	00110	01001
TC (ppm/°C)	8.99	14.61	14.37	20.21	16.46

3. Line regulation

Table 3. Line regulation - measured data for 5 samples.

V_{DD} [V]	V_{REF} [mV]				
	Sample1	Sample2	Sample3	Sample4	Sample5
0.65	4	5	5	5	5
0.7	16	22	20	20	17
0.75	62	83	77	76	65
0.8	215	275	265	260	226
0.85	587	873	674	664	604
0.9	865	940	874	873	868
0.95	938	994	939	939	938
1	1046	1046	1046	994	994
1.05	1096	1097	1096	1046	1046
1.1	937	1147	1146	1096	1096
1.15	904	1046	939	1146	1146
1.2	893	944	907	1027	1145
1.25	890	908	896	935	939
1.3	889	896	893	935	906
1.35	889	893	892	935	895
1.4	889	892	892	935	892
1.45	889	892	892	889	891
1.5	889	892	892	889	891
1.55	889	892	892	888	891
1.6	889	892	892	888	891
1.65	889	892	892	888	891
1.7	889	892	892	888	891
1.75	889	892	892	888	891
1.8	889	892	892	888	891

4. Load regulation

Table 4. Load regulation - measured data for 5 samples.

I_{LOAD} [mA]	V_{REF} [mV]				
	Sample1	Sample2	Sample3	Sample4	Sample5
0	889	890	890	888	890
0.5	888	888	889	887	888
1	887	887	888	886	887
1.5	886	887	887	885	887
2	885	886	886	885	886
2.5	885	885	886	884	885
3	884	885	885	883	885
3.5	883	884	884	882	884

4	882	883	884	881	883
4.5	882	883	883	880	882
5	881	882	882	880	882

V. DISCUSSION

For the current implementation, the the minimum operating supply voltage was limited by the high threshold voltage of the PMOS device, V_{TP} , which has a nominal value of -0.92V. Using a technology with a lower V_{TP} would reduce the minimum supply voltage from the current value of 1.4V to a value lower than 1.2V, the output voltage of a conventional bandgap reference.

The deviation of the measured ‘magic voltage’ of 890mV from its ideal value of 900mV is due to the lack of accurate models for substrate diode D. This deviation can be reduced by characterizing different geometries of substrate diodes across the operating temperature range to extract their model parameters along with associated temperature coefficients.

The circuit was trimmed using 4 trim bits which provided a resolution of 3mV and a trim range of 45mV. The temperature coefficient by the box method, as mentioned earlier, was found to be 34.7ppm/°C. The box method calculates the temperature coefficient of the reference by using the difference of the maximum and minimum reference voltage across all the measured samples over the entire temperature range.

The droop in the reference voltage with increasing load current is due to the degradation of the loop gain as the current through the pass device increases. This droop can be reduced by increasing the loop gain of the circuit using a higher number of gain stages. Obviously, the stability of the circuit needs to be maintained by compensating the additional poles introduced by each gain stage.

Sample Report