ECE 3040 Microelectronic Circuits

Exam 3

April 21, 2017

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Print your name clearly and largely: Solutions

Instructions:
DO NOT TAKE APART ANY PAGES OF THIS EXAM AND SHOW ALL WORK ON THE PROVIDED PAGES. Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your two note sheets from the previous exams as well as a calculator. There are 100 total points in this exam. Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

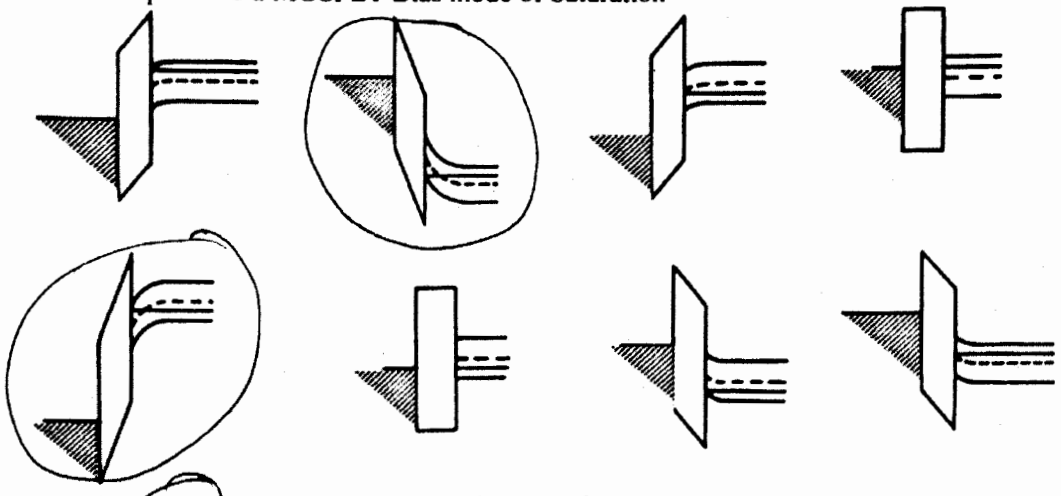
Sign your name on **ONE** of the two following cases:

I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:

First 24% **Multiple Choice and True/False (Select the most correct answer)**

1.) (6-points total) For the MOS Capacitors shown below, Circle the correct capacitor bias mode that corresponds to a MOSFET Bias mode of Saturation



2.) (3-points) True / False: Feedback can increase the closed loop bandwidth of an opamp.

3.) (3-points) True / False: When a MOSFET channel is "pinched-off", regardless of the length of the drain voltage V_{DS}, the end of the channel is at V_{DSAT}.

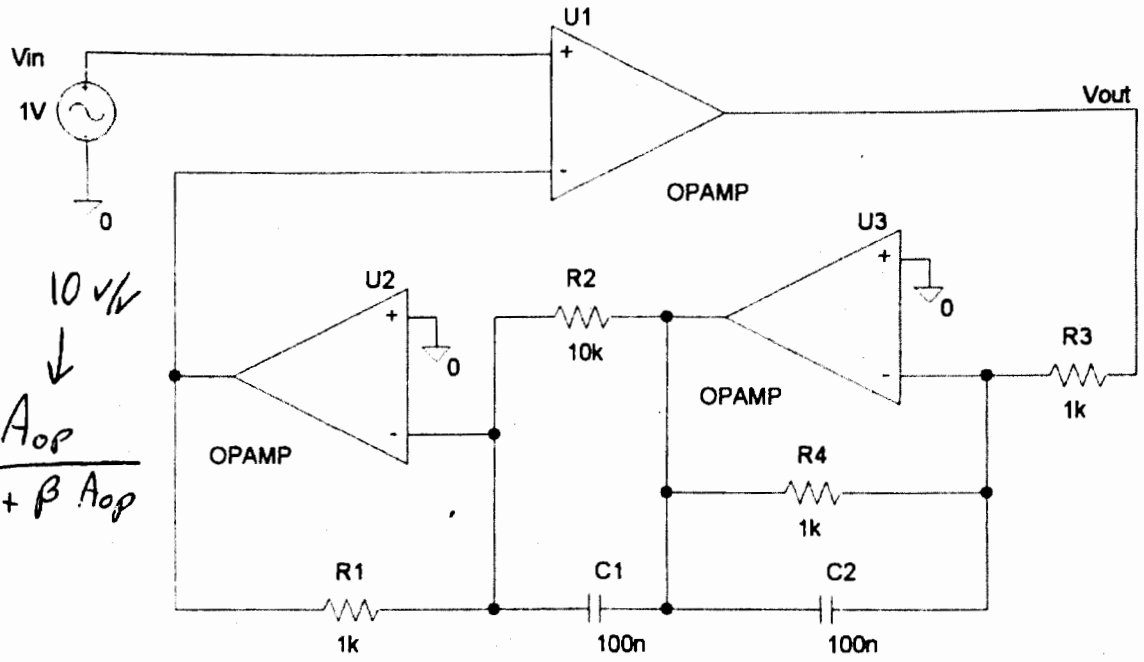
4.) (3-points) True / False: A PMOS transistor has a p-type drain.

5.) (3-points) True / False: A well designed current amplifier should have a very high input resistance.

6.) (3-points) True/False: A Common Drain amplifier has a negative gain whose magnitude can be greater than 1.

7.) (3-points) True/False: Minority carriers dominate MOSFET current flow in saturation.

8.) (26-points) The opamps used in the circuit below can be considered ideal except U1 (and only U1) has an open loop gain of only 10 volts/volt. Determine the closed loop gain and sketch and label the Bode plot showing the voltage gain in all flat regions and the break frequencies (gain in dB vs Log of Frequency).



10 V/V

$$A_{CL} = \frac{A_{op}}{1 + \beta A_{op}}$$

$$\beta(s) = -\left(\frac{\frac{1}{C_2 s} \| R_4}{R_3}\right) \times -\left(\frac{R_1}{\frac{1}{C_1 s} \| R_2}\right)$$

$$= \left(\frac{R_4}{(1 + R_4 C_2 s) R_3}\right)\left(\frac{(1 + R_2 C_1 s) R_1}{R_2}\right)$$

$$= \left(\frac{R_4}{R_3}\right)^{1}\left(\frac{R_1}{R_2}\right)^{0.1}\left(\frac{1 + R_2 C_1 s}{1 + R_4 C_2 s}\right)$$

$$A_{CL} = \frac{10}{1 + 10(0.1)\left(\frac{1 + R_2 C_1 s}{1 + R_4 C_2 s}\right)}$$

$$= \frac{10(1 + R_4 C_2 s)}{(1 + R_4 C_2 s) + (1 + R_2 C_1 s)} = \frac{10(1 + R_4 C_2 s)}{2 + (R_4 C_2 + R_2 C_1)s}$$

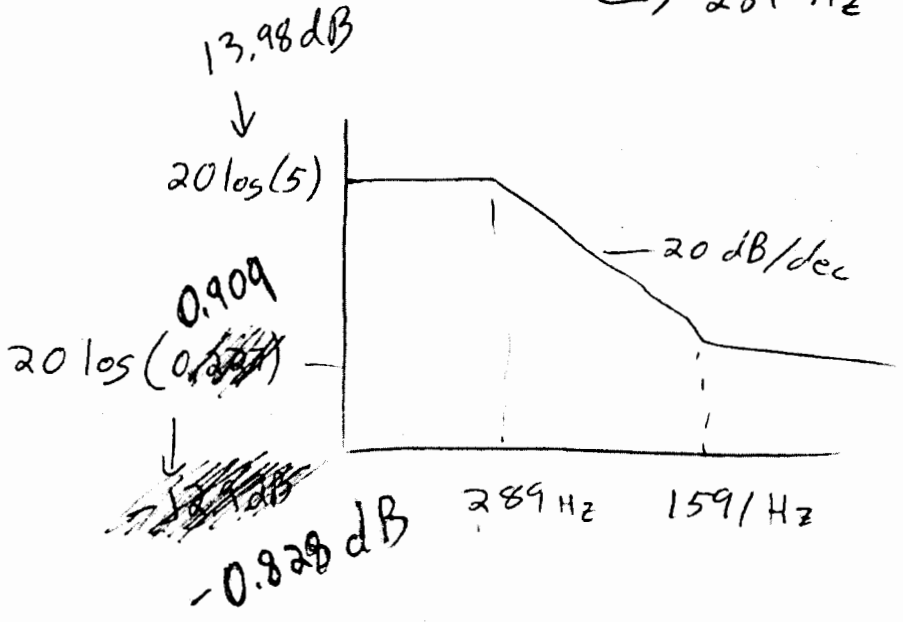
$$= \frac{5(1 + R_4 C_2 s)}{1 + \left(\frac{R_4 C_2 + R_2 C_1}{2}\right)s}$$

Extra work can be done here, but clearly indicate with problem you are solving.

$$A_{CL} = \frac{5\left(1 + 1e\text{-}4s\right)}{\left[1 + \left(\frac{1.1e\text{-}3}{2}\right)s\right]}$$

→ 1591 Hz

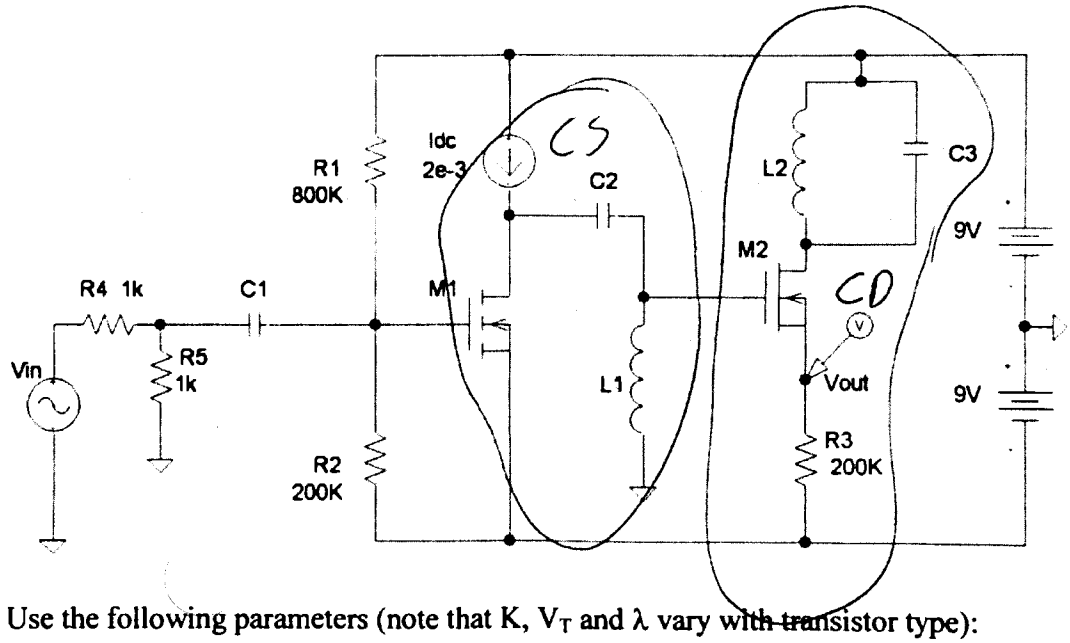
→ 289 Hz



Pulling all the concepts together for a useful purpose:

10) (50-points) Given the following amplifier circuit, (a) Identify the configuration of the stage (common ____). (b) What is the AC voltage gain, v_{out}/v_{in}? You may assume all capacitors have infinite capacitance and all inductors have infinite inductance. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances.

Grading will be based as such: part a=5 points, part b=18 points for DC solution (gate, source and drain voltages along with drain currents), 12 points for the conversion to the small signal model and 15 points for small signal analysis. ***SHOW ALL WORK TO GET CREDIT!!!!! Do not just quote a result!!!!!***



Use the following parameters (note that K, V_T and λ vary with transistor type):

M2: For NMOS Depletion Transistors:
K_n'=15 uA/V^2 **V_T= -4.0V** **λ=0.0 V^{-1}** Length (L)=10 um Width (W)=10 um

M1: For NMOS Enhancement Transistors:
K_n'=250 uA/V^2 **V_T= +1.0V** **λ=0.1 V^{-1}** Length (L)=10 um Width (W)=10 um

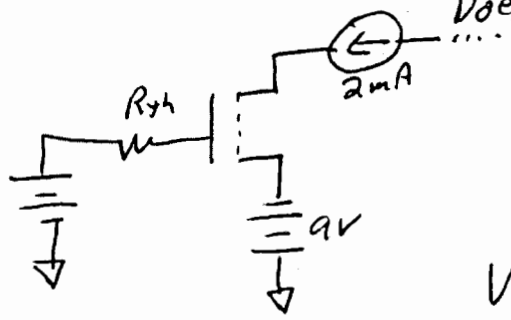
For PMOS Depletion Transistors:
K_p'=40 uA/V^2 **V_T= +3.0V** **λ=0.0 V^{-1}** Length (L)=10 um Width (W)=10 um

For PMOS Enhancement Transistors:
K_p'=50 uA/V^2 **V_T= -1.75V** **λ=0.1 V^{-1}** Length (L)=10 um Width (W)=10 um

Extra work can be done here, but clearly indicate with problem you are solving.

DC Solution

M1:



$$V_{th} = 9\left(\frac{200}{200+800}\right) - 9\left(\frac{800}{800+200}\right)$$
$$= -5.4V$$

$$V_{GS} = V_G - V_S = -5.4 - (-9) = 3.6V \quad (> V_{th} = 1)$$

$$I_{DS} = 2mA = \left(\frac{10}{10}\right)\left(\frac{250e\text{-}6}{2}\right)(3.6-1)^2(1+0.1V_{DS})$$

($\frac{10}{10}$: (W/L); $\frac{250e\text{-}6}{2}$: K_n'; $3.6-1$: V_{GS}; 0.1: λ)

$$V_{DS} = 13.668V \Longrightarrow V_D = V_{DS} + 9V = 4.668V$$

Check Saturation: $V_{DS} \overset{?}{>} V_{GS} - V_T$

$13.67 > 3.6 - 1$ ✓

M2: $V_G = 0 \quad V_D = 0 \quad V_S = -9 + I_{DS}R_3$

$$I_{DS} = \left(\frac{10}{10}\right)\left(\frac{15e\text{-}6}{2}\right)(V_{GS}-V_T)^2(1+0V_{DS})$$

($\frac{10}{10}$: (W/L); $\frac{15e\text{-}6}{2}$: K_p; 0: λ)

$V_{GS} = V_G - V_S$
$= 9 - I_{DS}R_3$
or $I_{DS} = \frac{9-V_{GS}}{R_3}$

$$\left(\frac{9-V_{GS}}{R_3}\right) = (7.5e\text{-}6)(V_{GS}^2 - 2V_{GS}V_T + V_T^2)$$

$$0 = 7.5e\text{-}6\,V_{GS}^2 + \left(8(7.5e\text{-}6) + \frac{1}{200k}\right)V_{GS} + \left[16(7.5e\text{-}6) - \frac{9}{200k}\right.$$

$V_{GS} = -1.37V$ or ~~$-7.30V$~~ → Cutoff

$I_{DS} = 51.85\mu A$

$V_S = 1.37V$

$V_{DS} = 9 - 1.37V = 7.63V > V_{GS} - V_T$ ($-1.37 - (-4) = 2.63$)

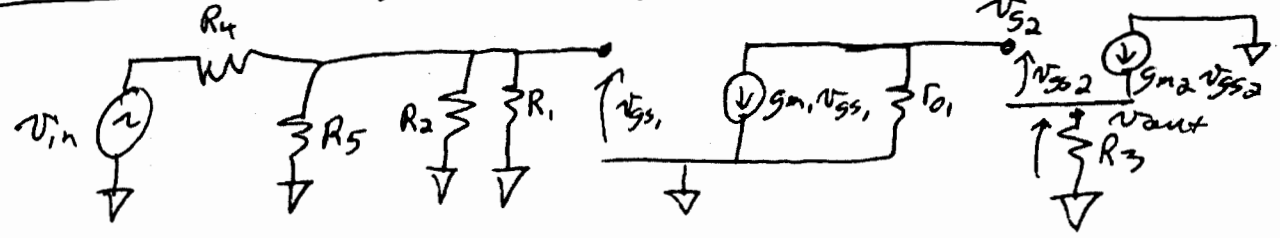
Saturated

Extra work can be done here, but clearly indicate with problem you are solving.

Conv:

$g_{m1} = 2I_{DS}/(V_{GS1} - V_{T1}) = 1.53e-3$ $\quad r_{o1} = \frac{1/\lambda + V_{DS}}{I_{DS}} = 11,835\ \Omega$

$g_{m2} = 3.94e-5\ \mho$ $\quad r_{o2} = \infty$



1) $\frac{v_{gs1}}{v_{in}} = \left(\frac{R_5 \| R_2 \| R_1}{R_4 + R_5 \| R_2 \| R_1}\right) = 0.5$

2) $\frac{v_{gs2}}{v_{gs1}} = -(g_{m1} r_{o1}) = -18.1$

3) $v_{s2} = v_{gs2} + R_3 g_{m2} v_{gs2} = v_{gs2}\underbrace{(1 + g_{m2}R_3)}_{8.88}$

4) $v_{out} = \underbrace{g_{m2} R_3}_{7.88} v_{gs2}$

$$\frac{v_{out}}{v_{in}} = \underset{①}{\left(\frac{v_{gs1}}{v_{in}}\right)}\underset{②}{\left(\frac{v_{s2}}{v_{gs1}}\right)}\underset{③}{\left(\frac{v_{gs2}}{v_{s2}}\right)}\underset{④}{\left(\frac{v_{out}}{v_{gs2}}\right)}$$

$$= \underset{①}{(0.5)}\underset{②}{(-18.1)}\underset{③}{\left(\frac{1}{8.88}\right)}\underset{④}{(7.88)}$$

$$\boxed{A_V = -8.03\ V/V}$$