The transistors in this homework are to be implemented in 0.18 µm MOS technology so all dimensions must be a multiple of these numbers (we will approximate 5.04 as 5).

1. For the basic transistor circuit in Fig. 1, solve for the Q-point (all three currents and voltages on the transistor) assuming a V_{TNO} =+0.5V, $K_n'=\mu_n C_{ox}$=100 µA/V^2, W=5µm, L=0.18µm, a channel length modulation parameter, λ=0.0 V^{-1}, a body effect parameter, γ=0.0 V$^{1/2}$ and φ_F=0.4V.
    a. Assuming the transistor is biased in cutoff (neglect leakage currents).
    b. Assuming the transistor is biased in triode/linear.
    c. Assuming the transistor is biased in saturation.
    d. Which assumption is valid?

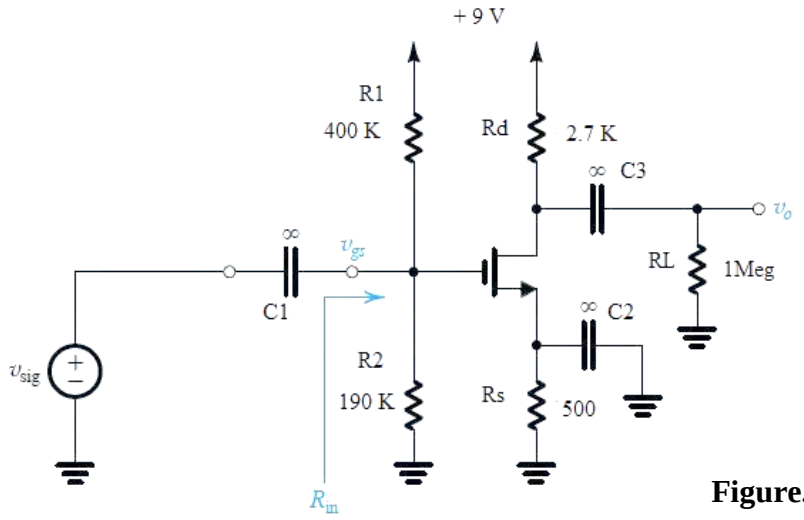

Figure. 1

    e. Repeat part c for λ=0.1 V^{-1} .
    f. For λ=0.1 V^{-1}, (part e answers) determine the voltage gain v_o/v_{sig}
    g. What is the maximum allowable v_o signal swing without distortion.

2. For the circuits shown in Fig. 2, find the labeled node voltages. The NMOS transistors have V_t = 1 V and W/L = 5 mA/V^2.

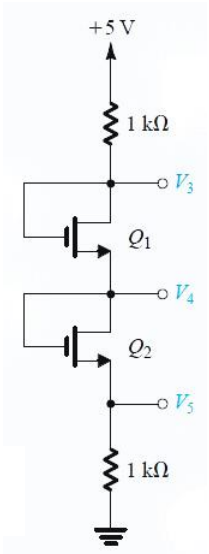

Figure. 2

3. For the circuit below,
   a) Calculate the voltage gain. This configuration uses a current source as a load instead of the resistor, Rd.
   b) Why is the body of the PMOS transistor tied to the source/highest potential?
   c) If the PMOS transistor could be made with arbitrary dimensions such that W/L=2.81, what would be the new gain?
   d) Given the dimensions must be a multiple of 0.18 μm, how could we best approximate this value so as to get the benefits of the higher gain you should have found in part c but stay within the limits of the 0.18 μm technology?
   In an integrated circuit, this transistor load (or "active" load as opposed to the "passive" resistor load) results in huge space savings making complex analog circuits very compact and thus cheaper and higher performance.

   For M1, V_{TNO} =+0.5V, $K_n'=\mu_n C_{ox}$=100 μA/V^2 , W=5μm, L=0.18μm, a channel length modulation parameter, λ=0.0 V^{-1}, a body effect parameter, γ=0.0 $V^{1/2}$ and φ_F=0.4V.

   For M2, V_{TPO} =+4V, $K_p'=\mu_n C_{ox}$=100 μA/V^2 , W=0.54 μm, L=0.18 μm, a channel length modulation parameter, λ=0.0 V^{-1}, a body effect parameter, γ=0.0 $V^{1/2}$ and φ_F=0.4V.

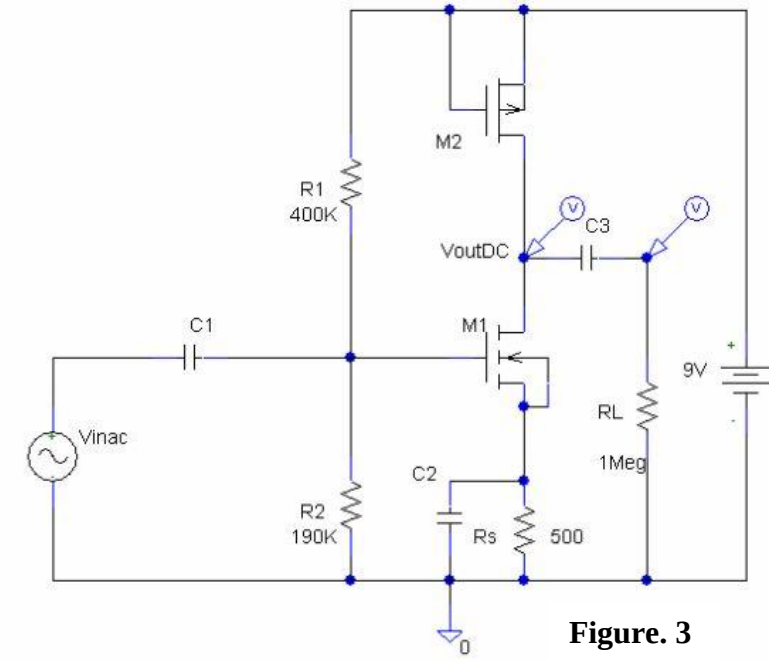

Figure. 3

4. Figure 4 shows a discrete-circuit amplifier. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage signal that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite).

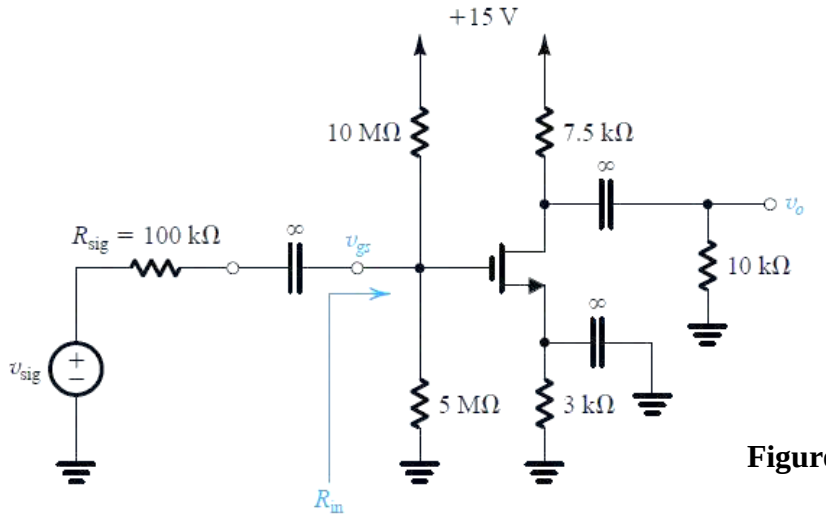

Figure. 4

a. If the transistor has V_t = 1 V, and = 2 mA/V^2, verify that the bias circuit establishes V_{GS} = 2 V, I_D = 1 mA, and V_D = +7.5 V. That is, assume these values, and verify that they are consistent with the values of the circuit components and the device parameters.
b. Find g_m and r_o if V_A = 100 V.
c. Draw a complete small-signal equivalent circuit for the amplifier, assuming all capacitors behave as short circuits at signal frequencies.
d. Find R_{in}, v_{gs}/v_{sig}, v_o/v_{gs}, and v_o/v_{sig}.