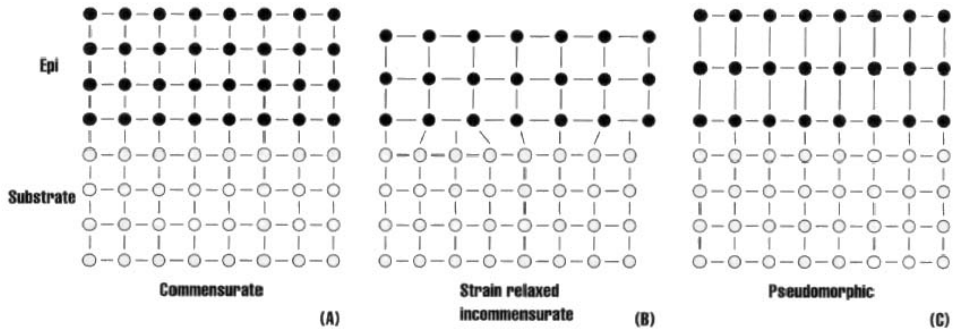


Figure 14-15 Epitaxial growth processes can be divided into (a) commensurate, (b) strain relaxed incommensurate, and (c) incommensurate but pseudomorphic.

Besides these problems, good example problems (not to be turned in) include 12.2 and 14.3 .

1.) A simple cubic epitaxial material is grown by MBE pseudomorphically strained to a simple cubic substrate as shown in cross section in figure 14-15C. During this process, extra energy is required to force the atoms to arrange in the above configuration. The epitaxial material has a lattice constant that is 1% larger than the substrate. The bond energy per atomic bond is 2.2 eV/bond, about the value found for GaN semiconductors. Assuming that the epitaxial layer has a natural unstrained lattice constant of 2.5 angstroms and the increase in bond energy is linearly dependent on its deviation from its natural bond energy (ie the strained material has a bond energy of 1.01 x 2.2 eV/bond), what is the total amount of stored *excess* energy in a 0.5 um thick layer on a 4" diameter wafer? For simplicity, you may assume the material distorts the same vertically as it does laterally (normally, this is not accurate as the Poisson ratio would describe the asymmetry in the distortion).

A 4" wafer (8.1e17 angstroms^2 area) by 5000 angstrom thick layer constitutes a volume of 4.05e21 angstroms^3. Thus, there are 4.05e21/(1.01 x 2.5 x0.99 x 2.5 x 0.99x2.5) or 2.62e20 unit cells. Each cubic unit cell contains 2 atoms (or only one bond) because the atoms (or bonds) on cell vertices (or edges) are shared with other unit cells. Thus, the extra stored energy in the film is:
2.62e20 bonds x (0.01*2.2 eV/bond)=5.76e18 eV or 0.92 Joules.

This is a lot of energy for atomic bonds to handle! Enough to completely break 2.62e18 bonds (not surprisingly, 1% of the total number of bonds in the material). Thus, in reality, the bonds tend to break well before this much energy is stored up, resulting in MANY dislocations and a strain relaxed incommensurate lattice as shown in figure 14-15B.

2.) Discuss the differences that pressure makes in a CVD or MOCVD system versus a MBE system. Include discussions of step coverage, purity, and growth rates. Would the same comparisons be applicable to sputtering versus evaporation?

Higher pressures in MOCVD compared to MBE result in better step coverage (less directional species flow resulting in material getting into rounded or "hidden" crevices), lower purity (if a gas-species/ambient environment has a given purity, say 99.9999%, then the higher pressures ensure more overall impurities in the ambient). No effect on growth rates results.

3.) A thick low doped region is needed for a power device (often used to withstand very large voltages). Is this best achieved by diffusion, ion implantation or epitaxy? Why?

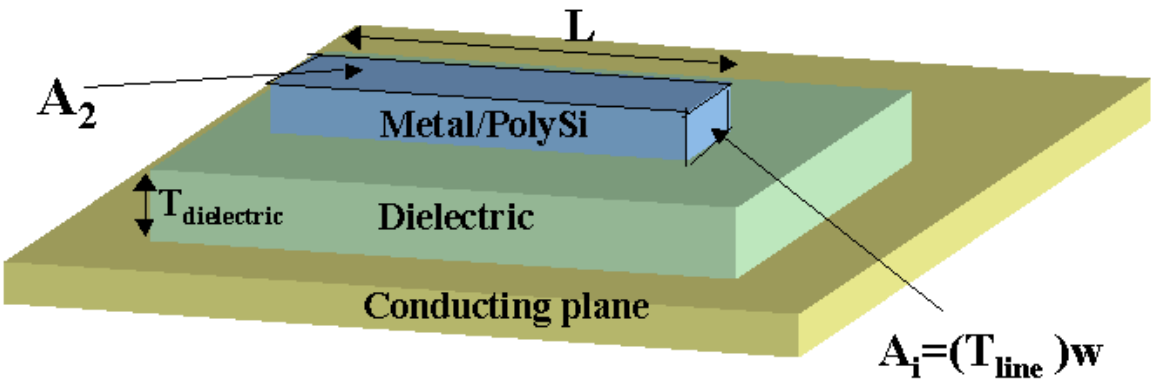
Epitaxy. Both diffusion and ion implantation have regions that are highly doped. Epitaxy can make a low doped region uniformly throughout the material.

4.) A pure metallic aluminum layer is needed for a Schottky diode contact to Si. These contacts require a clean, undamaged region just under the metal. Is a thermal evaporator or a sputterer a better system to apply this metal? Why?

Evaporator. Sputterers result in some plasma damage.

5.) A 1 cm long (global interconnect), 5000 angstrom thick, 1000 angstrom wide interconnect line is placed over a conducting plane separated by a 1 um thick dielectric SiO_2 layer (ε_R=K=3.9) as shown below. This forms a standard parallel plate capacitor (ignore fringing fields). Fill in the following table for the RC delay expected for the materials listed in the table (see figure and/or equations 15.18-15-20). This RC delay represents the time delay required for the electrical signal to charge the capacitor through the wire resistance. If the RC charging were viewed as a simple RC filter, what would be the frequency at which ½ the power is lost (an estimate of the maximum frequency operation of such an interconnect line). Why is copper used for high speed CMOS? What other means could be used to increase these operational frequencies?

The delays and frequencies are given below. Notice the slow charging of poly-Si lines. This is why they are only used for very short interconnects (local interconnects). Note the ~50% improvement when using copper, justifying its use in high speed circuitry. Another means of increasing speed is to use a dielectric with a lower relative dielectric constant (K). Currently materials with K's as low as 2.5 are being used. Air, k~1 is used in multi-10's of GHz III-V transistor circuits. Another approach is in the architecture, limiting the need to send signals over such great distances.



$$R = \frac{\rho L}{A_i} \qquad C = \frac{\varepsilon_{dielectric} A_2}{T_{dielectric}} = \frac{\varepsilon_o \varepsilon_R L w}{T_{dielectric}}$$

$$RC = \frac{\rho \varepsilon_o \varepsilon_R L^2}{T_{line} T_{dielectric}}$$

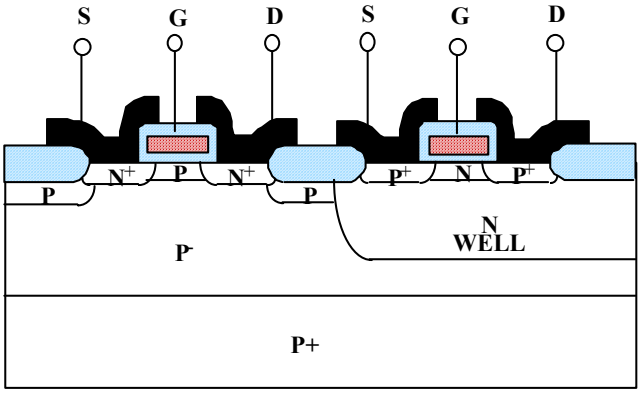
L=	1	cm	
T_{line}=	5.00E-05	cm	
$T_{dielectric}$=	1.00E-04	cm	
ε_o=	8.85E-14	cm^2/F	
ε_R=K=	3.9		
Material	ρ ($\mu\Omega$-cm)	RC (nsec)	Frequency @ 50% power loss (GHz)
poly-Si	1000	69.061	0.002
Al	2.65	0.183	0.870
Cu	1.678	0.116	1.373
Ag	1.586	0.110	1.453

3.) Sketch a process flow for the CMOS structure below by drawing a series of drawings showing each step in the fabrication process. For each step provide details of the process used (tool, temperature, chemistry, etc...).

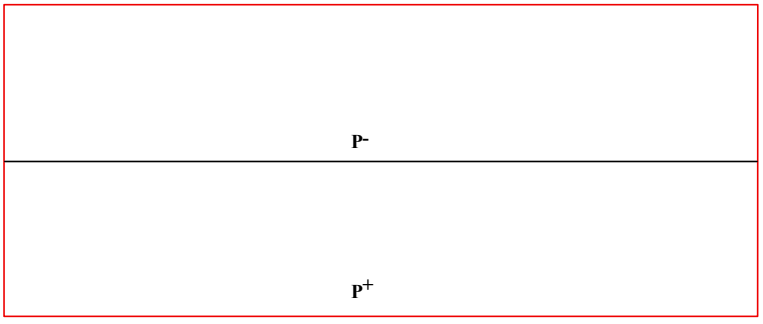
Figure Key:
Blue hashed region is an oxide.
Red cross-hashed region is the polysilicon gate contact.
Black layers are the metal contacts.

**********************This answer is *WAY* more detailed than I would expect from you. It is meant as a learning tool.***************************

The CMOS technology we need to realize is shown below.

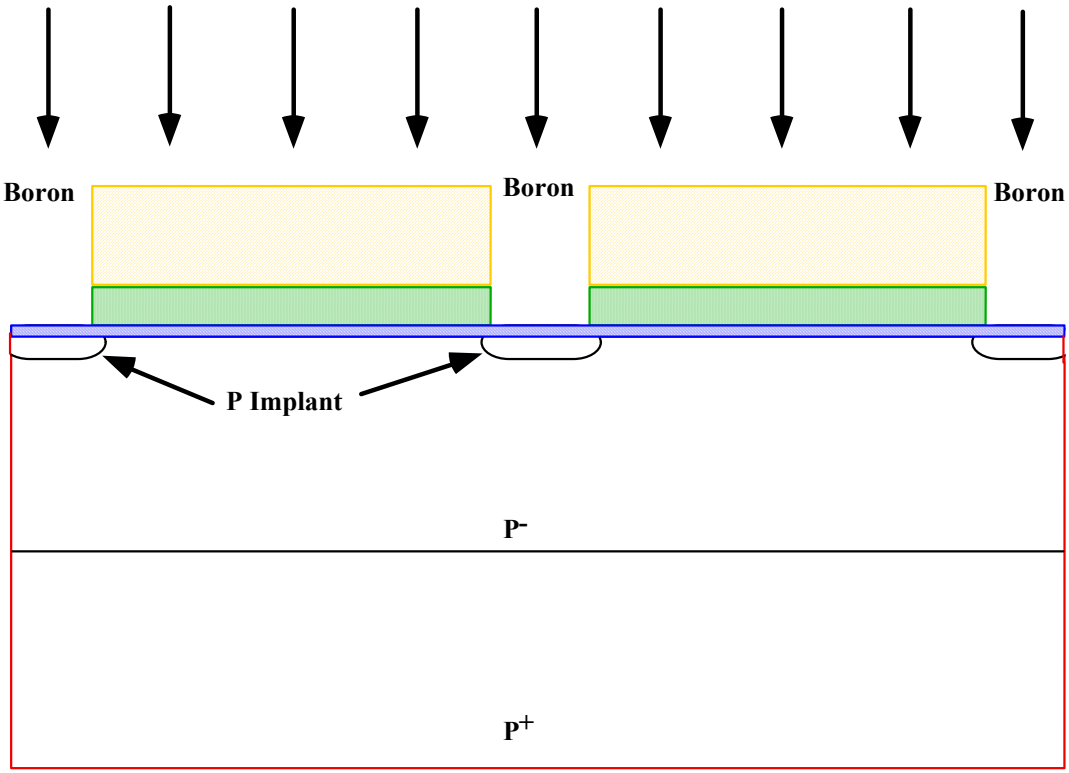


We can follow many of the process steps used in the CMOS process flow in Chapter 16. An epi layer is needed, only one well (P well) is used, and the device structures are considerably simplified from those in the text because there are no Lateral Double Diffused regions etc.



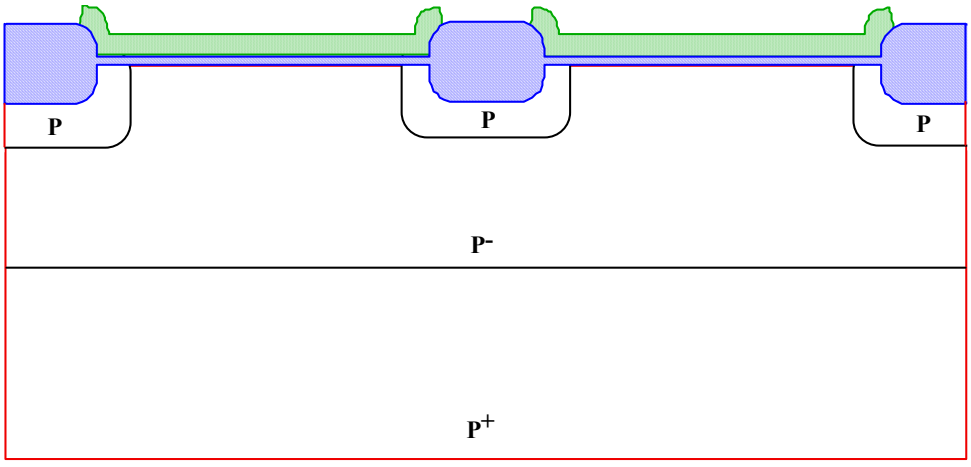
The first step is to grow the blanket epi layer shown in the final cross-section. A heavily doped P^+ substrate is chosen (even though we will not use a denuded zone due to the epi layer being grown with high purity we still use a CZ wafer to prevent wafer warpage during processing) and a lightly doped boron epitaxial layer is grown uniformly on its surface. Chemical Vapor Deposition (CVD) is used. One suggested chemistry would be to use Dichlorosilane (SiH_2Cl_2) (most common) and

allows growth at ~800 to 1050 °C (higher T is possible). Doping is done with diborane, B_2H_6.

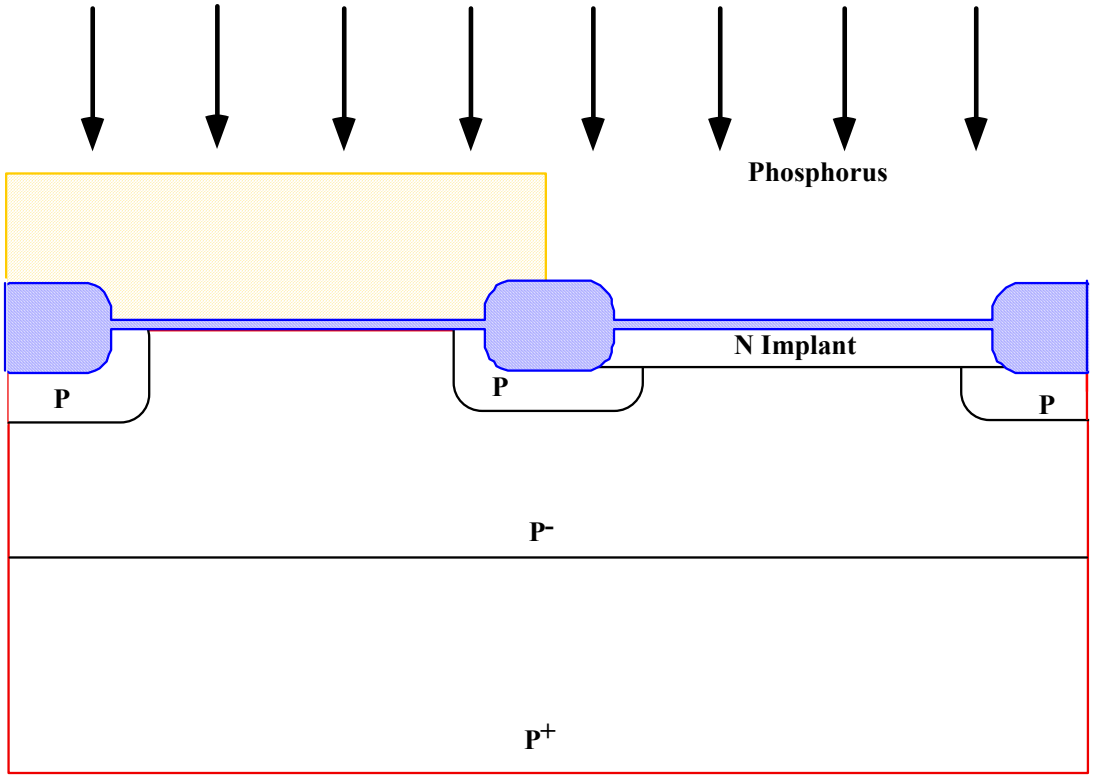


After growing a sacrificial oxide (wet or dry oxide, normally wet, at ~850-1100 C in a furnace or RTP system) a silicon nitride (shown in green) layer is deposited. In a furnace, this could be done by using dichlorosilane and ammonia, NH_3, at ~600-750 C.

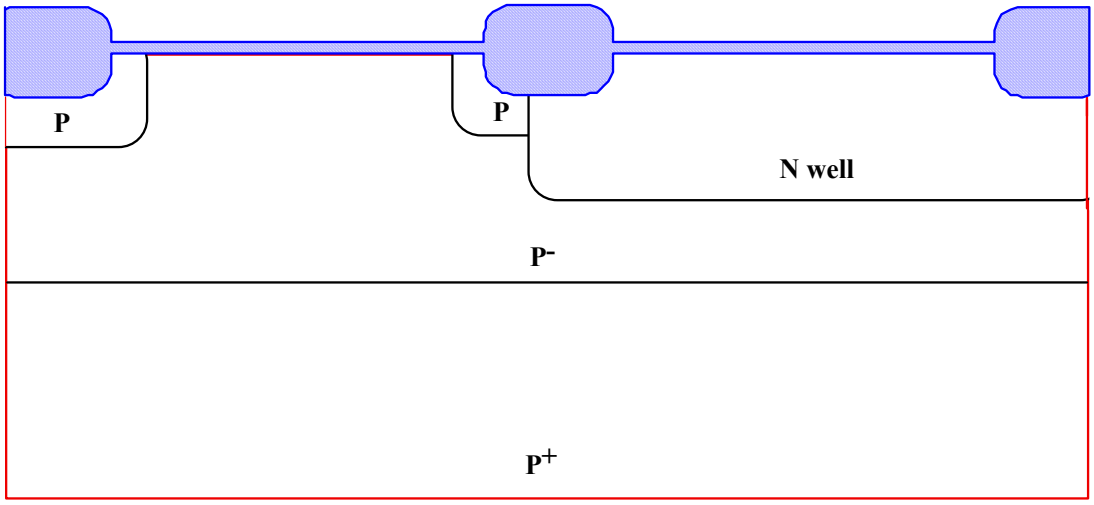
Mask #1 patterns the photoresist. The Si_3N_4 layer is removed where it is not protected by the photoresist by dry etching (RIE, ICP etc...) . Since the technology uses field implants below the field oxide, a boron implant is used to dope these P regions.



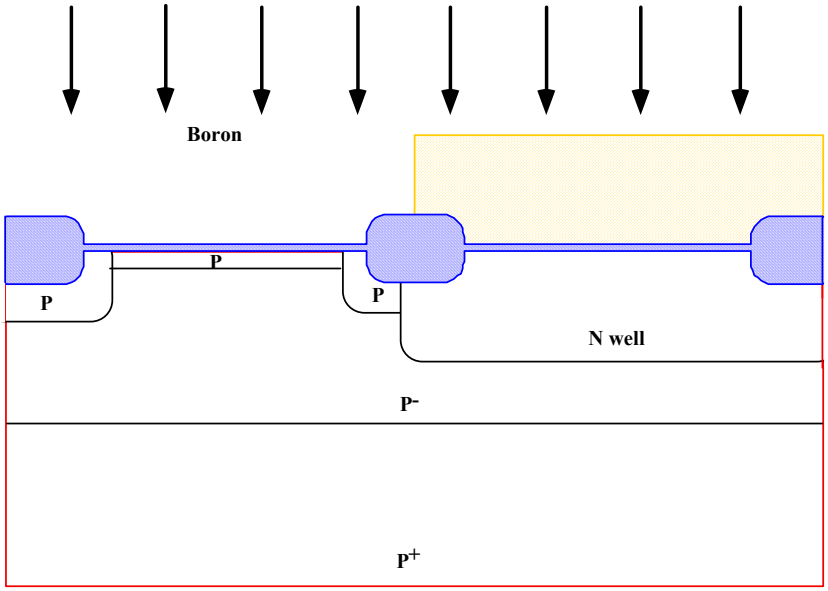
During the LOCOS oxidation, the boron implanted regions diffuse ahead of the growing oxide producing the P doped regions under the field oxide. The Si_3N_4 is stripped after the LOCOS process.



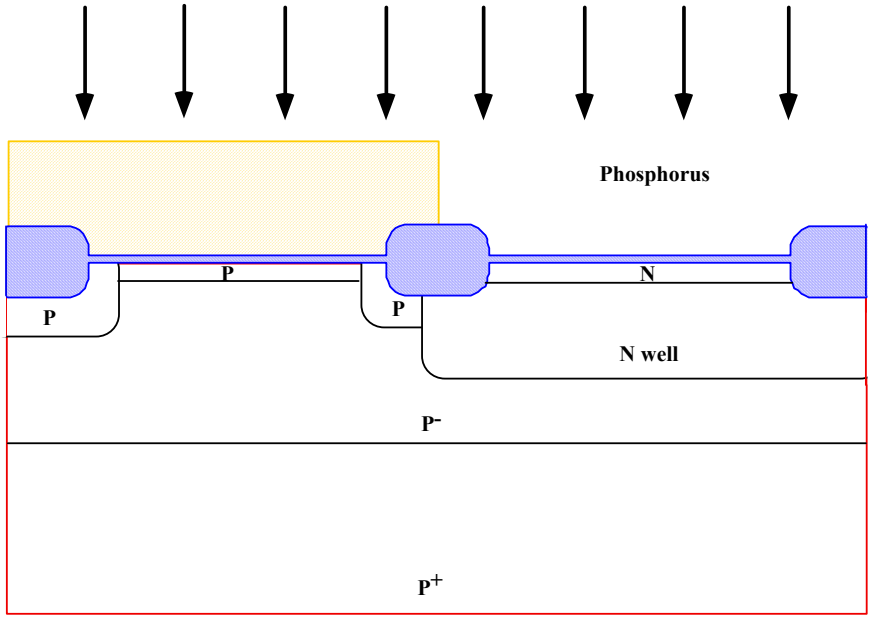
Mask #2 is used to form the N well. Photoresist is used to mask the regions where NMOS devices will be built. A phosphorus implant provides the doping for the N wells for the PMOS devices. The well is driven deep (if needed) by a high temperature anneal.



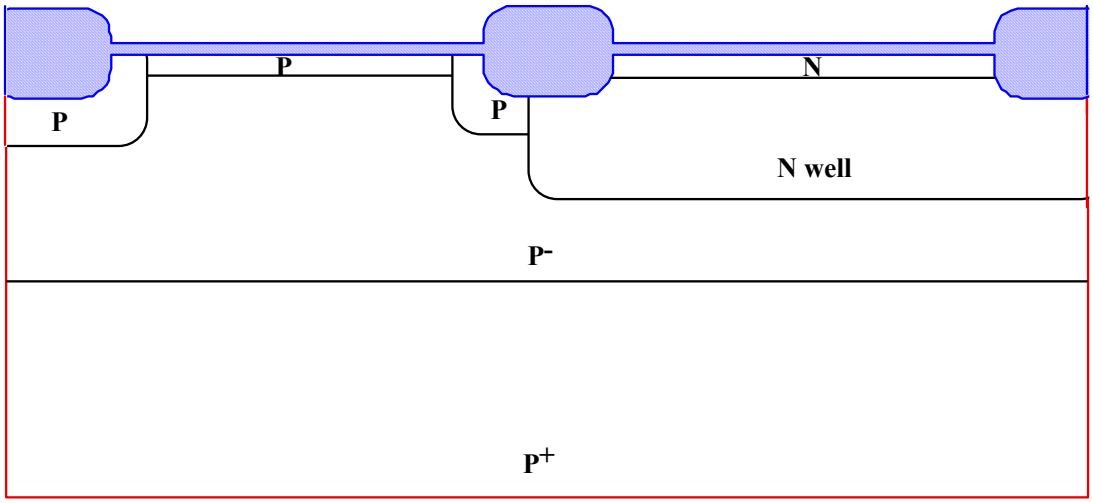
The high temperature drive-in completes the formation of the N well.



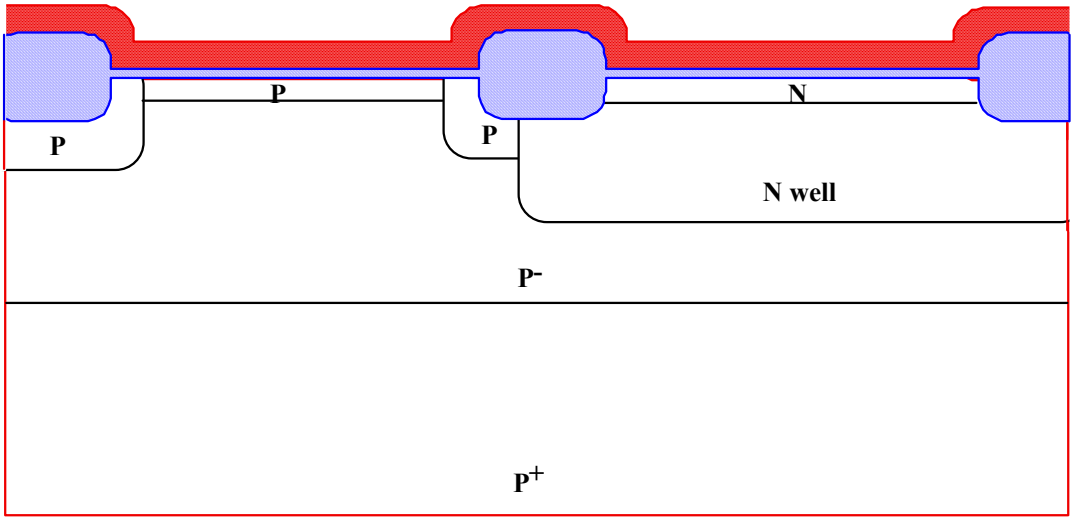
After spinning/defining photoresist on the wafer, mask #3 is used to define the NMOS transistors. A boron implant adjusts the N channel threshold voltage, V_{TH}.



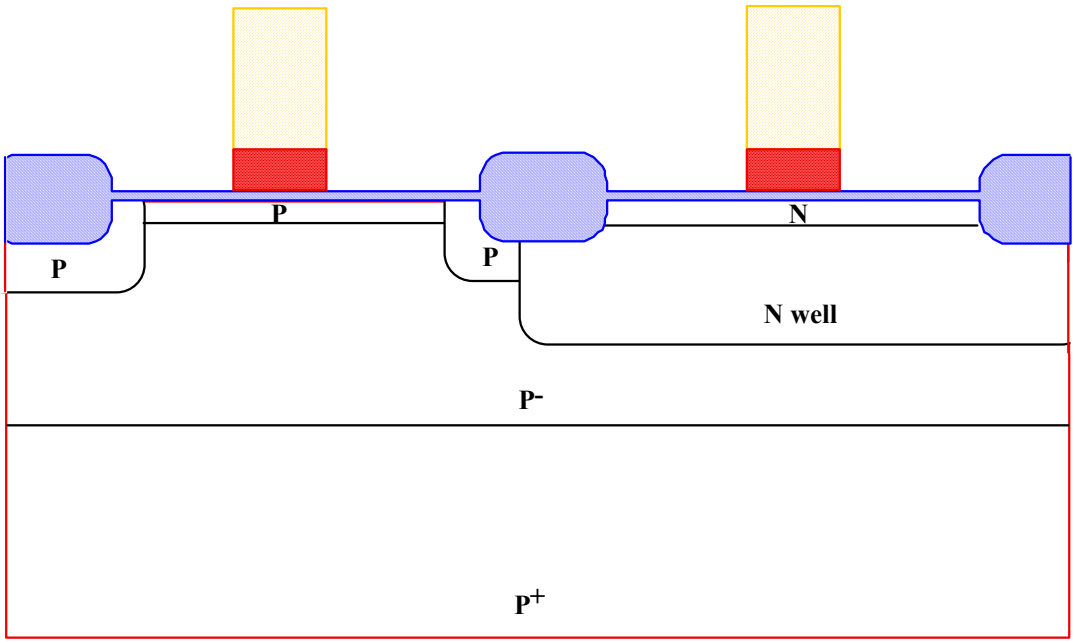
After spinning/defining photoresist on the wafer, mask #4 is used to define the PMOS transistors. A phosphorus or arsenic implant adjusts the P channel threshold voltage, V_{TH}. (Depending on the N well doping, a boron implant might actually be needed at this point instead of an N type implant, to obtain the correct threshold voltage.)



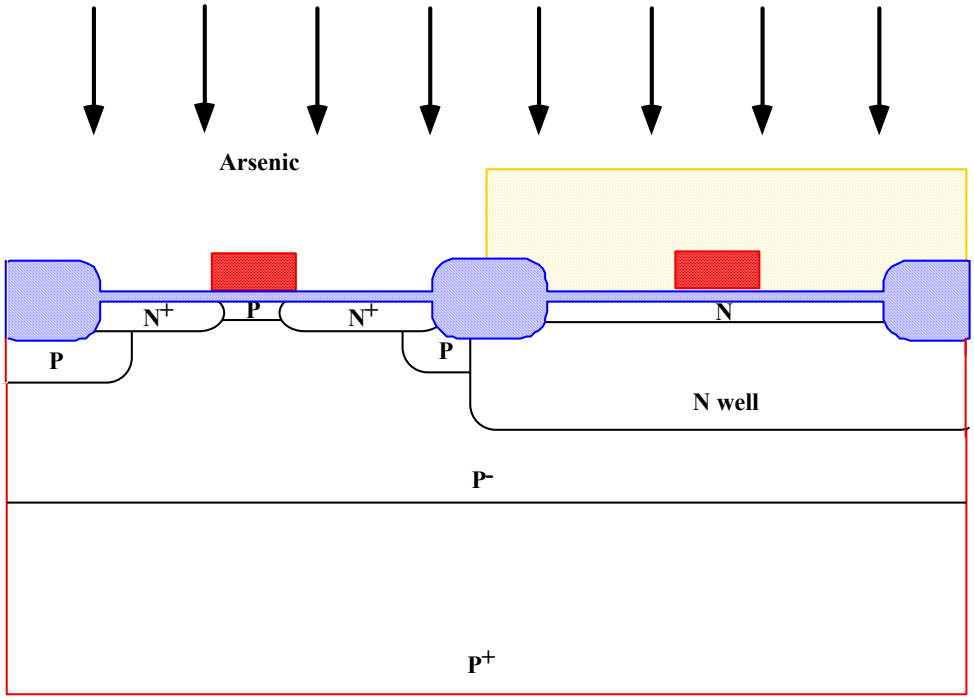
After etching back the thin oxide to bare silicon, the gate oxide is grown for the MOS transistors.



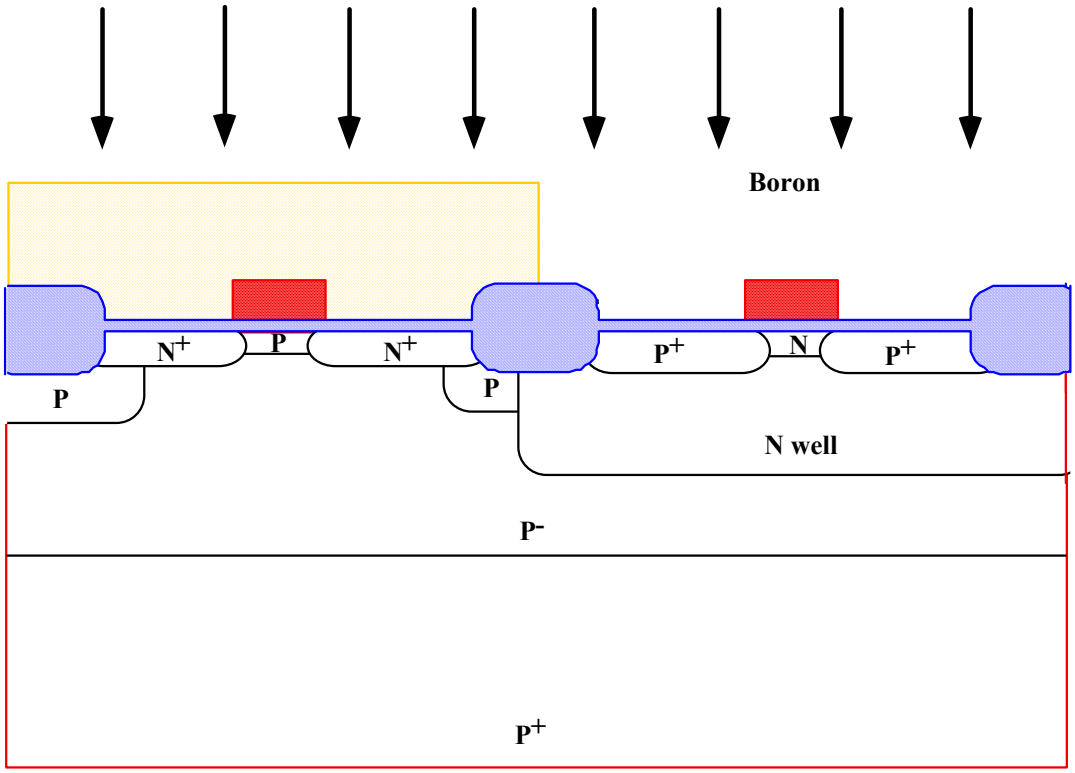
A layer of polysilicon is deposited. The poly-Si is either doped during deposition or Ion implantation of phosphorus follows the deposition to heavily dope the poly. Deposition will likely use silane in the 575-650 degree range. If doped during deposition, phosphine can be use to dope the poly-Si.



Photoresist is applied and mask #5 is used to define the regions where MOS gates are located. The polysilicon layer is then etched using plasma etching.

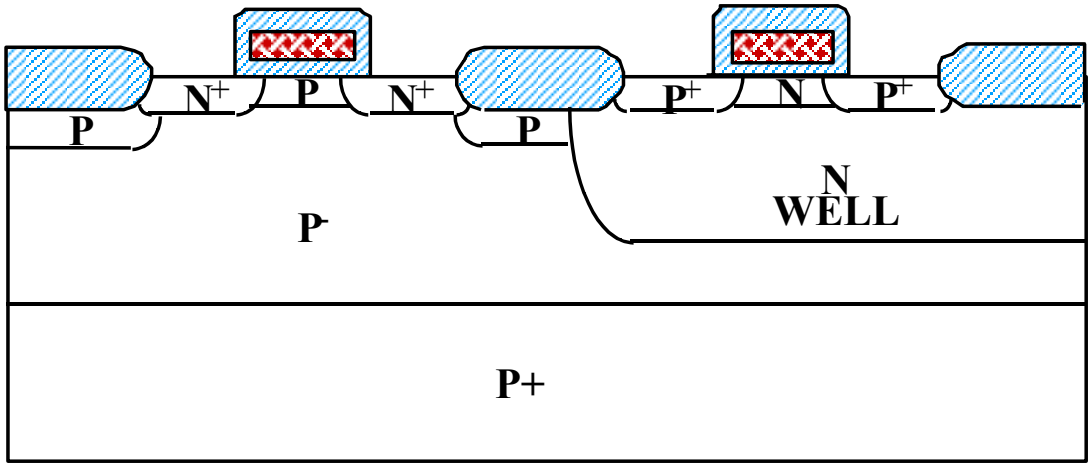


Photoresist is applied/defined and mask #6 is used to protect the PMOS transistors. An arsenic implant then forms the NMOS source and drain regions.

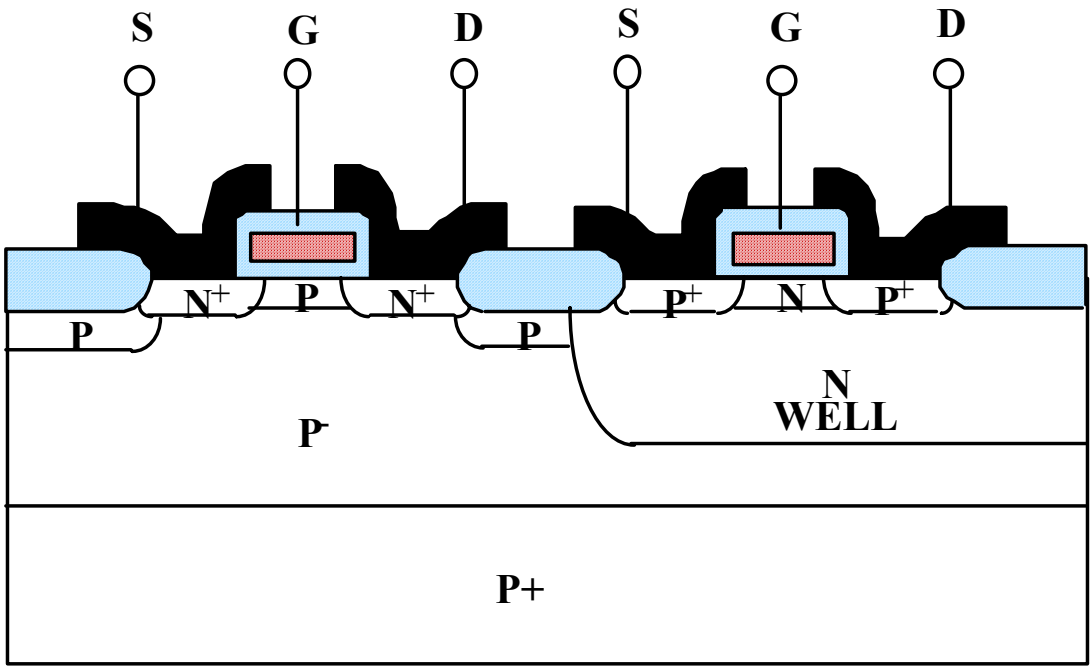


After applying/defining photoresist, mask #7 is used to protect the NMOS transistors. A boron implant then forms the PMOS source and drain regions.

At this point we have completed the formation of the active devices, except for a final high temperature anneal to activate the dopants and drive in the junctions to their final depth.



The gate isolation oxide is deposited. This is a PBSG layer (doped oxide) and is patterned and heatedto round off the edges.



Finally the metal lines are added. These may be Al (most common), or Cu (more modern) and will likely have a metal silicide layer for contact adhesion (Al case) or a diffusion barrier (Ta, TaN, Ti, TiN, etc...) for Cu. The Al metal is deposited with a sputtering system (most common) or an evaporator. Cu is done with a CVD or sputtered seed layer followed by an electrodeposited thick layer. The final pattern is etched to form the contacts.