Lecture 15

Process Integrations

Reading:

Selections from Chapters 15-18

Analog Technology: Bipolar Junction Transistors

Consider a lateral npn transistor (makes up a significant percentage of analog devices used)

1.) Diffuse a n-type (20-50 ohms/sq) "buried layer" into a p-type (~1e16 Boron doped) wafer.

2.) Use CVD to grow a high quality, single crystal epitaxial layer. If a BVCEO=36 V is desired, a reasonable margin of error is a C-B depletion width that can withstand 90V. This requires an epitaxial width of:

6 um @ 1e15 for depletion width in collect.
+8 um due to buried layer diffusion
+3 um required for the base
17 um thick CVD layer

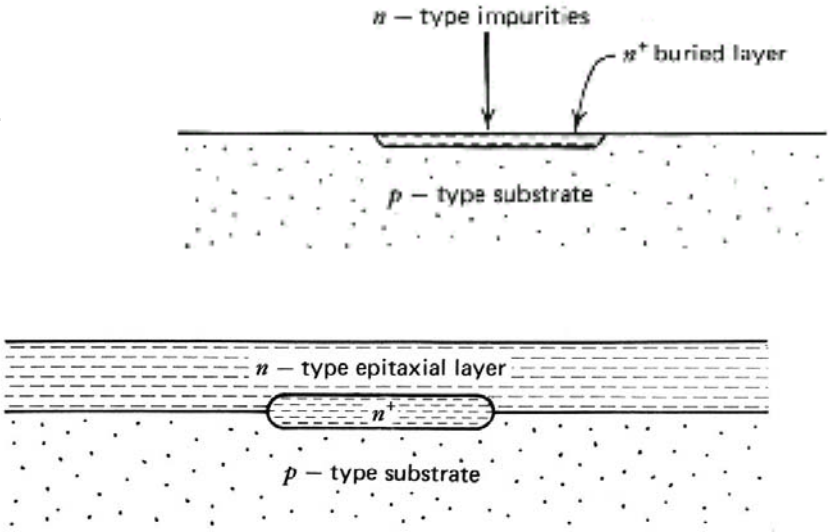


Figure 2.11 Bipolar integrated-circuit wafer following epitaxial growth.

3.) Isolation diffusion or Trenches
A very high temperature, long time p-type (~20-40 ohms/sq.) diffusion must be formed to "isolate" one device from another. Alternatively a trench can be etched, p-type implanted, oxidized, filled with poly-Si and re-oxidized (will describe this later in MOS discussion).

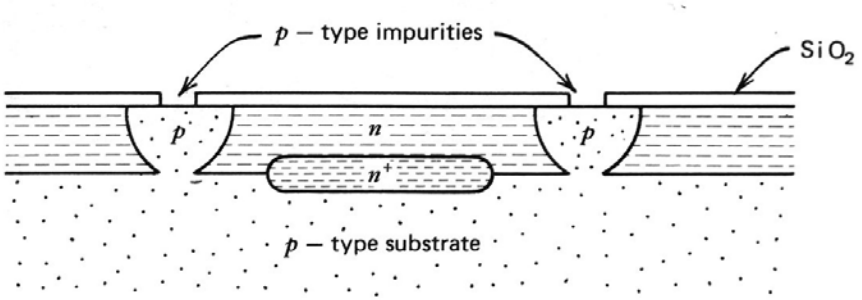


Figure 2.12 Structure following isolation diffusion.

Analog Technology: Bipolar Junction Transistors

4.) The p-type (100-300 ohms/sq) base is diffused ~1-3 um deep.

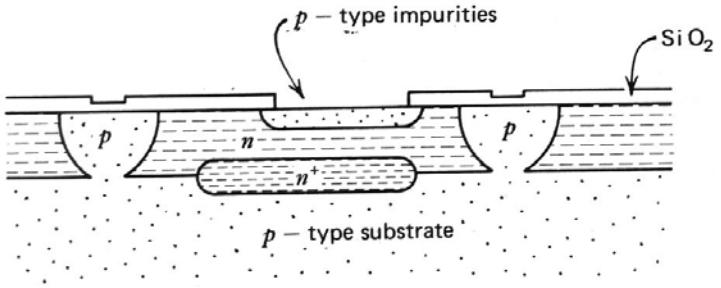


Figure 2.13 Structure following base diffusion.

5.) The n-type (2-10 ohms/sq.) emitter and a low resistance collector contact pad is simultaneously diffused ~0.5 to 2.5 um. The

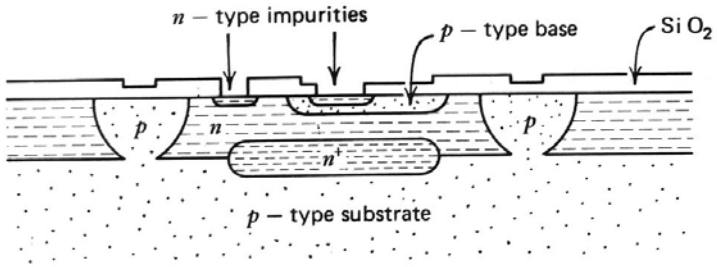


Figure 2.14 Structure following emitter diffusion.

6.) Aluminum or poly-Si/Aluminum or metal-silicide/aluminum is deposited over the wafer contacting the opened windows of the Base, Emitter and collector.

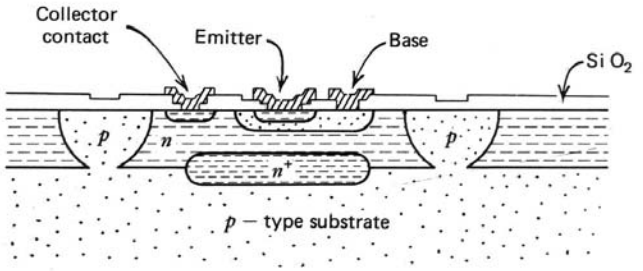


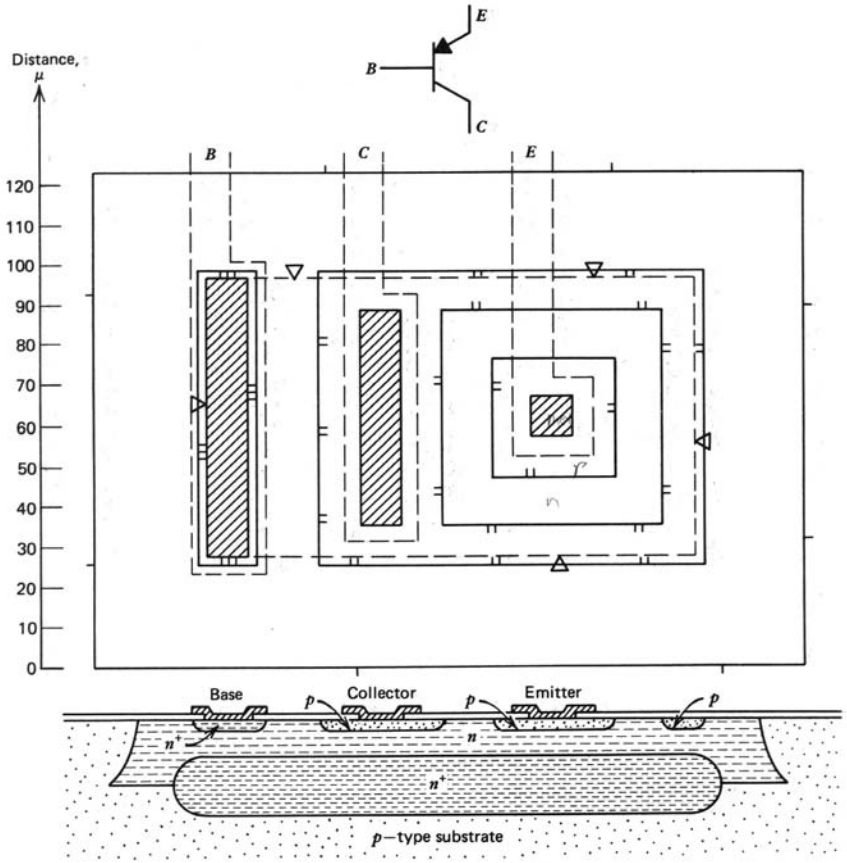
Figure 2.15 Final structure following contact mask and metallization.

7.) The interconnect pattern is etched into the aluminum, leaving only the desired wiring pattern.

Analog Technology: Bipolar Junction Transistors

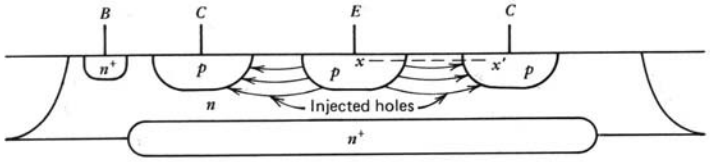
Lateral PNP Transistor:

Collector is a ring around the emitter. The emitter is separated from the collector by the base region (whose contact is outside of the collector).



(a)

Figure 2.24*a* Lateral *pnp* structure.



(b)

Figure 2.24*b* Minority-carrier flow in the lateral *pnp* transistor.

Analog Technology: Bipolar Junction Transistors

Substrate PNP Transistor:

For some power electronic devices, the epi thickness required is sometimes unreasonably thick (the thickness is needed to support a very large depletion region for high voltage devices). For these applications, the entire wafer thickness can be used as the collector.

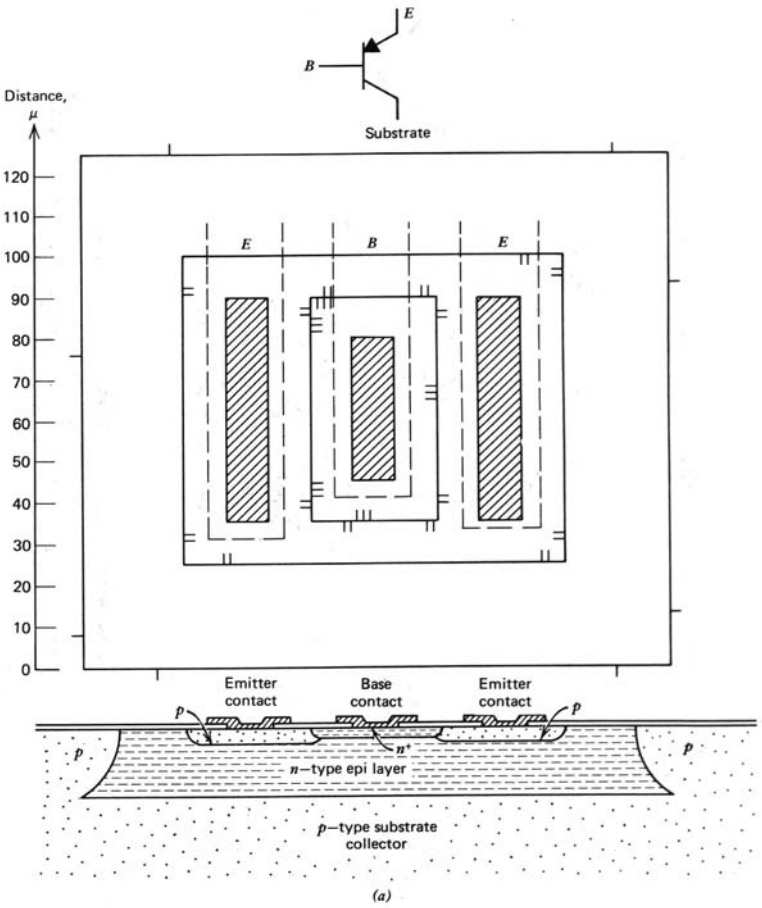


Figure 2.27*a* Substrate *pnp* structure.

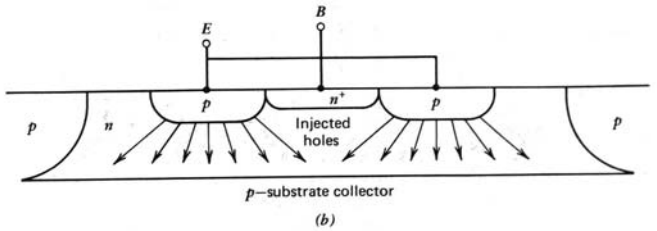


Figure 2.27*b* Minority-carrier flow in the substrate *pnp* transistor.

Analog Technology: Resistors and Capacitors

Resistors can be formed via base diffusion step (of a BJT), pinched resistor (base and emitter diffusion) or poly-Silicon or Semi-insulating Poly Silicon (SIPOS formed by oxygen "doped" CVD of polysilicon) depending on the resistance needed..

Capacitors can be formed by poly-Si separated by a dielectric. The use of high permitivity dielectrics can lead to increased capacitance without increased area. Most modern capacitors save area by using deep, high aspect ratio trenches. In (digital) Random Access Memory (RAM) chips, these trenches can store the charge required for maintaining logic and isolate neighboring transistors simultaneously.

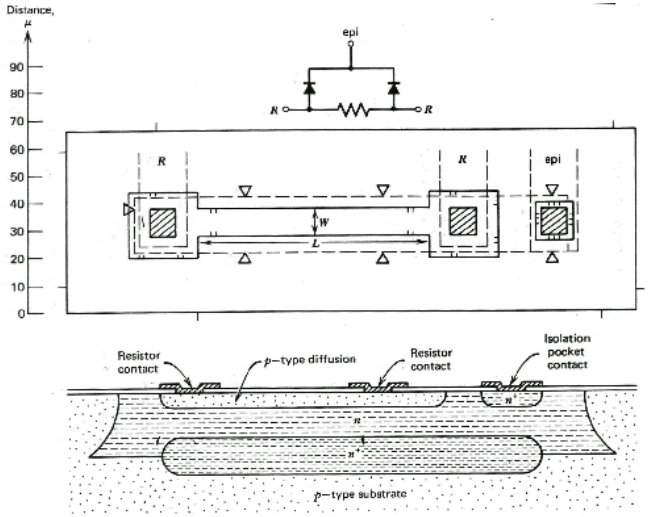


Figure 2.30 Base-diffused resistor structure.

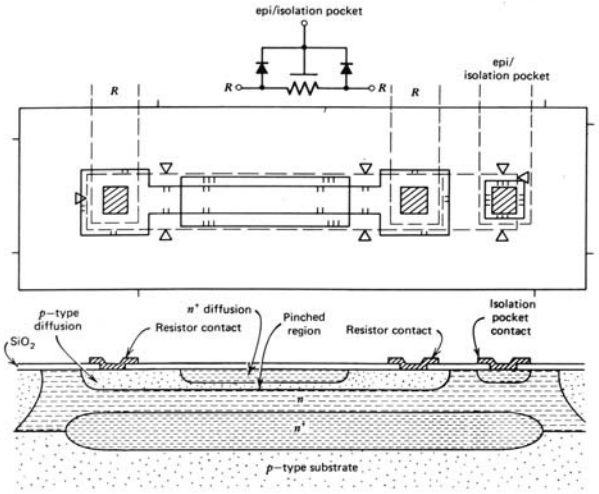


Figure 2.32 Pinch resistor structure.

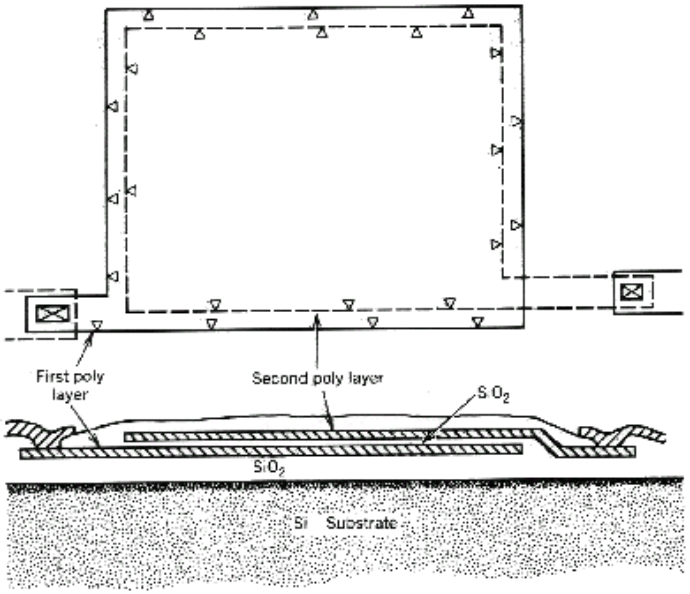
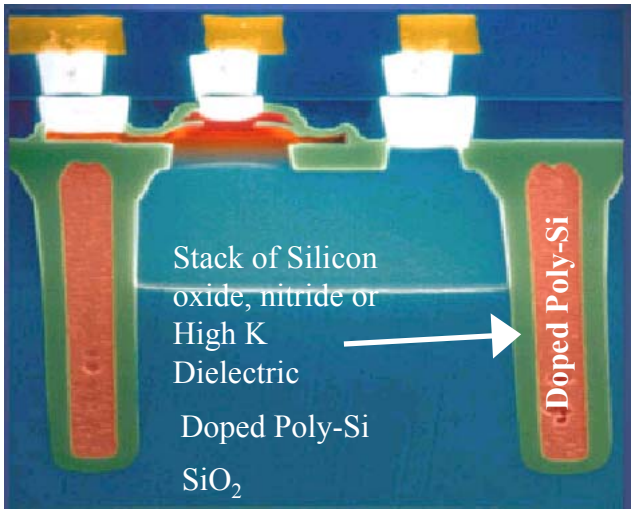


Figure 2.55*b* Plan view and cross section of typical poly–poly capacitor.



Oxide Isolated Self-Aligned Metal-Oxide Semiconductor Field Effect Transistors

1.) A field/gate oxide and CVD Nitride are grown and deposited on a n-type wafer.

2.) The dielectrics are patterned to cover the future device areas.

3.) The n-channel FET is protected with PR and a high energy, deep p-type implant/anneal forms the p-doped well.

4.) A second low energy very high dose implant is used to form the p-type isolation guard rings around the p-type well.

5a.) The LOCOS (Local Oxidation of Si) oxide is grown driving the guard rings deeper and isolating the active areas. The nitride is stripped and an optional implantation step to control the turn on voltage of devices is performed.

5b.) A poly SI gate contact and interconnects are deposited and defined with lithography.

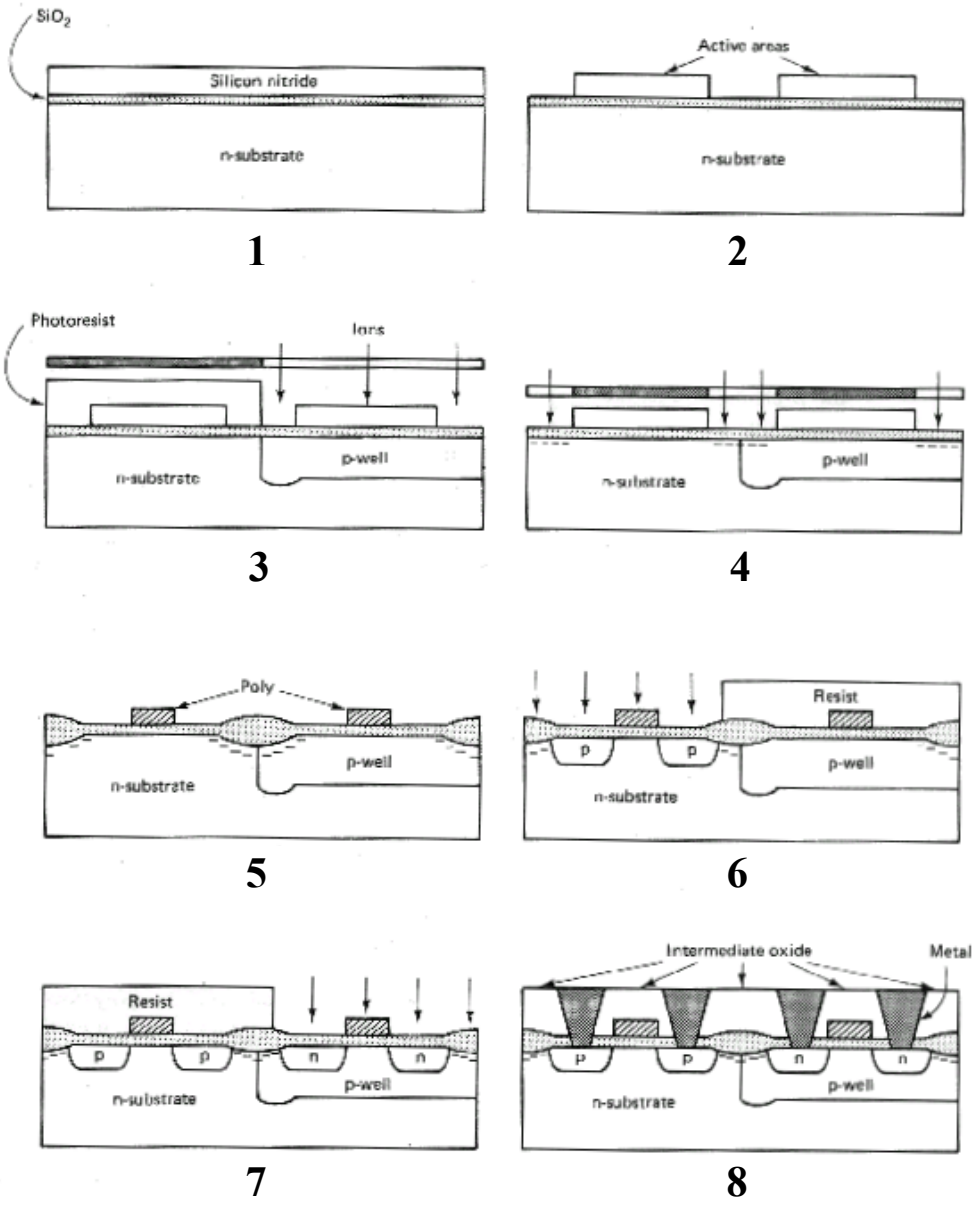


Figure 4.9 Oxide-isolation CMOS process.

Oxide Isolated Self-Aligned Metal-Oxide Semiconductor Field Effect Transistors

6.) The source and drain implants/anneals are performed in the n-channel then the (7) p-channel regions. The Poly-Si gate acts as a mask, thus coining the phrase "self aligned".

8a.) A doped (undoped for Damascene) CVD oxide is deposited and windows are opened up. If Damascene, skip to 14.

8b.) An optional reflow of the doped oxide can be performed.

8c.) The metal contacts are formed (Ti, TiN, W, Ta, TaNx or Al) are deposited.

8d.) An interlayer dielectric is deposited, patterned and metalized for the next interconnect layer.

8e.) The metal is deposited, polished back (Damascene process only) to a planar structure.

8f.) Repeat 13 & 14 as many times as necessary to construct the circuit.

9 – not shown.) A nitride protective layer is deposited over everywhere. Holes are opened up for contacts to the IC package

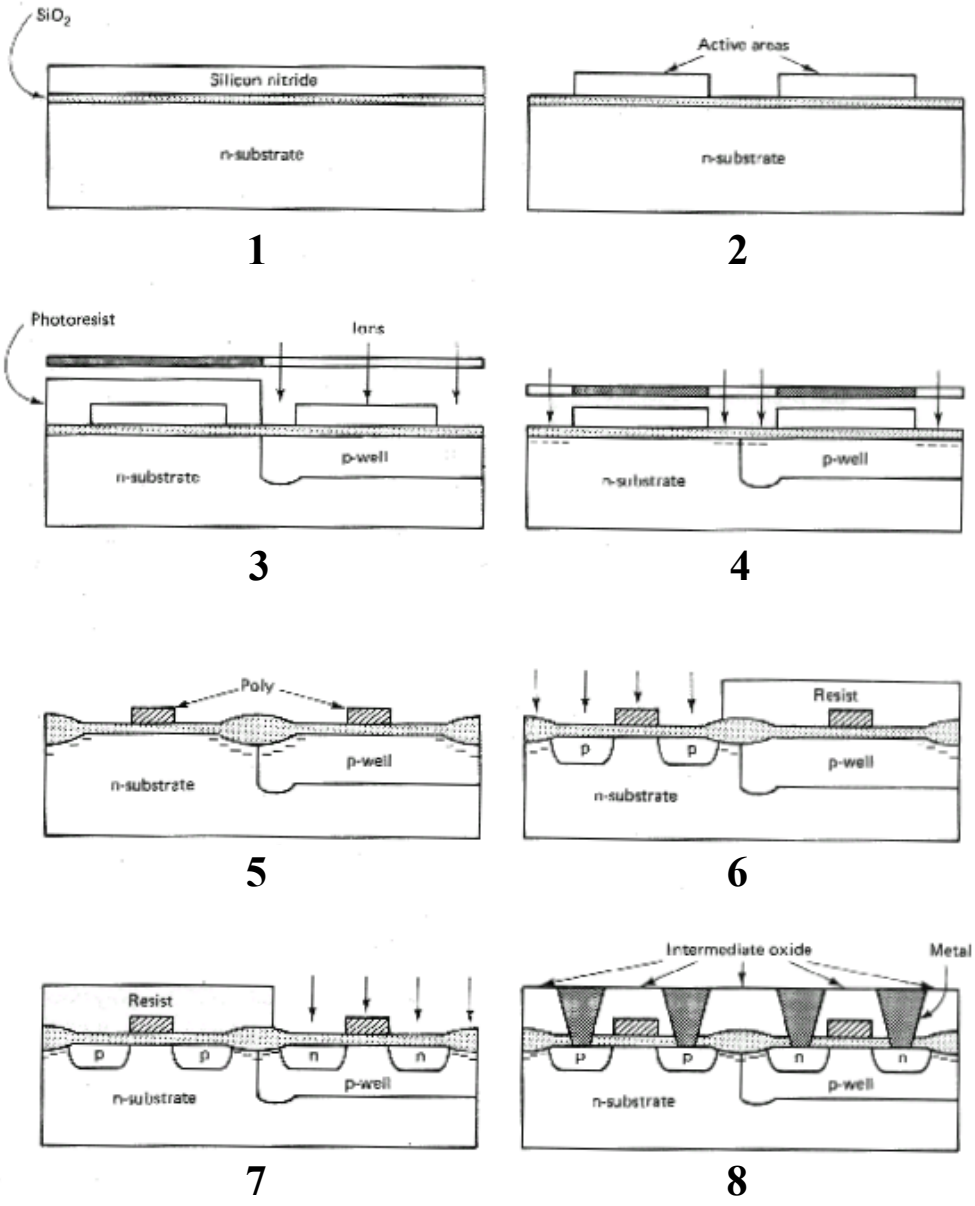


Figure 4.9 Oxide-isolation CMOS process.

Trench Isolated Self-Aligned Metal-Oxide Semiconductor Field Effect Transistors

Trench Isolation: The LOCOS isolation is replaced with etch trenches that are implanted, oxidized, filled with poly-si filler material and then re-oxidized.

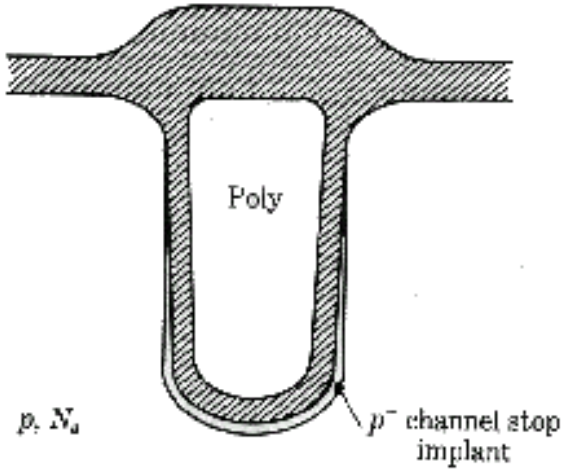


FIGURE 5.31 Example of nonideal trench cross section.

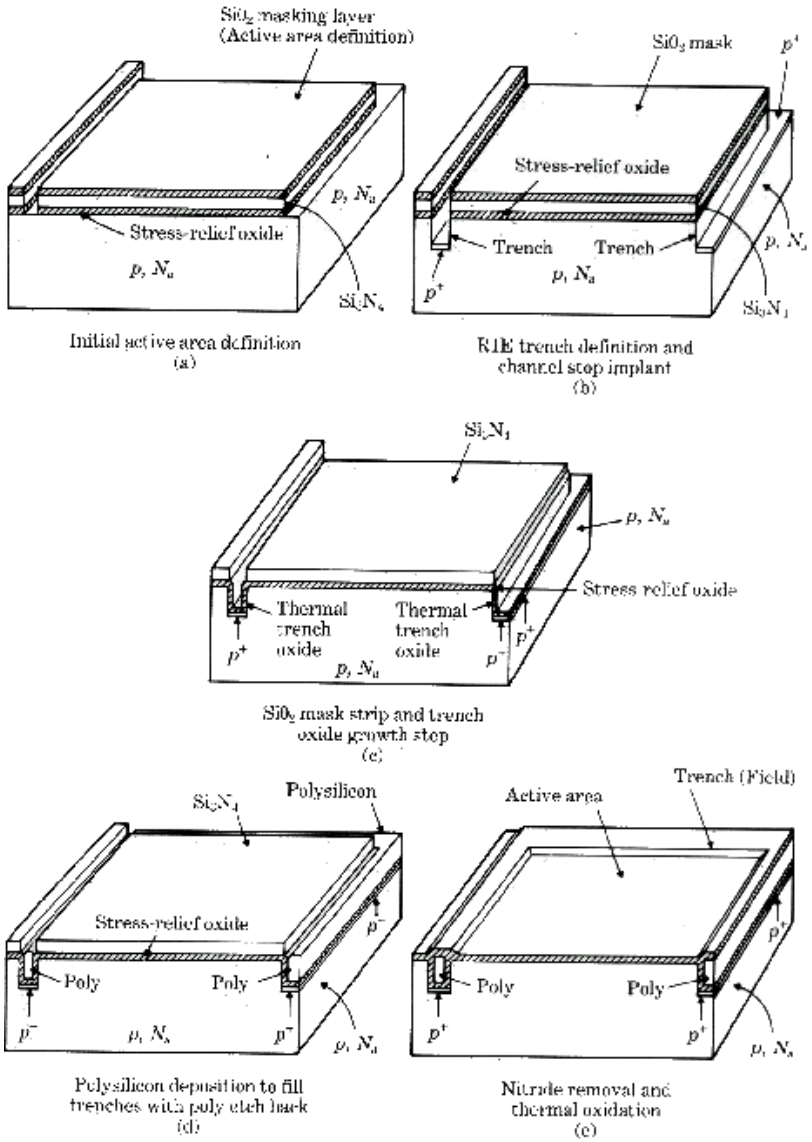


FIGURE 5.29 Basic sequence for trench isolated integrated circuits.

Oxide Isolated Self-Aligned Metal-Oxide Semiconductor Field Effect Transistors

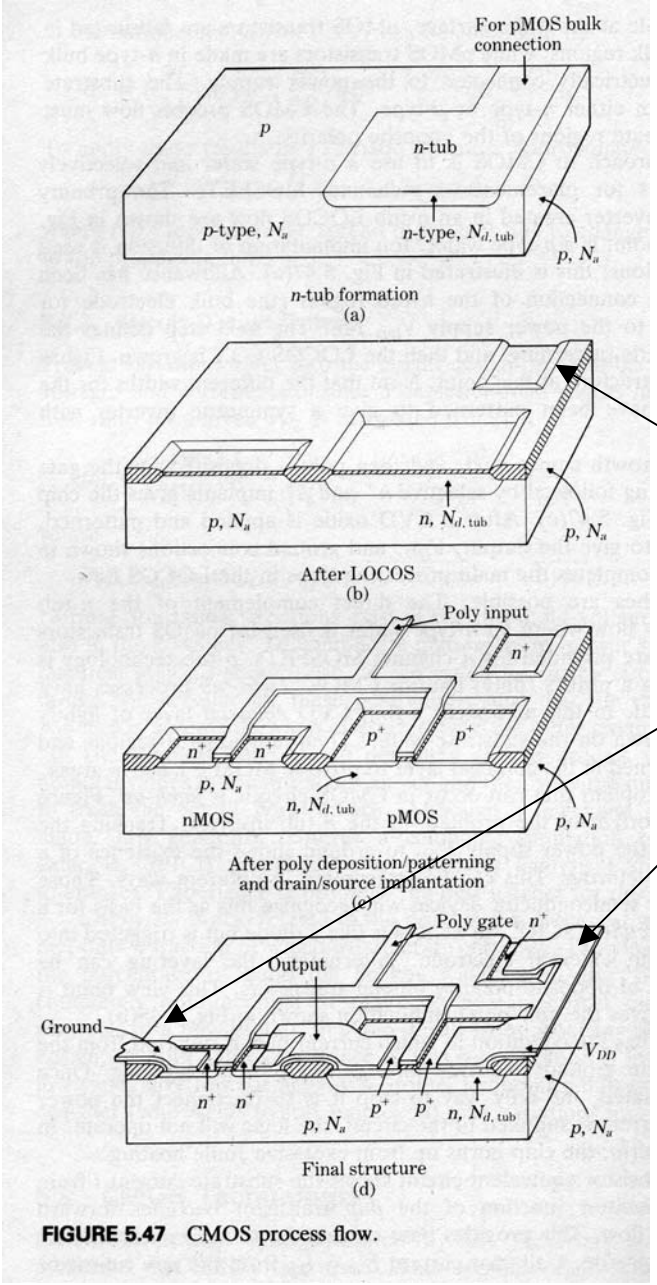


FIGURE 5.47 CMOS process flow.

One also needs to allow for connections to properly bias the wells as shown.