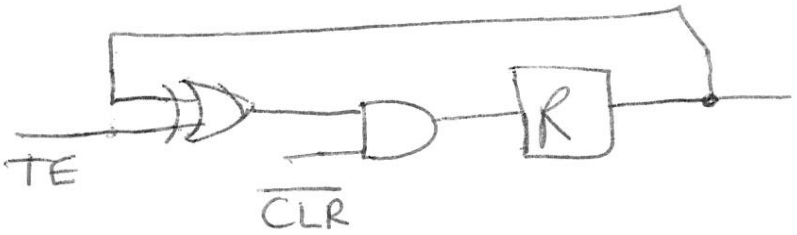
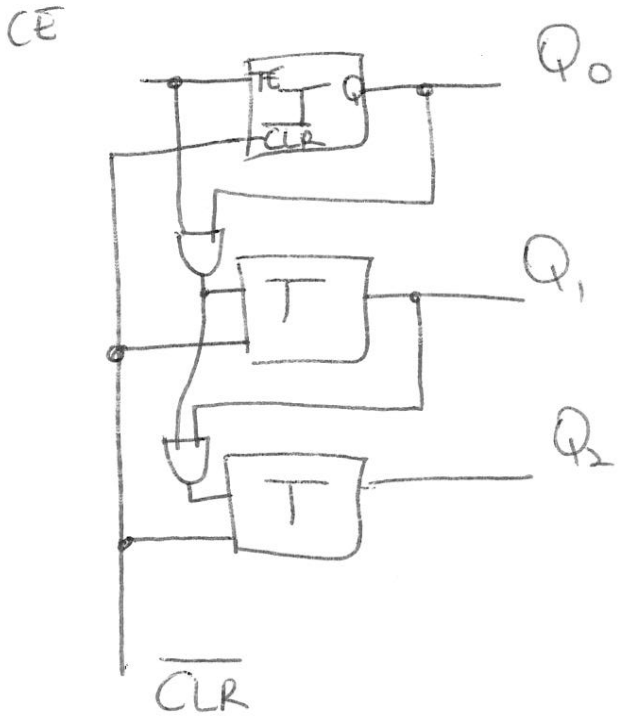
ECE 2030 Spring 2006 Test 3 sol, Dr. Heck

Problem 1 (25 Points):

a) Draw the schematic of a toggle cell using gates and registers.



b) Draw the schematic of a 3-bit counter using toggle cells and gates.

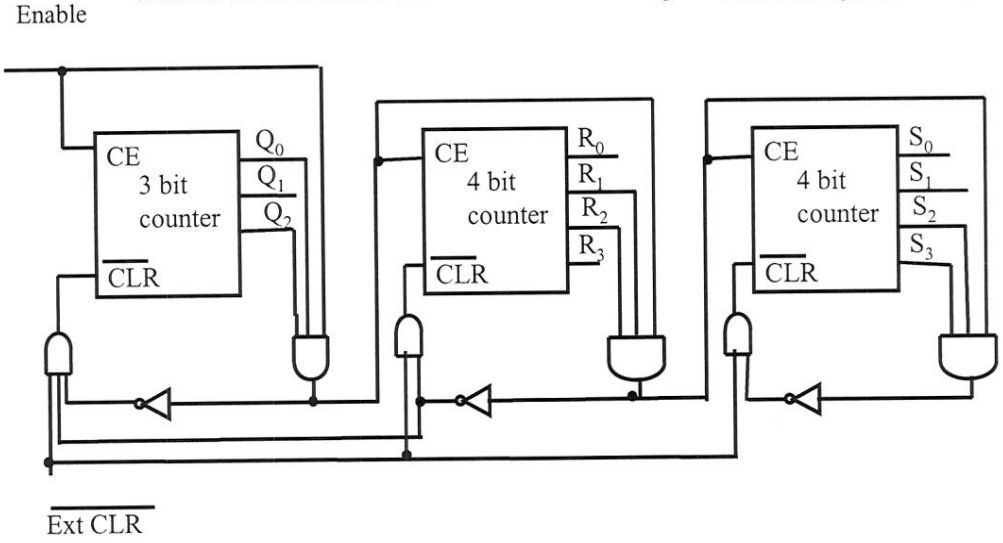


c) Consider the set of counters shown below. (Note, don't worry if the counter is connected in a way that doesn't make sense. It is not meant to be practical.)

What is the maximum of the counter on the left? $101_2 = 5_{10}$

What is the maximum of the counter in the middle? $110_2 = 6_{10}$

What is the maximum of the counter on the right? $1100_2 = 12_{10}$



d) For this same counter, consider the sequences below. Suppose that Enable = 1 and $\overline{\text{EXT CLR}} = 1$. Complete the table for the next three sets of values starting from the value given.

S_3	S_2	S_1	S_0	R_3	R_2	R_1	R_0	Q_2	Q_1	Q_0
1	0	0	0	0	0	1	0	0	1	1
1	0	0	0	0	0	1	0	1	0	0
1	0	0	0	0	0	1	0	1	0	1
1	0	0	0	0	0	1	1	0	0	0

e) Repeat part d) for the starting count shown below.

S_3	S_2	S_1	S_0	R_3	R_2	R_1	R_0	Q_2	Q_1	Q_0
1	0	0	1	0	1	1	0	1	0	0
1	0	0	1	0	1	1	0	1	0	1
1	0	1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	1

Problem 2 (25 Points): Different size memory systems are to be built from 64M x 8 memory chips. Answer the following questions.

How many memory cells are in the memory chip? 2^{29} 2^{26} 2^3

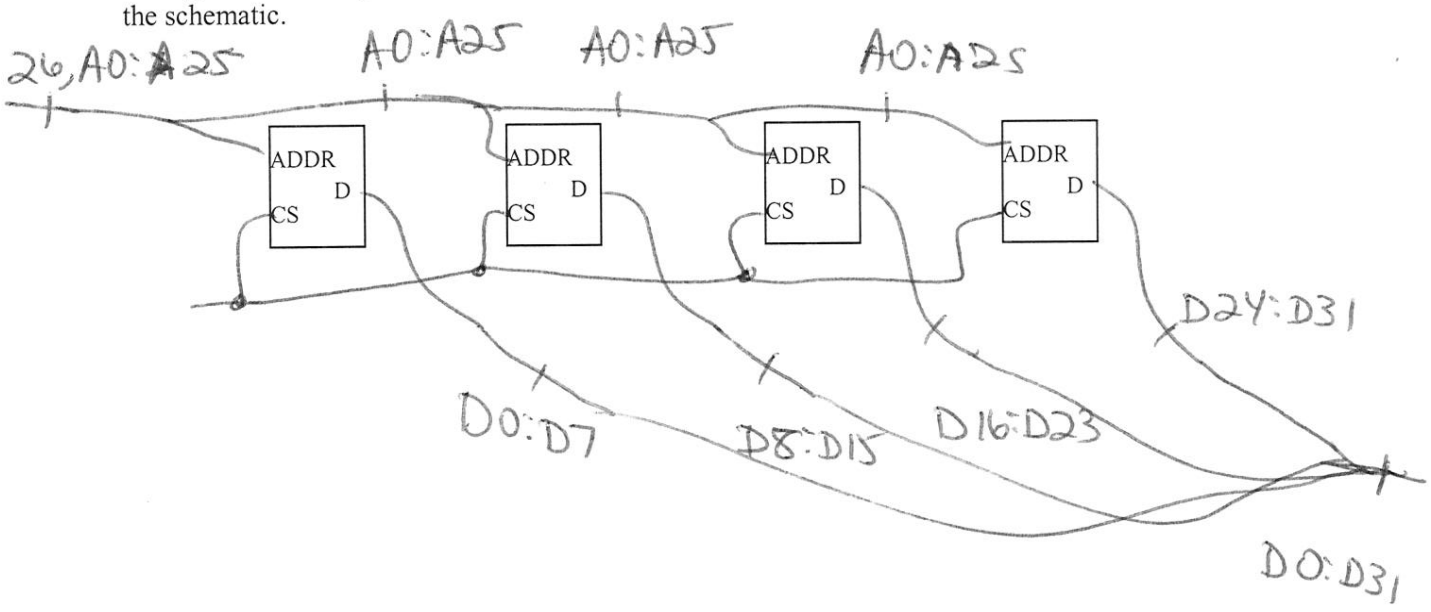
How many address lines are used for the memory chip? 26

Case 1: A 64M x 32 memory system.

How many banks are in the memory system? 1

How many address lines are used for the memory system? 26

Show the schematic of the memory system using the memory chips shown below. Identify all buses (using the notation An:Am and Dn:Dm, where n and m represent the starting and the ending line numbers), the sizes of all buses, and add any extra components needed to complete the schematic.

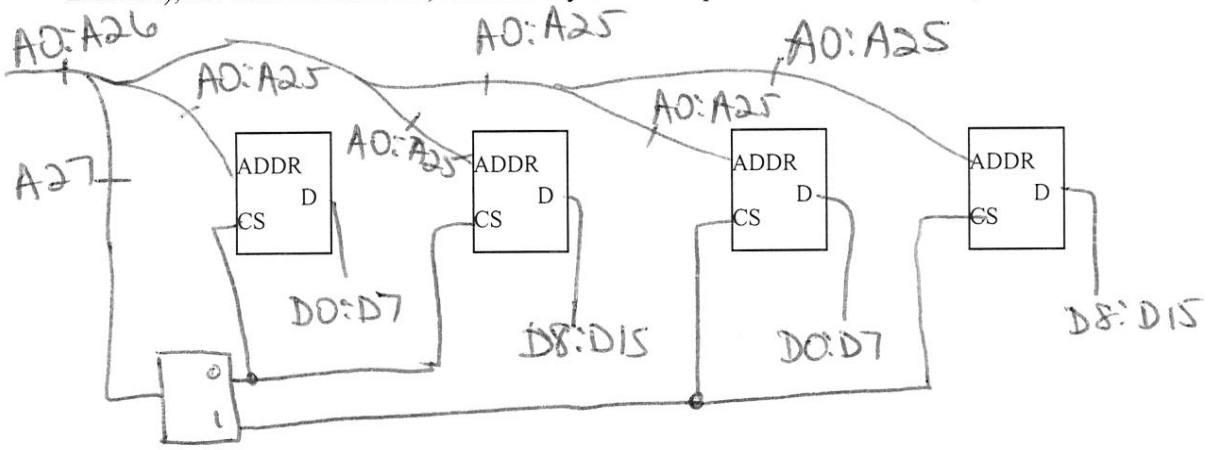


Case 2: A 128M x 16 memory system.

How many banks are in the memory system? 2

How many address lines are used for the memory system? 27

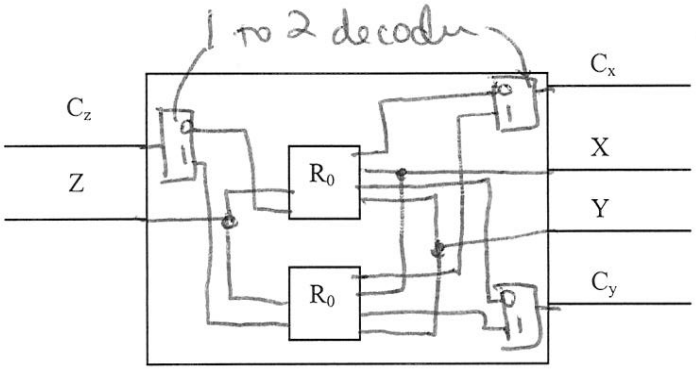
Show the schematic of the memory system using the memory chips shown below. Identify all buses (using the notation An:Am and Dn:Dm, where n and m represent the starting and the ending line numbers), the sizes of all buses, and add any extra components needed to complete the schematic.



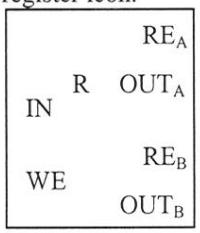
1 to 2 decoder

Problem 3 (20 Points):

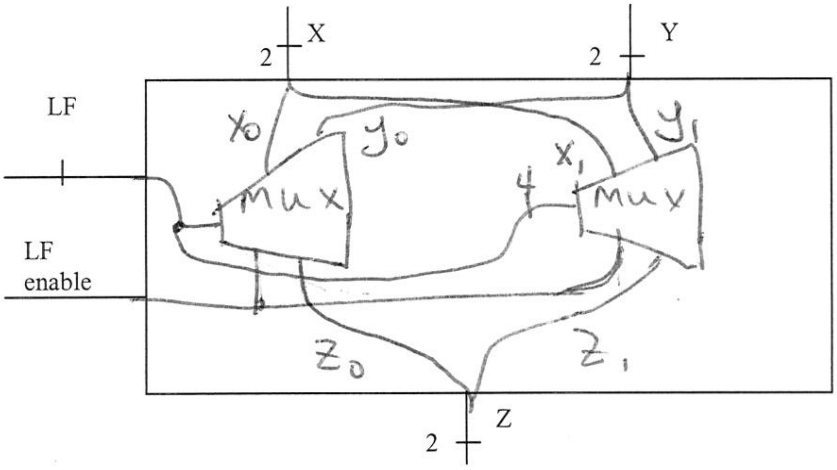
a) Complete the schematic of a register file that contains 2 registers. Identify all lines and components used. (You do not need to show the register write enable in this schematic.)



Expanded view of the register icon.



b) Complete the schematic of a 2 bit logic unit.



Problem 4 (30 Points):

Write the microcode to complete the following operations

1 $R_2 = R_1$ AND R_5
2 $R_3 = R_4/8$
3 $R_4 = R_5 \times 4$
4 $R_{10} = R_1 - R_3$
5 $M[R_2] = R_3$
6 $R_4 = M[R_1]$

unmarked spots are don't cares

Step	cX	cY	cZ	RWE	imm. en.	imm val.	au en	ā / s	lu. en.	l.f.	st. en.	s.t.	store en.	load en.	r / w̄	mem. sel.
1	1	5	2	1	0		0		1	1000	0		0	0		0
2	4		3	1	1	3	0		0		1	1	0	0		0
3	5		4	1	1	-2	0		0		1	1	0	0		0
4	1	3	10	1	0		1	1	0		0		0	0		0
5	2	3		0	0		0		0		0		1	0	0	1
6	1		4	1	0		0		0		0		0	1	1	1

Consider the following assembly code. Write the corresponding microcode for these instructions.

1. ADD \$1,\$2,\$3
2. ADDI \$1,\$1,1
3. OR \$4,\$3,\$2

Step	cX	cY	cZ	RWE	imm. en.	imm val.	au en	ā / s	lu. en.	l.f.	st. en.	s.t.	store en.	load en.	r / w̄	mem. sel.
1	2	3	1	1	0		1	0	0		0		0	0		0
2	1		1	1	1	1	1	0	0		0		0	0		0
3	3	2	4	1	0		0		1	1110	0		0	0		0