

ECE 2030 Homework 4

Due Thurs. February 19

1. Build circuits using decoders to implement the following logic:

a) $F = \overline{(\overline{AB} \overline{C} + \overline{D})}A$

b) $F = \overline{A} \overline{B} C + AB$

c) $F = (A + B)(A + \overline{B} + C + D)(\overline{A} + \overline{D})$

d) $F = \sum m(0,4,8,12,14)$

2. Design a priority encoder with the following priorities: $D_0 > D_1 > D_2 > D_3$
3. Design a 1 to 4 demux. (Hint: examine the transmission gate implementation of the 4 to 1 mux)
4. Fill in the following truth table for a 2 to 1 MUX with inputs $D_0=B$ and $D_1=A$, and switch lines $S_0 = Y$ and $S_1 = X$.

AB	XY	OUT
00	00	
00	01	
00	10	
00	11	
01	00	
01	01	
01	10	
01	11	
10	00	
10	01	
10	10	
10	11	
11	00	
11	01	
11	10	
11	11	

5. Perform the following additions assuming 2's complement, 5 bit representation

$$\begin{array}{r} 01110 \\ +10110 \\ \hline \end{array}$$

$$\begin{array}{r} 10110 \\ +10010 \\ \hline \end{array}$$

$$\begin{array}{r} 01101 \\ +00111 \\ \hline \end{array}$$

$$\begin{array}{r} 11101 \\ +11111 \\ \hline \end{array}$$

Error? _____ Error? _____ Error? _____ Error? _____