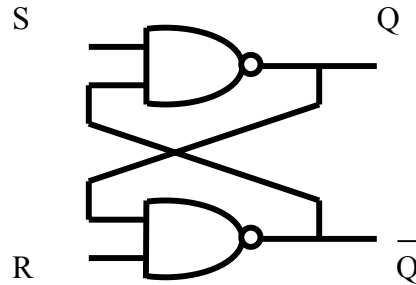


ECE 2030 Homework 5

Due Thurs. February 26

1) Give a truth table that shows all the stable operating states for this circuit.



Consider the following sequence for S and R. SR = 00, SR = 01, SR = 11, SR = 10, SR = 00
Fill in the corresponding output for Q into the table.

SR	00	01	11	10	00
Q					

2) Draw the schematic for a 3 bit adder/subtractor including the add/subtract bit and the error checking.

3) Draw the following timing diagram:

