Analog--Digital Auditory Signal Processing and Biologically Inspired Signal Processing

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...the road to smaller, cheaper, more energy-efficient consumer electronics may be paved with analog technology.

--- Wired Magazine, March 2003

For decades all effort and focus has been on miraculous advancements in digital chips, but the next ten years will see a shift in emphasis to analog technologies... 

--- Red Herring Magazine, February 2003
Gene’s Law and CADSP

Gene’s Law

DSP Power

CADSP Power

A 20 Year Leap in Technology

CADSP Power Savings

Sensor Signals

ASP IC

DSP/μC

Same Power
Increased Computation

Lower Power
Same Computation

• Increased Computation/mW

Computation
Resolution for Analog / Digital Tradeoffs

(a) POWER COSTS

(b) AREA COSTS

Limit set by
1/f noise
for a fixed
area consumption

Limit set by
thermal noise
for a fixed
power consumption

Input → 16bit A/D → FFT → DSP Application Program

SNR < 10 bits

Input → filter → 10 bit A/D → DSP Application Program
Basic Cochlear Models

- Matching
- Need for high Q, high SNR filters
- Cascades increase noise / distortion

Cochlea Designs: Lyon & Mead model / Sarpeskar, A. van Schaik (1997)
2D fluid modeling (L. Watts 1992)
Auditory Localization Using Cochleas

Higher order processing
- Binaural Hearing (Lazzaro, Mead)
- Cochlea front-end for recognition (Lazzaro, Andreou)
Floating-Gate Devices and Circuits

- Information Storage
- Floating-Gate Transistor
- Modifying Floating-Gate Charge
  - Electron tunneling
  - Hot-electron injection

- Reliable storage of analog charge levels
- Rapid Programming of devices (row parallel)
- Design to minimize Temp effects
- Several options for scaled processes

**Analog Circuits/Systems:** Tuning Offsets, Voltage Regulators, DACs, ADCs

**Floating-gate systems:** Auditory, Image, IF FPAA, Adaptive Systems, Classification

![Diagram of Floating-Gate Device]
Automatic Floating-Gate Programming

Row Parallel Block Diagram

- Pre-Process
- FG Core
- Pulse S/H & Current Measurement
- Modified SRAM
- Program MUX Logic
- Additional S/H & Measure Logic
- MUX Out Logic

Graph:
- X-axis: Year
- Y-axis: 1/minute, 1/second, 1000/second
- Data points indicating performance over time

Additional notes:
- 1000/second
- 1/second
- 1/minute
- Year range from 2001 to 2004
Computing in Memory

Today (Digital)

Tomorrow (Mixed Signal)

Memory

Input

Micro Processor (Pipelined Multiplexed)

Y = A * B

Computing Element
Continuous-Time Filterbank

- Programmable corner frequencies

- Second-order response from 32 Filters

- High corner is programmed to have exponentially spaced bias currents.

- Programmed in doublets (differential filters)

- Standard deviation from target = 0.506%
Peak / Min Level Estimation

output from peak detector = noisy signal level estimate

output from min detector = noise level estimate

Noisy signal

“Cleaner” output signal
Analog Auditory / Speech Processing

Analog-Digital Speech Recognition

Microphone → Cepstrum → VQ → HMM → Digital Signal Processing

Analog Cepstrum

Digital Cepstrum Outputs
Building a VQ Array

How to set the offsets?
• Programming
• Continuous Adaptation
Another viewpoint on Recognition

Can build circuits for HMM recognition based upon floating-gate circuits techniques that look similar to dendritic networks.
Conclusions

Programmable analog signal processing techniques allow real-time techniques not realizable for 20 years. (including some biologically motivated techniques)

Wide range of analog and digital signal processing techniques that developing rapidly.

Techniques open a large range of opportunities / new challenges for real-time signal processing.

Neuromorphic analog systems provide insight into biological processing and models/systems that can be directly used in signal processing problems.