

Finite Ground Coplanar Lines on CMOS Grade Silicon with a Thick Embedded Silicon Oxide Layer Using Micromachining Techniques

Guoan Wang, Andrew Bacon, Reza Abdolvand, Farrokh Ayazi, John Papapolymerou, and Emmanouil M. Tentzeris

School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA 30332-0250, USA

Abstract—Finite Ground Coplanar (FGC) waveguide transmission lines on CMOS grade silicon wafer ($\rho < 0.01$ ohm-cm) with a thick embedded silicon oxide layer have been developed using micromachining techniques. Lines with different lengths were designed, fabricated and measured. Measured attenuation and s-parameters are presented in the paper. Results show that the attenuation loss of the fabricated FGC lines is as low as 3.2 dB/cm at 40 GHz.

INTRODUCTION

Radio Frequency and Microwave Monolithic Integrated Circuits (RFICs and MMICs) fabricated on silicon substrates have obtained widespread use in personal communication, GPS, and other systems that are highly dependent on cost. The possibility of low cost RF and microwave circuits integrated with digital and analog circuits on the same chip is creating a strong interest in silicon as a microwave substrate. Their operation on CMOS grade Si, however, is degraded by the high loss of transmission lines and antennas. Transmission lines and passive circuit components fabricated directly on standard, low-resistivity silicon wafers, commonly used in commercial foundries, have high loss, or low Q-factors [1]. To overcome this problem researchers have used two different approaches. In the first approach, high resistivity Si (HRS) wafers are used ($\rho > 2500$ Ω -cm) [2]-[3] and traditional microwave components have a performance similar to those on dielectric substrates, such as GaAs. In the second approach, polyimide or BCB layers are used on top of the CMOS substrate to create an interface layer that can host low loss microwave components. Both microstrip and coplanar waveguide transmission lines fabricated in this way have exhibited low attenuation for an optimum polyimide thickness [4]-[5].

In the case of finite coplanar lines with an interface layer, the structure may be thought of as

a Metal-Insulator-Semiconductor (MIS) one that may support three modes of propagation (skin effect mode, a dielectric quasi-TEM mode, and a slow-wave mode). Prior work on MIS coplanar waveguides has explored this with the goal of developing slow wave structures for circuit size reduction [5-7]. However, the slow-wave structures were built on thin insulators deposited over a thin, highly doped semiconductor layer that is grown on an insulating material [7, 8]. Because the insulating layer is thin (less than 1 μ m), the fields interact strongly with the semiconductor layer and the attenuation is reported to be greater than 10 dB/cm [8, 9]. Thus, while interesting and useful for some purposes, the attenuation is too high for most Si RFICs. References [6] and [7] demonstrated the viability of using thick polyimide interface layers to reduce the dielectric loss of FGC lines and Coplanar Waveguides (CPW) on low resistivity silicon wafers.

In this paper, we present for the first time measured characteristics of FGC lines built on a CMOS grade silicon substrate ($\rho < 0.01$ Ω -cm) with an embedded thick silicon oxide layer using micromachining techniques. A schematic of the proposed structure can be seen in Figure 1. The oxide layer has a thickness of 50 microns and minimizes substantially the electromagnetic field interaction with the lossy Si substrate. The proposed technique is simple and low cost, and does not require the deposition and post-

processing of several layers as in the case of BCB or polyimide.

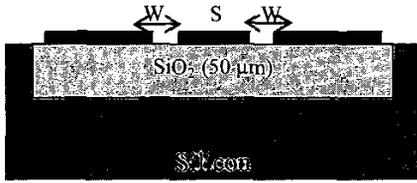


Figure 1: Cross-sectional view of the Finite Ground Coplanar (FGC) waveguide fabricated on thick oxide islands inside the silicon substrate.

CIRCUIT FABRICATION AND CHARACTERIZATION

The resistivity of silicon substrates was first measured with a four-point probe and determined to be 0.0057 Ω-cm. The fifty microns thick silicon dioxide islands were embedded in the silicon substrate by etching deep trenches in selected areas of the silicon substrate (using the Bosch process) and subsequently oxidizing the silicon left in between the trenches. This process was then augmented by a LPCVD oxide deposition in order to fill any empty space between the oxidized slabs and create a solid piece of thick SiO₂ island. Figure 2 is an SEM picture of the cross section of such an oxide island (~50μm thick), showing the excellent quality of the oxide and very small surface roughness (<0.5μm).



Figure 2: Cross section of 50μm thick silicon dioxide embedded in low resistivity silicon substrate.

Once the oxide islands were created the coplanar waveguide transmission lines were patterned and Au electroplated to a thickness of 3 μm (Figure 3). Measurements were taken using an Agilent 8510 network analyzer and a probe station. The GGB SOLT calibration was implemented. To improve the accuracy, each circuit was measured several times. The dimensions of the different lines are

summarized in Table 1. Full wave simulations were also performed using *Sonnet* for the fabricated transmission lines and results yielded a characteristic impedance of 85 Ω and an effective dielectric constant of 2.35. The latter value indicates that most of the electromagnetic field is contained in the thick oxide layer.

Table 1: Dimensions of FGC lines

S (μm)	W (μm)	Length of the line (μm)
42	24	5000
42	24	4000
42	24	2500

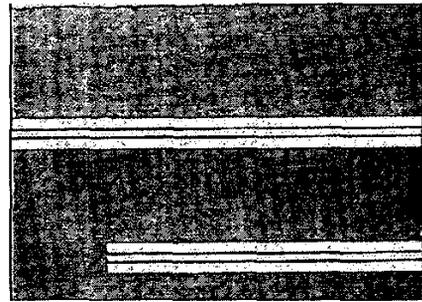


Figure 3: Photo of the fabricated FGC lines.

RESULTS

The measured s-parameters of the three FGC lines fabricated on CMOS grade silicon with embedded silicon oxide are shown in Figure 4. It is seen that the maximum return loss for all lines is around 6 dB. The maximum insertion loss comes from the longest line as expected, and it is around 2.75 dB at 27.5GHz. Based on the s-parameter measurements of all three lines, the attenuation for the transmission line with s=42 μm and w=24 μm was extracted.

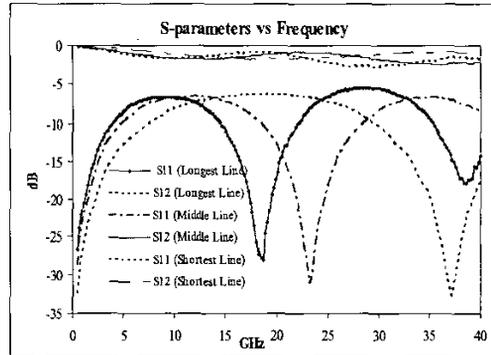


Figure 4: Measured S-parameters of FGC lines on silicon oxide islands with silicon substrates.

The measured attenuation for the FGC lines is shown in Figure 5. The average value of the three lines is plotted. As it is shown, the attenuation is only 3.2 dB/cm at 40 GHz and 1.8 dB at 20 GHz.

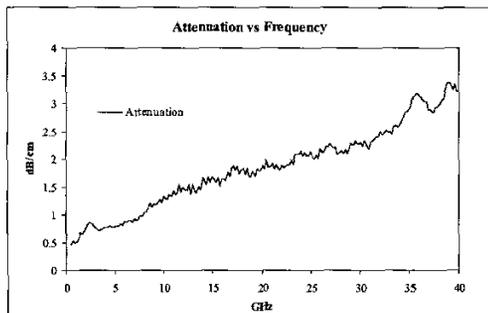


Figure 5: Measured attenuation of FGC lines on CMOS grade Si ($\rho=0.0057 \Omega\text{-cm}$) with embedded thick SiO_2 island.

CONCLUSIONS

Measured s-parameters and attenuation of FGC lines on CMOS grade silicon with embedded thick silicon oxide using micromachining techniques are presented for the first time. Results indicate that the line attenuation for a wafer with very low resistivity using this technique is as low as 3.2 dB/cm at 40 GHz. The proposed micromachining technique is, thus, an excellent candidate for the fabrication of several microwave components on CMOS grade Si substrates. More results will be presented at the conference, including measurements for the effective dielectric constant.

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