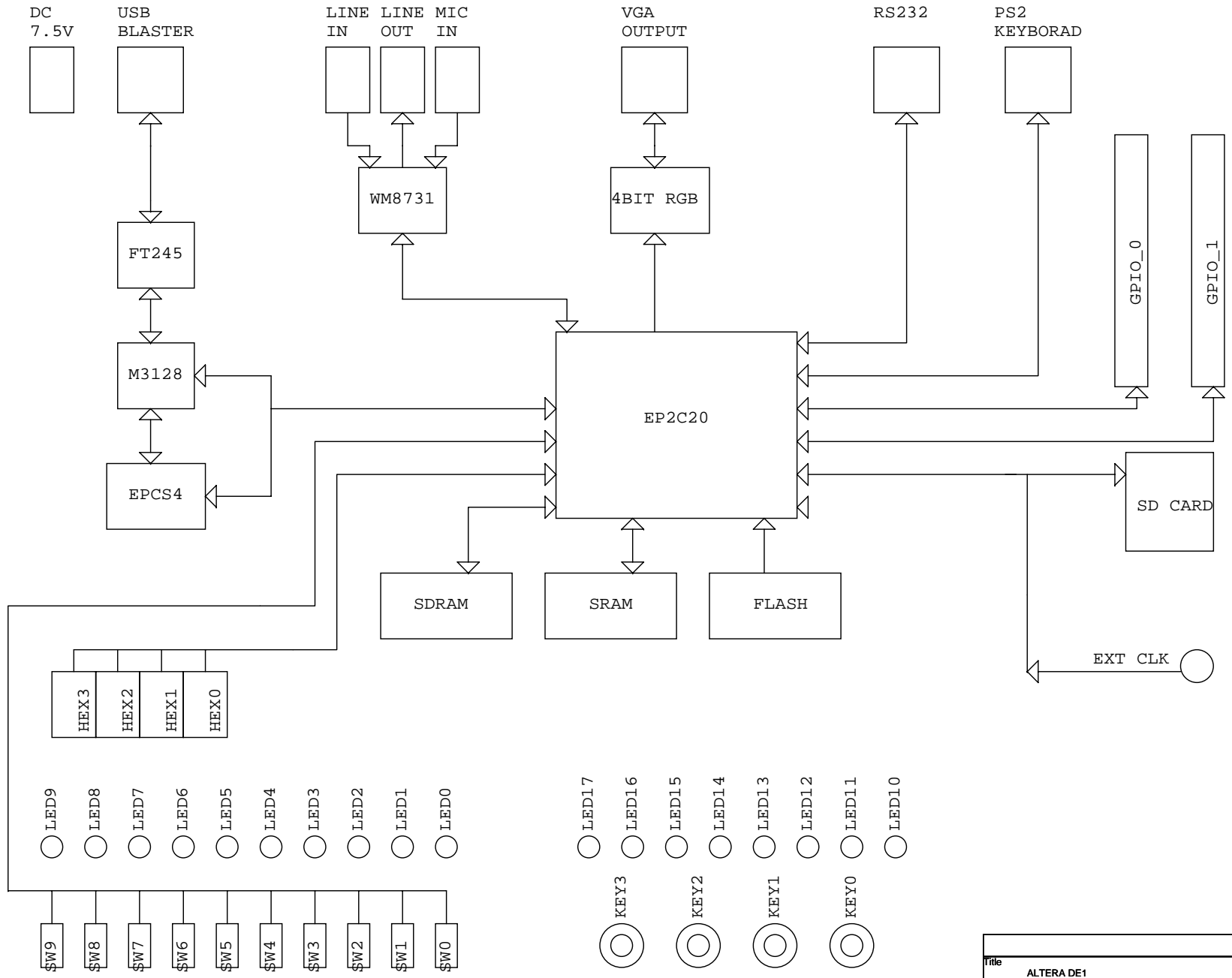
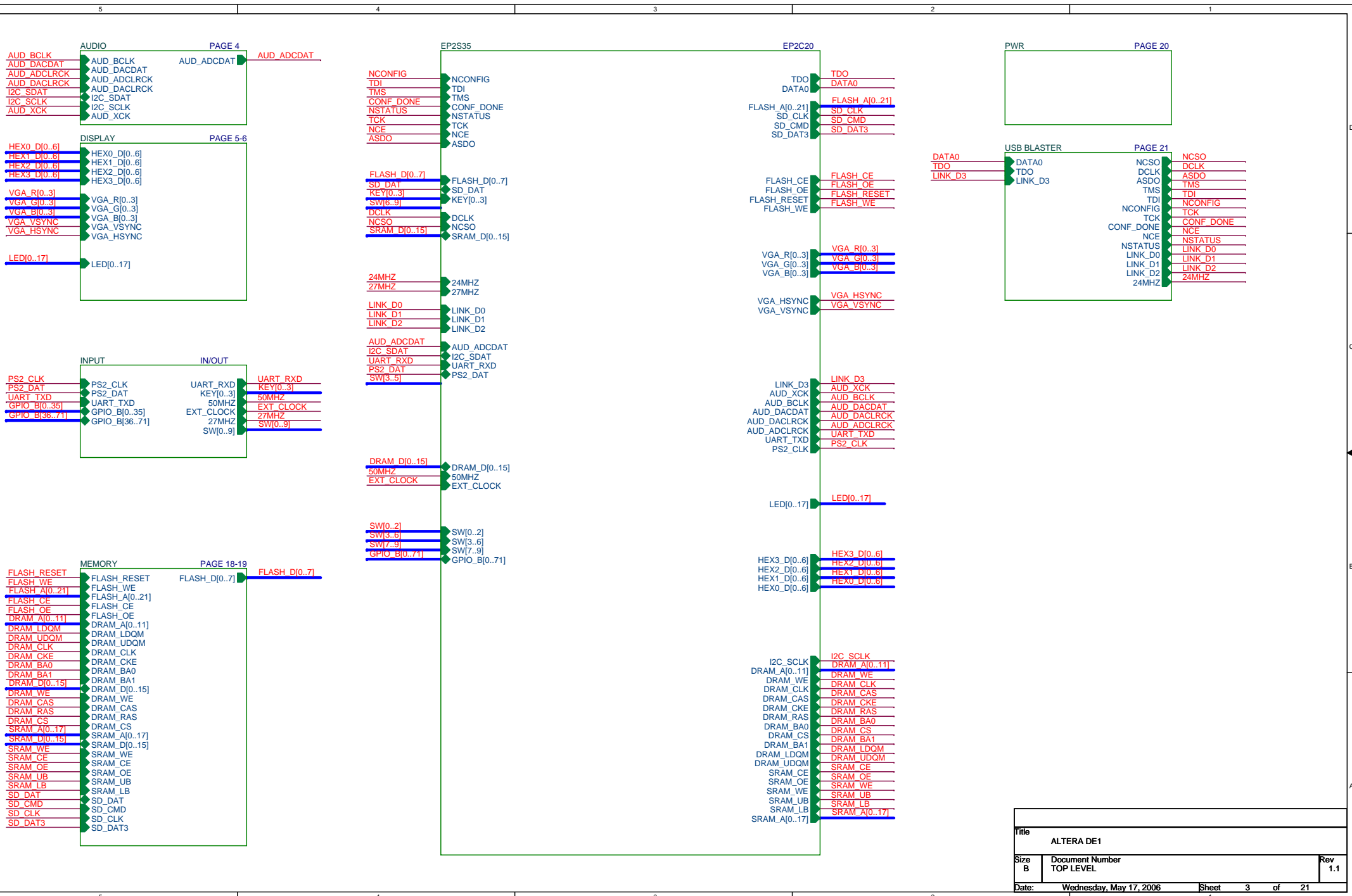


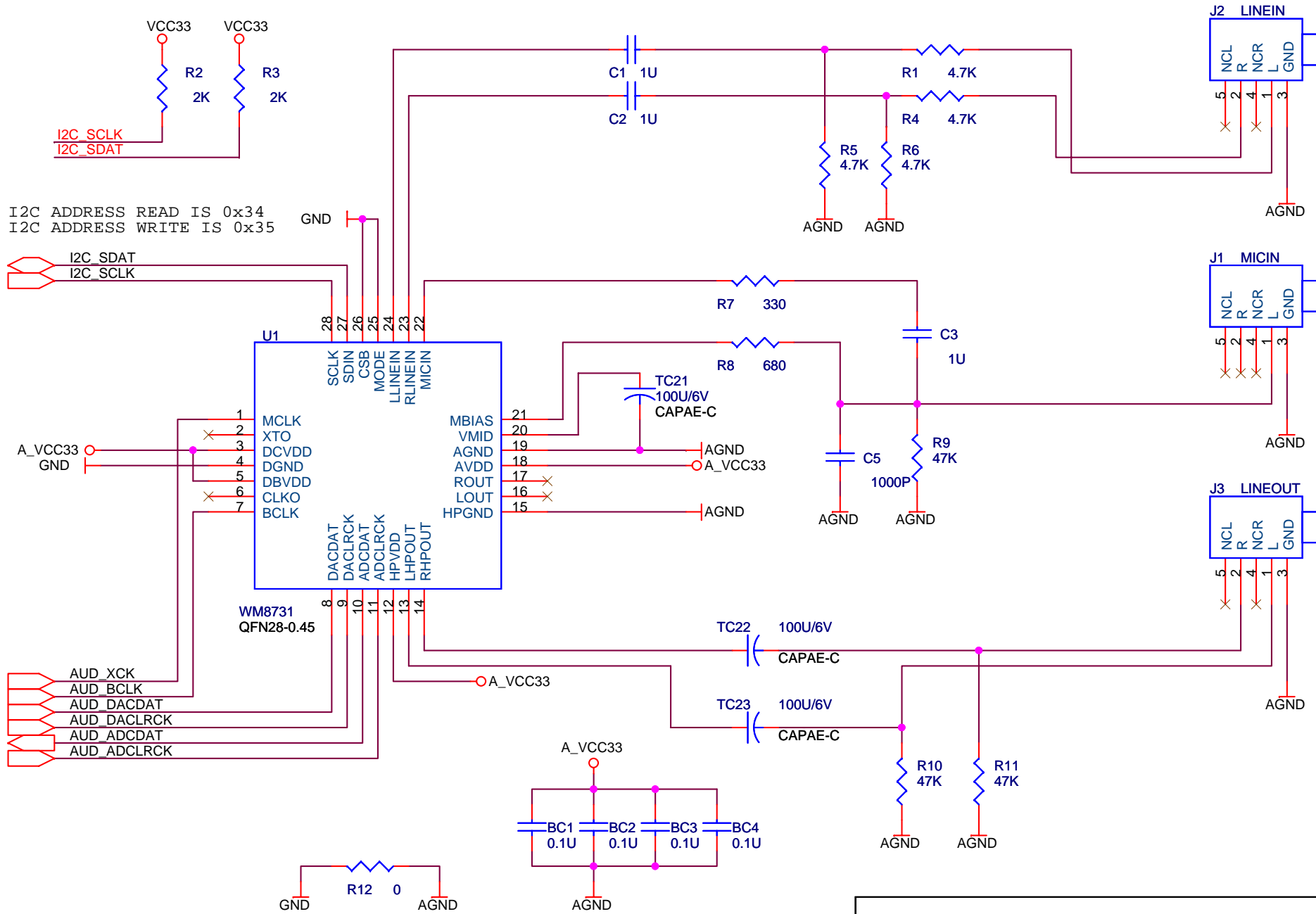
TERASIC CYCLONE II EP2C20 DAUGHTER BOARD

SCHEMATIC	CONTENT	PAGE
TOP	COVER PAGE , TOP	01 ~ 03
AUDIO	WM8731	04 ~ 04
DISPLAY	VGA , 7SEGMENT ,LED	05 ~ 07
EP2C20	EP2C20 BANK1..BANK8 , POWER , CONFIG	08 ~ 12
INPUT	CLOCK , PS2 , RS232 , KEY , SWITCH , CONNECT	13 ~ 17
MEMORY	SRAM , DRAM , FLASH , SD CARD	18 ~ 19
POWER	POWER	20 ~ 20
BLASTER	USB BLASTER	21 ~ 21





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B	TOP LEVEL			1.1	
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I2C ADDRESS READ IS 0x34
 I2C ADDRESS WRITE IS 0x35

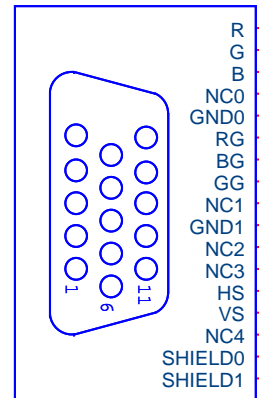
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 I2C_SCLK

A_VCC33
 GND

AUD_XCK
 AUD_BCLK
 AUD_DACDAT
 AUD_DACLK
 AUD_ADCLK

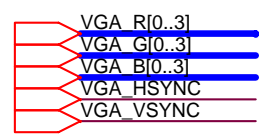
Title		
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A	AUDIO	1.1
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DB15-RA-F2
VGA



J4

GND



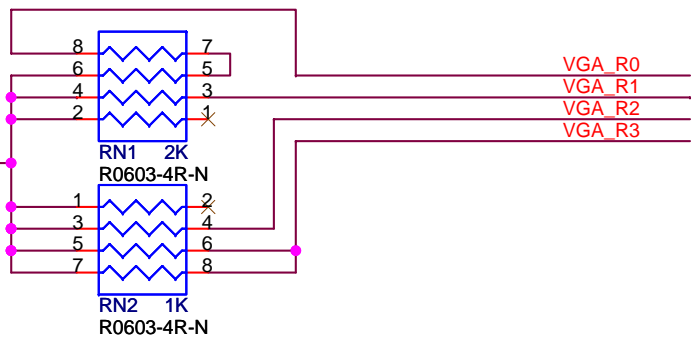
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G

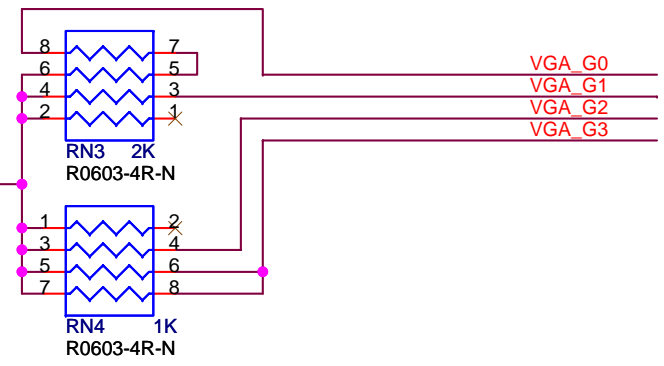
B

H

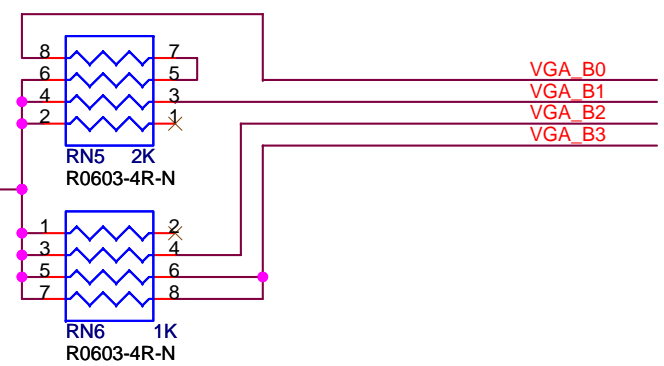
V



VGA_R0
VGA_R1
VGA_R2
VGA_R3



VGA_G0
VGA_G1
VGA_G2
VGA_G3



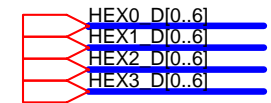
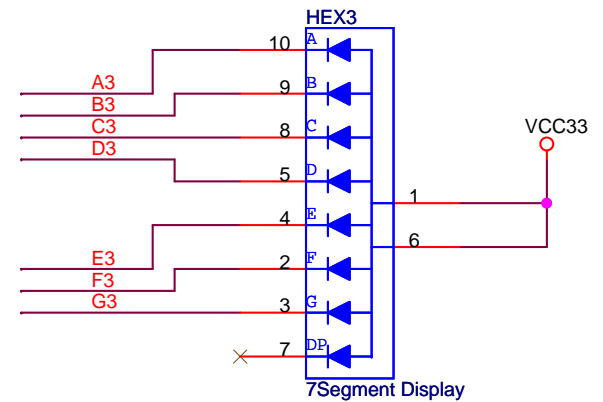
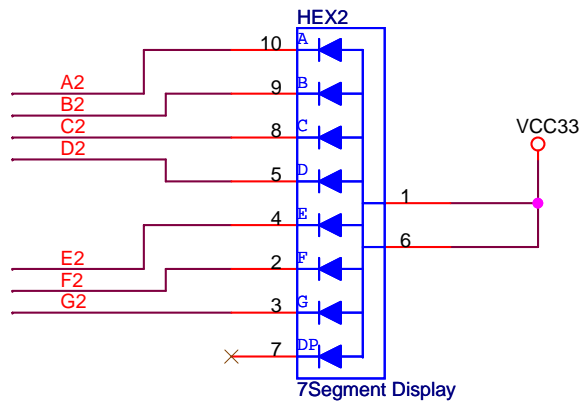
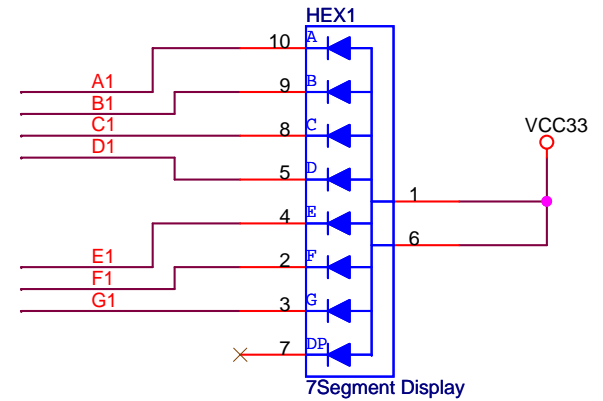
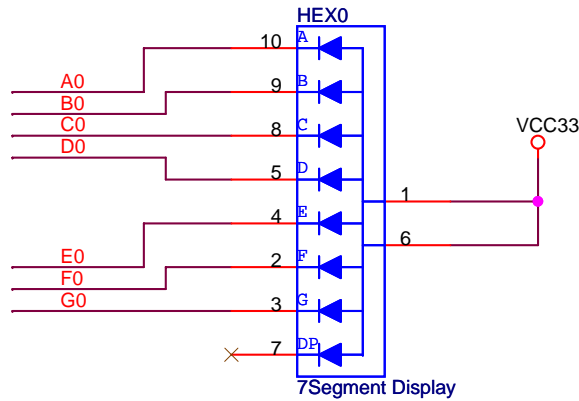
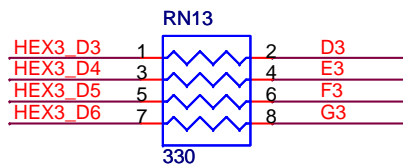
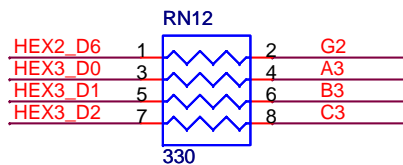
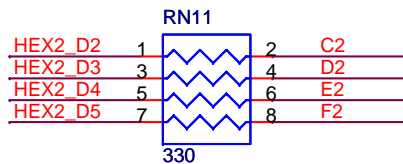
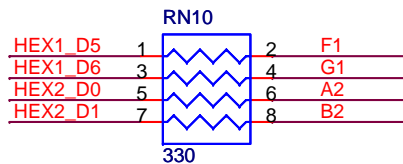
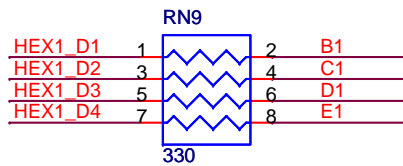
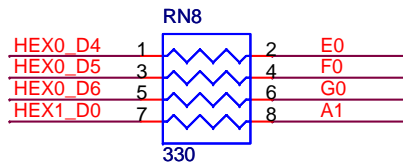
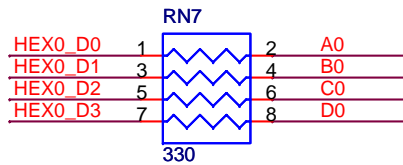
VGA_B0
VGA_B1
VGA_B2
VGA_B3

R-0603
R13 120

R14 120
R-0603

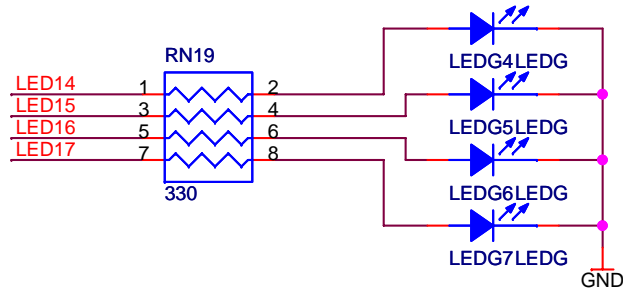
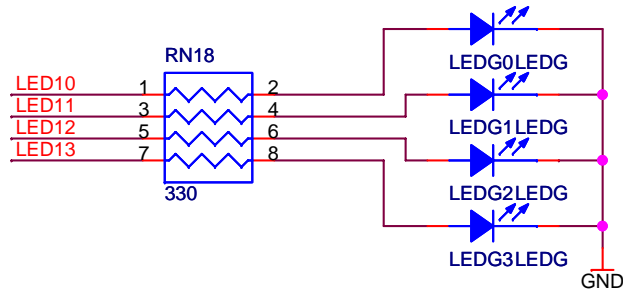
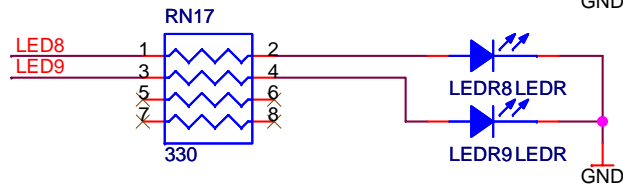
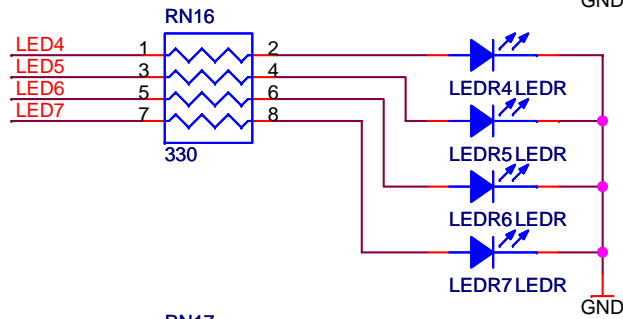
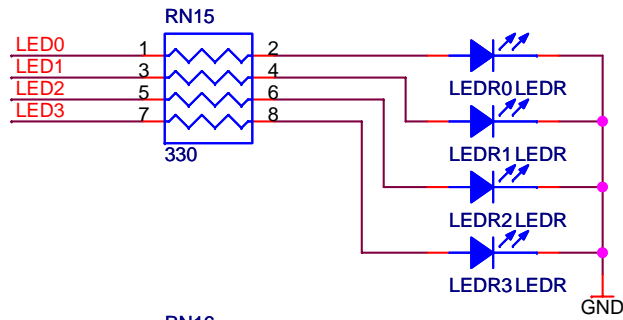
VGA_HSYNC
VGA_VSYNC

Title		
ALTERA DE1		
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A	VGA	1.1
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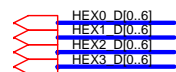
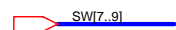
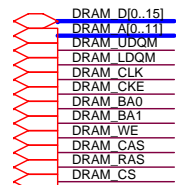


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A	7 SEGMENT	1.1
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LED[0..17]



Title		
ALTERA DE1		
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A	LED	1.1
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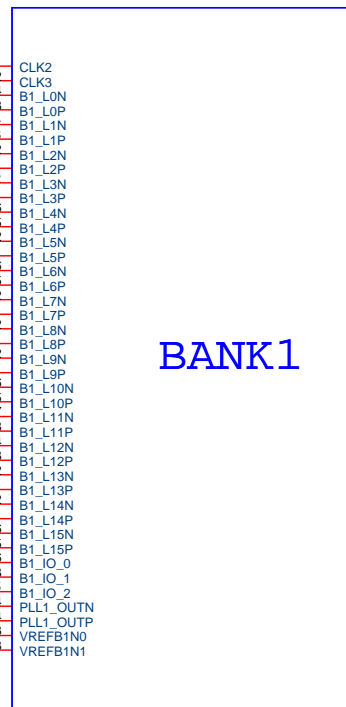


SW8	M1
SW7	M2
DRAM A0	W4
DRAM A1	W5
DRAM A2	Y3
DRAM A3	Y4
DRAM A4	R6
DRAM A5	R5
DRAM A6	P6
DRAM A7	P5
DRAM A8	P3
DRAM A9	N4
DRAM A10	W3
DRAM A11	N6
DRAM D0	U1
DRAM D1	U2
DRAM D2	V1
DRAM D3	V2
DRAM D4	W1
DRAM D5	W2
DRAM D6	Y1
DRAM D7	Y2
DRAM D8	N1
DRAM D9	N2
DRAM D10	P1
DRAM D11	P2
DRAM D12	R1
DRAM D13	R2
DRAM D14	T1
DRAM D15	T2
DRAM BA0	U3
DRAM BA1	V4
DRAM LDQM	R7
DRAM UDQM	M5
DRAM CAS	T3
DRAM RAS	T5
DRAM WE	R8
DRAM CS	T6
DRAM CLK	U4
DRAM CKE	N3

50MHZ	L1
SW9	L2
HEX0 D0	J2
HEX0 D1	J1
HEX0 D2	H2
HEX0 D3	H1
HEX0 D4	F2
HEX0 D5	F1
HEX0 D6	E2
HEX1 D0	E1
HEX1 D1	H6
HEX1 D2	H5
HEX1 D3	H4
HEX1 D4	G3
HEX1 D5	D2
HEX1 D6	D1
HEX2 D0	G5
HEX2 D1	G6
HEX2 D2	C2
HEX2 D3	C1
HEX2 D4	E3
HEX2 D5	E4
HEX2 D6	D3
HEX3 D0	F4
HEX3 D1	D5
HEX3 D2	D6
HEX3 D3	J4
HEX3 D4	L8
HEX3 D5	F3
HEX3 D6	D4

M1	M1	CLK2
M2	M2	CLK3
Y4	Y4	B1_L0N
Y3	Y3	B1_L0P
W4	W4	B1_L1N
W3	W3	B1_L1P
Y2	Y2	B1_L2N
Y1	Y1	B1_L2P
W2	W2	B1_L3N
W1	W1	B1_L3P
T6	T6	B1_L4N
T5	T5	B1_L4P
V2	V2	B1_L5N
V1	V1	B1_L5P
R6	R6	B1_L6N
R5	R5	B1_L6P
U2	U2	B1_L7N
U1	U1	B1_L7P
T2	T2	B1_L8N
T1	T1	B1_L8P
R2	R2	B1_L9N
R1	R1	B1_L9P
P6	P6	B1_L10N
P5	P5	B1_L10P
R7	R7	B1_L11N
R8	R8	B1_L11P
N4	N4	B1_L12N
N3	N3	B1_L12P
P2	P2	B1_L13N
P1	P1	B1_L13P
N2	N2	B1_L14N
N1	N1	B1_L14P
M6	M6	B1_L15N
M5	M5	B1_L15P
N6	N6	B1_IO_0
T3	T3	B1_IO_1
W5	W5	B1_IO_2
V4	V4	PLL1_OUTN
U4	U4	PLL1_OUTP
P3	P3	VREFB1N0
U3	U3	VREFB1N1

U2A



BANK1

CYCLONE II EP2C20

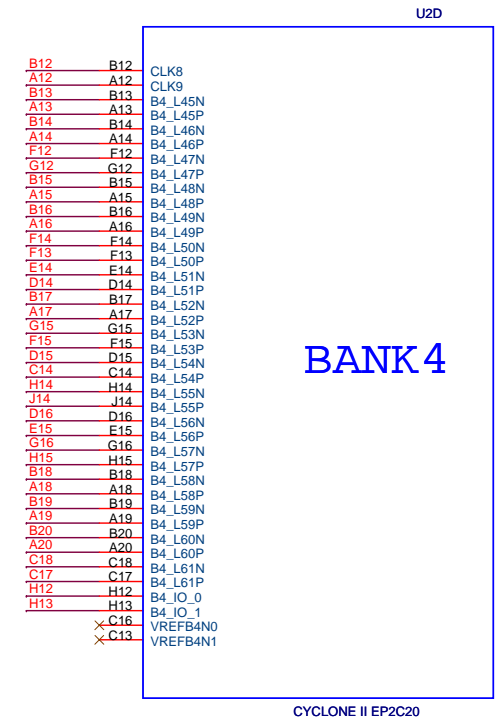
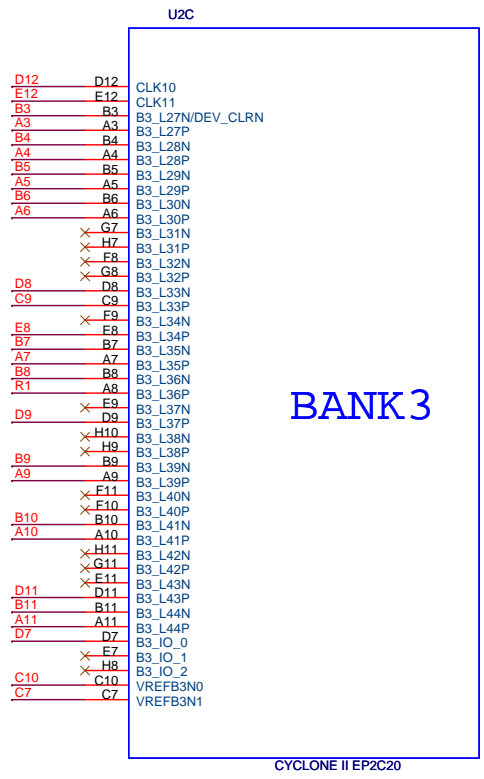
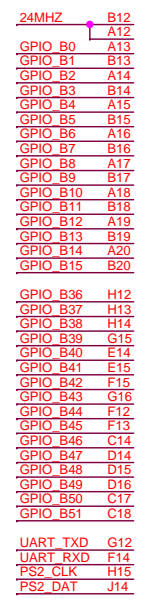
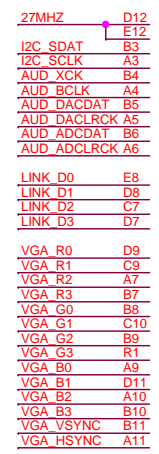
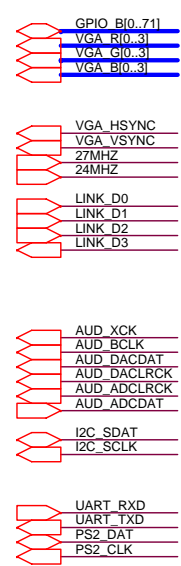
U2B

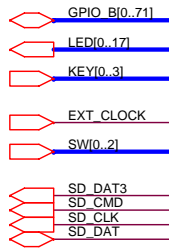
L1	L1	CLK0
L2	L2	CLK1
J2	J2	B2_L16N
J1	J1	B2_L16P
H2	H2	B2_L17N
H1	H1	B2_L17P
F2	F2	B2_L18N
F1	F1	B2_L18P
E2	E2	B2_L19N
E1	E1	B2_L19P
H6	H6	B2_L20N
H5	H5	B2_L20P
H4	H4	B2_L21N
G3	G3	B2_L21P
D2	D2	B2_L22N
D1	D1	B2_L22P
G5	G5	B2_L23N
G6	G6	B2_L23P
C2	C2	B2_L24N
C1	C1	B2_L24P
E4	E4	B2_L25N
E3	E3	B2_L25P
D4	D4	B2_L26N
D3	D3	B2_L26P
F3	F3	B2_IO_0
J4	J4	B2_IO_1
L8	L8	B2_IO_2
D6	D6	PLL3_OUTN
D5	D5	PLL3_OUTP
F4	F4	VREFB2N0
H3	H3	VREFB2N1

BANK 2

CYCLONE II EP2C20

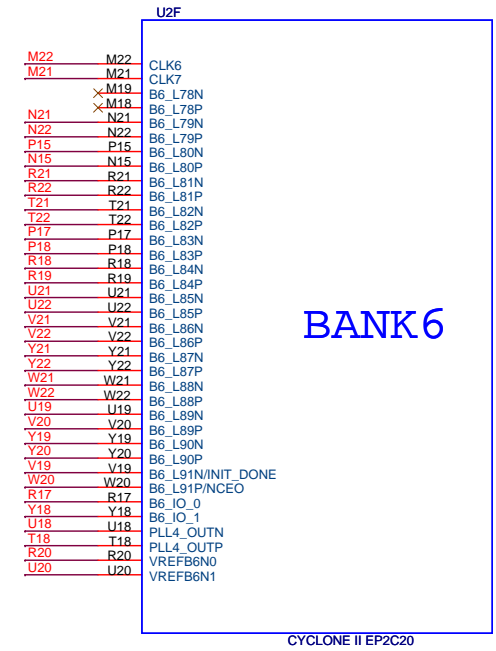
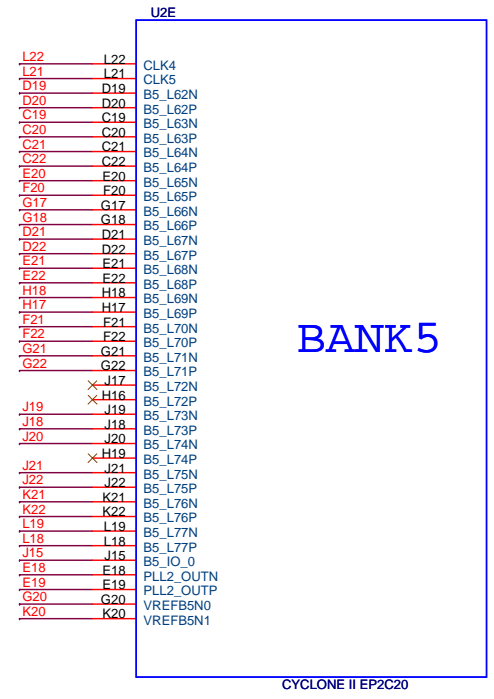
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B	EP2C20 BANK1 AND BANK 2	1.1
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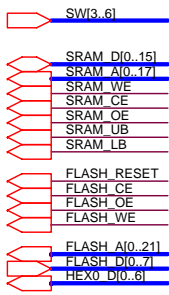


SW0	L22
SW1	L21
GPIO B16	C21
GPIO B17	C22
GPIO B18	D21
GPIO B19	D22
GPIO B20	E21
GPIO B21	E22
GPIO B22	F21
GPIO B23	F22
GPIO B24	G21
GPIO B25	G22
GPIO B26	J21
GPIO B27	J22
GPIO B28	K21
GPIO B29	K22
GPIO B30	J19
GPIO B31	J20
GPIO B32	J18
GPIO B33	K20
GPIO B34	L19
GPIO B35	L18
GPIO B52	C19
GPIO B53	C20
GPIO B54	D19
GPIO B55	D20
GPIO B56	E20
GPIO B57	F20
GPIO B58	E19
GPIO B59	E18
GPIO B60	G20
GPIO B61	G18
GPIO B62	G17
GPIO B63	H17
GPIO B64	J15
GPIO B65	H18
GPIO B66	N22
GPIO B67	N21
GPIO B68	P15
GPIO B69	N15
GPIO B70	P17
GPIO B71	P18

SW2	M22
EXT_CLOCK	M21
KEY0	R22
KEY1	R21
KEY2	T22
KEY3	T21
SD_CLK	V20
SD_CMD	Y20
SD_DAT	W20
SD_DAT3	U20
LED0	R20
LED1	R19
LED2	U19
LED3	Y19
LED4	T18
LED5	V19
LED6	Y18
LED7	U18
LED8	R18
LED9	R17
LED10	U22
LED11	U21
LED12	V22
LED13	V21
LED14	W22
LED15	W21
LED16	Y22
LED17	Y21



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B	EP2C20 BANKS AND BANK 6	1.1
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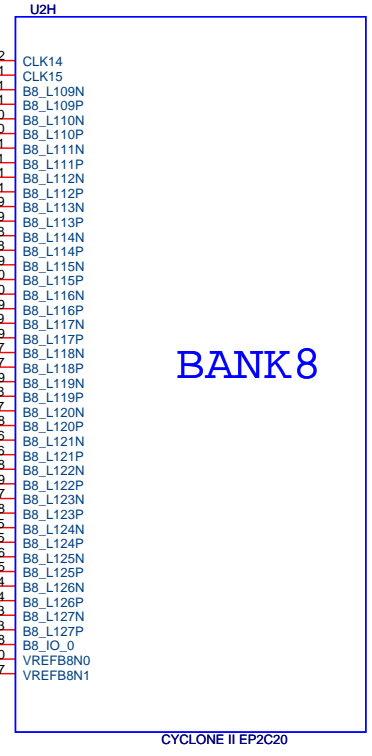
SW3	V12
SW4	W12
FLASH A0	AB20
FLASH A1	AA14
FLASH A2	Y16
FLASH A3	R15
FLASH A4	T15
FLASH A5	U15
FLASH A6	V15
FLASH A7	W15
FLASH A8	R14
FLASH A9	Y13
FLASH A10	R12
FLASH A11	T12
FLASH A12	AB14
FLASH A13	AA13
FLASH A14	AB13
FLASH A15	AA12
FLASH A16	AB12
FLASH A17	AA20
FLASH A18	U14
FLASH A19	V14
FLASH A20	U13
FLASH A21	R13
FLASH D0	AB16
FLASH D1	AA16
FLASH D2	AB17
FLASH D3	AA17
FLASH D4	AB19
FLASH D5	AA18
FLASH D6	AB19
FLASH D7	AA19
FLASH WE	Y14
FLASH OE	AA15
FLASH CE	AB15
FLASH RESET	W14

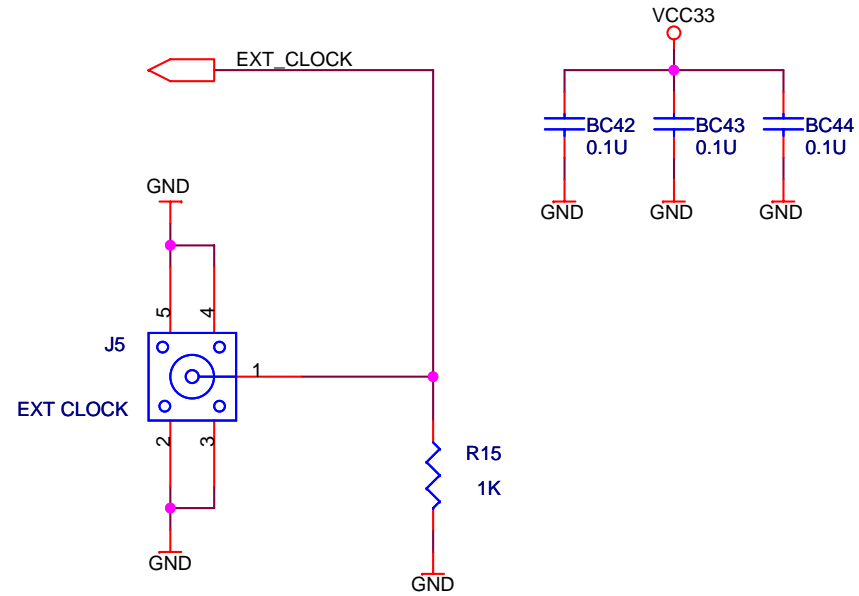
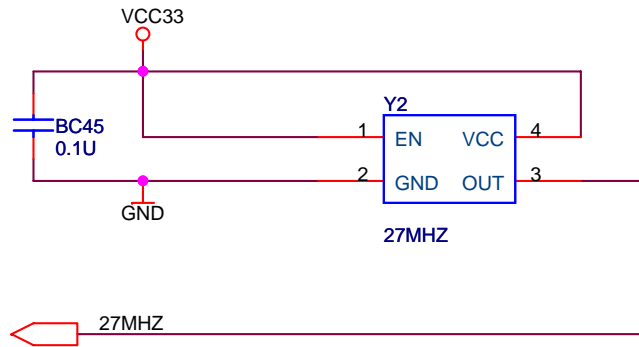
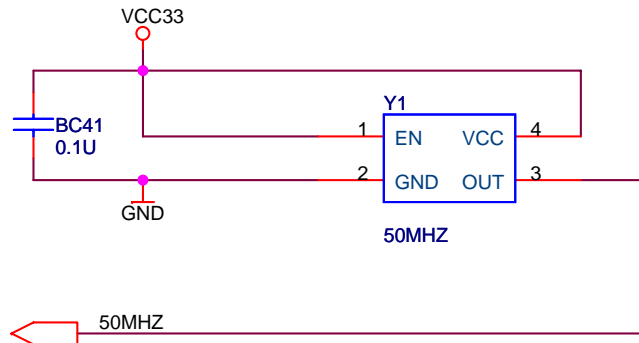
SW5	U12
SW6	U11
SRAM A0	AA3
SRAM A1	AB3
SRAM A2	AA4
SRAM A3	AB4
SRAM A4	AA5
SRAM A5	AB10
SRAM A6	AA11
SRAM A7	AB11
SRAM A8	V11
SRAM A9	W11
SRAM A10	R11
SRAM A11	T11
SRAM A12	Y10
SRAM A13	U10
SRAM A14	R10
SRAM A15	T7
SRAM A16	Y6
SRAM A17	Y5
SRAM D0	AA6
SRAM D1	AB6
SRAM D2	AA7
SRAM D3	AB7
SRAM D4	AA8
SRAM D5	AB8
SRAM D6	AA9
SRAM D7	AB9
SRAM D8	Y9
SRAM D9	W9
SRAM D10	V9
SRAM D11	U9
SRAM D12	R9
SRAM D13	W8
SRAM D14	V8
SRAM D15	U8
SRAM LB	Y7
SRAM UB	W7
SRAM WE	AA10
SRAM OE	T8
SRAM CE	AB5

V12	V12	CLK12
W12	W12	CLK13
AA20	AA20	B7_L92N
AB20	AB20	B7_L92P
AA19	AA19	B7_L93N
AB19	AB19	B7_L93P
	XW16	B7_L94N
	XW17	B7_L94P
V15	XV15	B7_L95N
U15	U15	B7_L95P
	XR16	B7_L96P
	XR16	B7_L97N
AA18	AA18	B7_L97P
AB18	AB18	B7_L98N
R15	R15	B7_L98P
R14	R14	B7_L99N
W15	W15	B7_L99P
Y14	Y14	B7_L100N
T15	T15	B7_L100P
U14	U14	B7_L101N
AA17	AA17	B7_L101P
AB17	AB17	B7_L102N
V14	V14	B7_L102P
W14	W14	B7_L103N
AA16	AA16	B7_L103P
AB16	AB16	B7_L104N
AA15	AA15	B7_L104P
AB15	AB15	B7_L105N
AA14	AA14	B7_L105P
AB14	AB14	B7_L106N
U13	U13	B7_L106P
T12	T12	B7_L107N
AA13	AA13	B7_L107P
AB13	AB13	B7_L108N
AA12	AA12	B7_L108P
AB12	AB12	B7_L109P
R12	R12	B7_IO_0
R13	R13	B7_IO_1
Y16	Y16	VREFB7N0
Y13	Y13	VREFB7N1

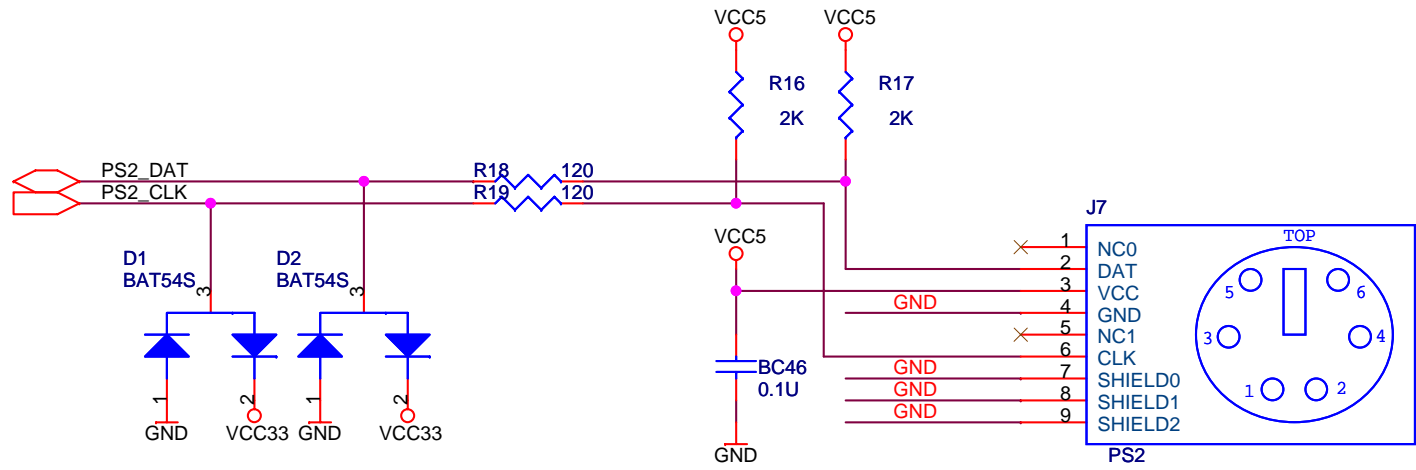
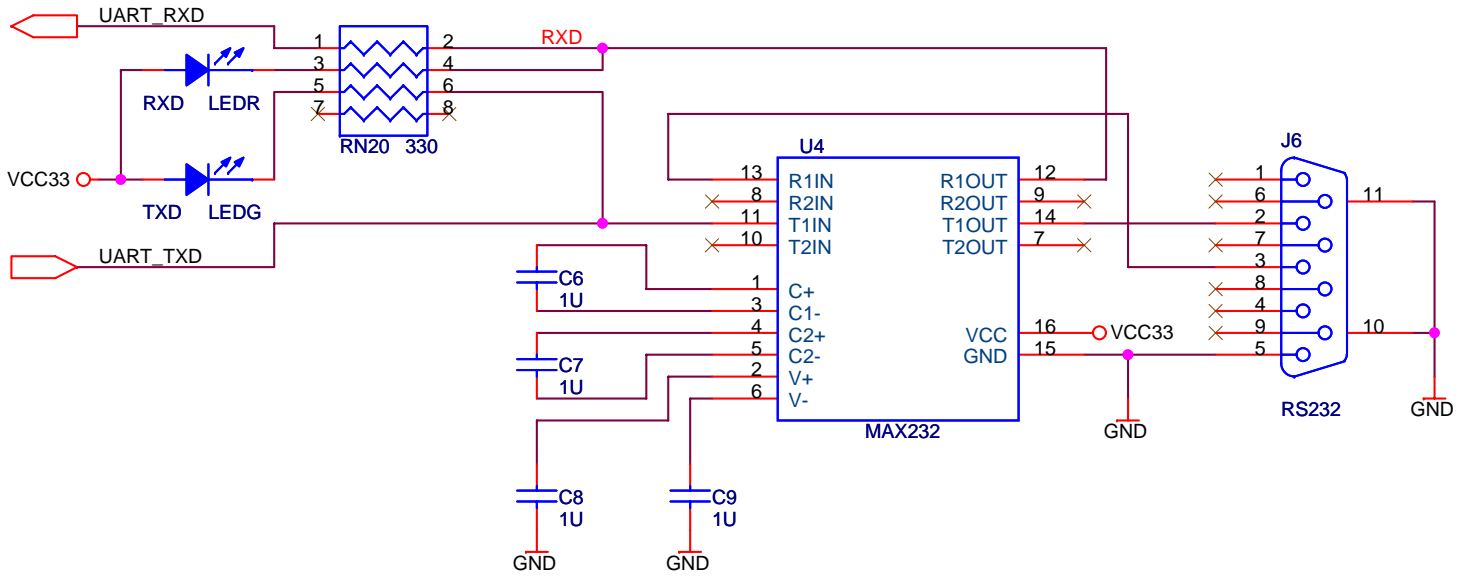


U12	U12	CLK14
U11	U11	CLK15
AA11	AA11	B8_L109N
AB11	AB11	B8_L109P
AA10	AA10	B8_L110N
AB10	AB10	B8_L110P
V11	V11	B8_L111N
W11	W11	B8_L111P
R11	R11	B8_L112N
T11	T11	B8_L112P
AA9	AA9	B8_L113N
AB9	AB9	B8_L113P
AA8	AA8	B8_L114N
AB8	AB8	B8_L114P
R9	R9	B8_L115N
R10	R10	B8_L115P
U10	U10	B8_L116N
U9	U9	B8_L116P
W9	W9	B8_L117N
Y9	Y9	B8_L117P
AA7	AA7	B8_L118N
AB7	AB7	B8_L118P
V9	V9	B8_L119N
W8	W8	B8_L119P
W7	W7	B8_L120N
V8	V8	B8_L120P
AA6	AA6	B8_L121N
AB6	AB6	B8_L121P
	XP8	B8_L122N
	XP9	B8_L122P
T7	T7	B8_L123N
T8	T8	B8_L123P
AA5	AA5	B8_L124N
AB5	AB5	B8_L124P
Y6	Y6	B8_L125N
Y5	Y5	B8_L125P
AA4	AA4	B8_L126N
AB4	AB4	B8_L126P
AA3	AA3	B8_L127N
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U8	U8	B8_IO_0
Y10	Y10	VREFB8N0
Y7	Y7	VREFB8N1

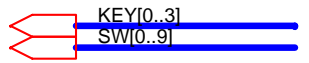
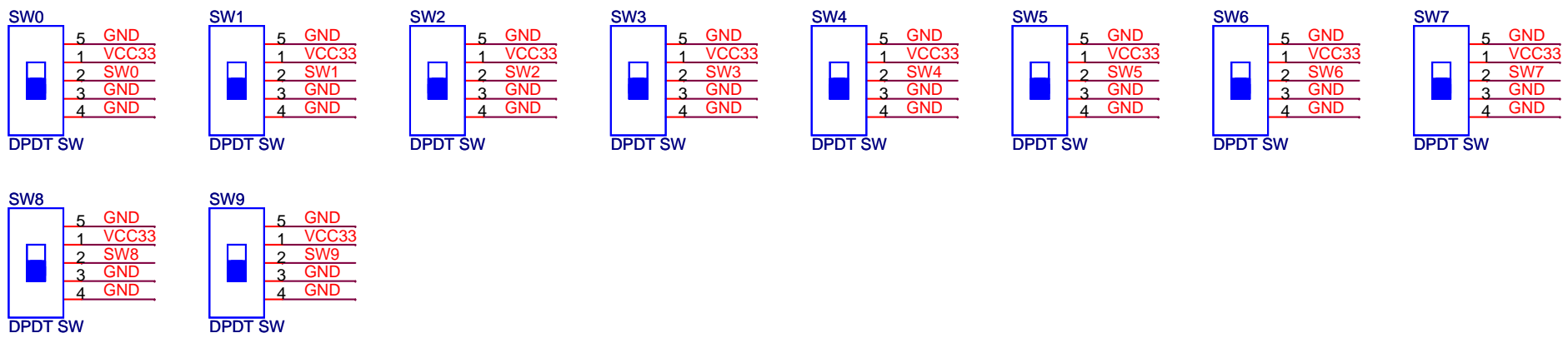
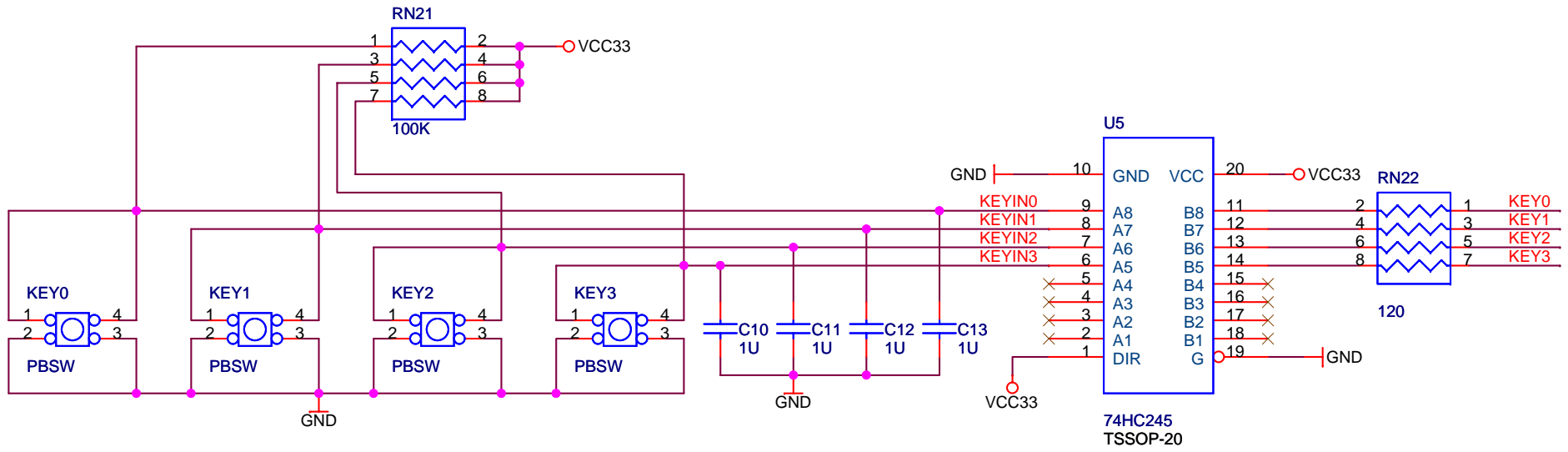




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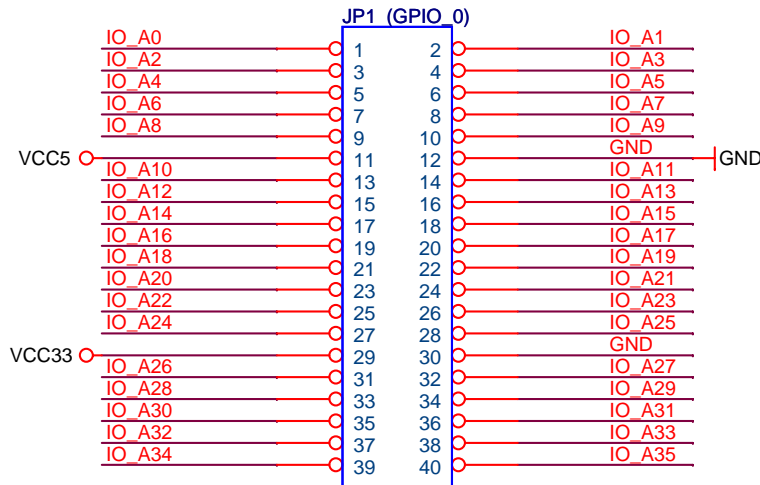
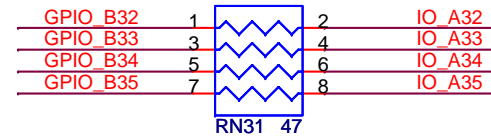
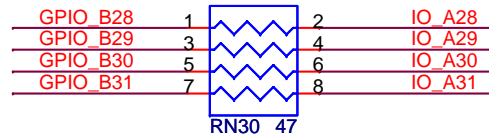
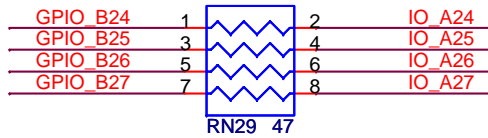
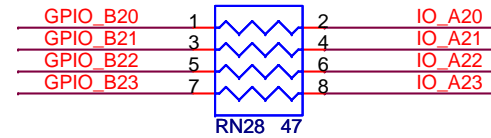
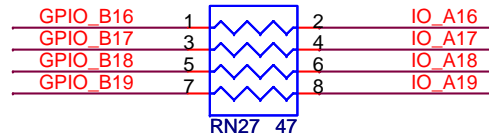
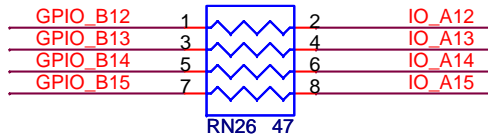
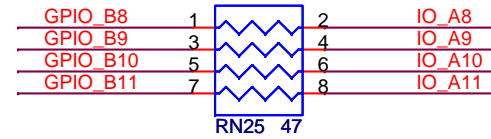
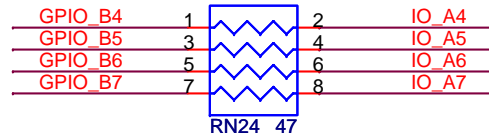
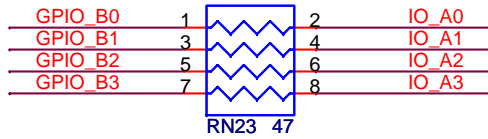


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A	PS2 AND RS232	1.1
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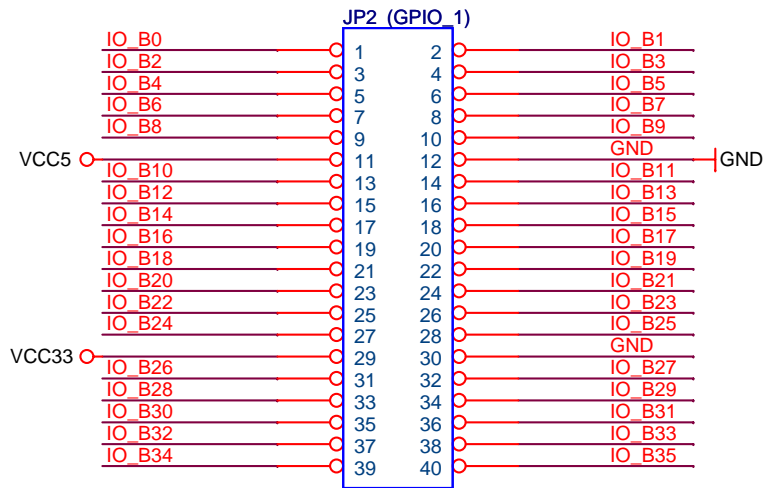
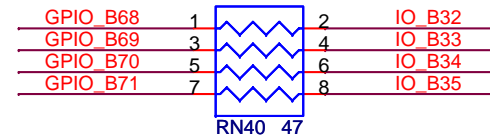
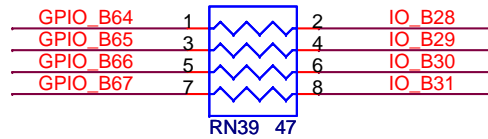
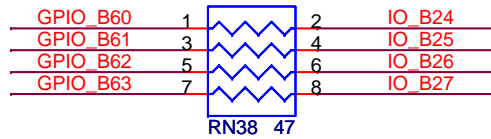
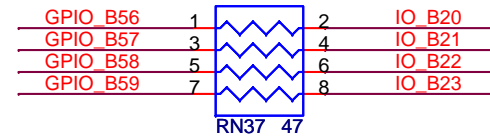
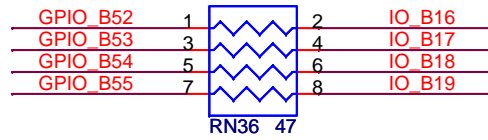
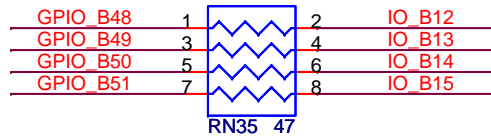
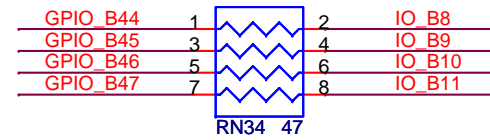
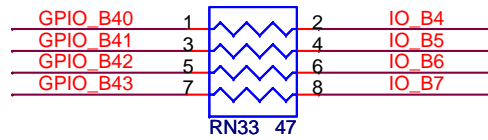
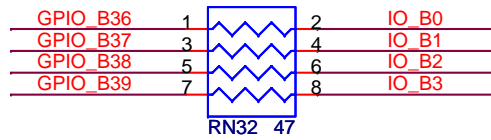
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A	KEY AND SWITCH	1.1
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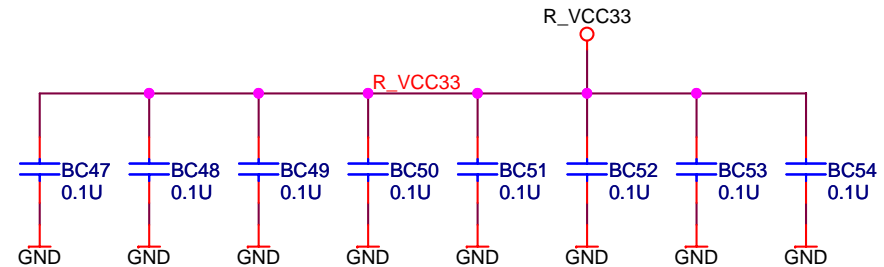
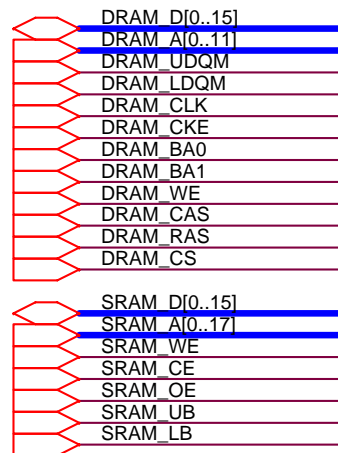
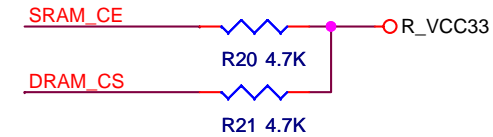
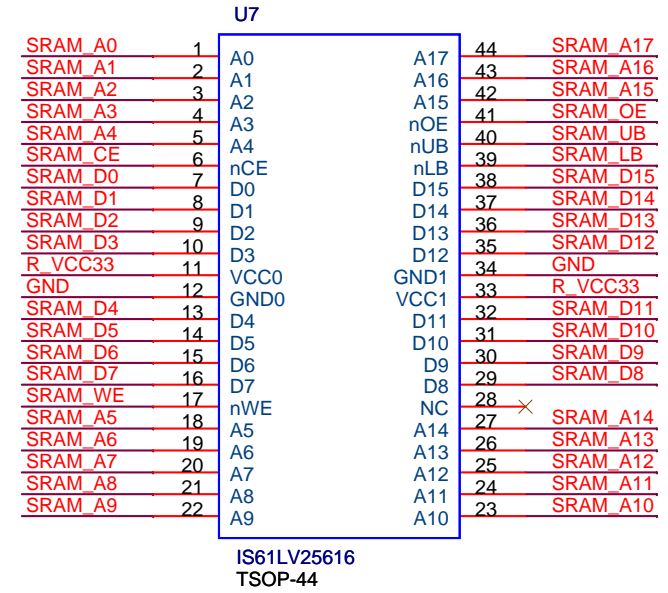
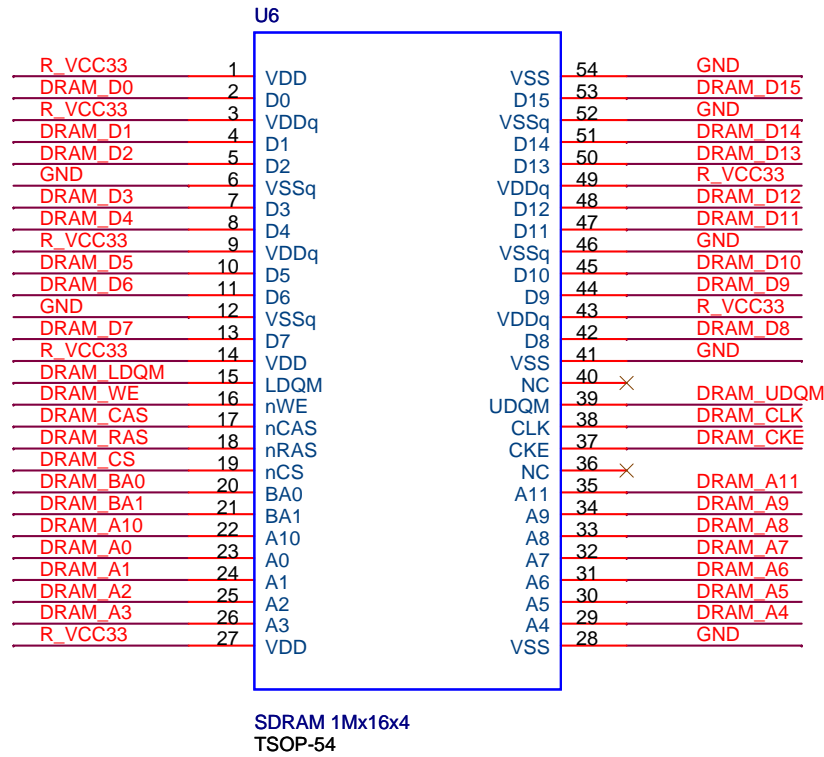


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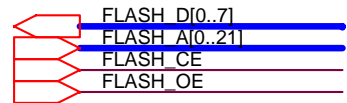
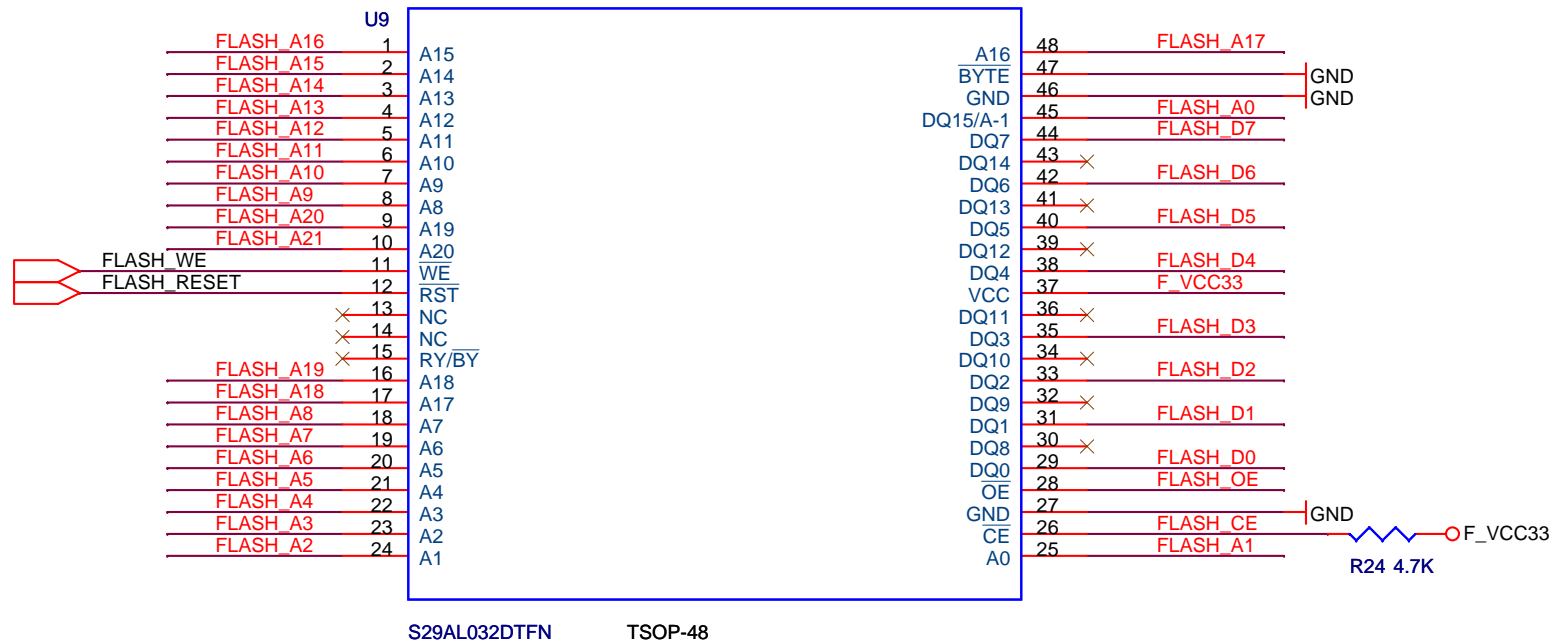
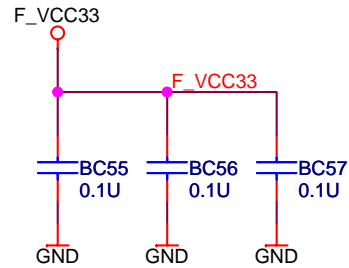
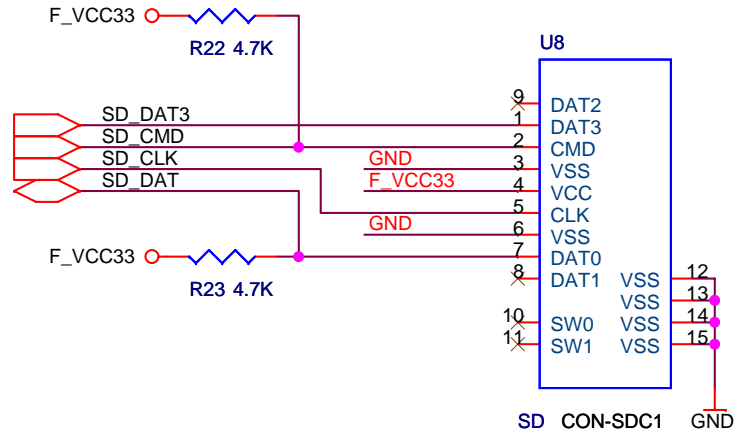
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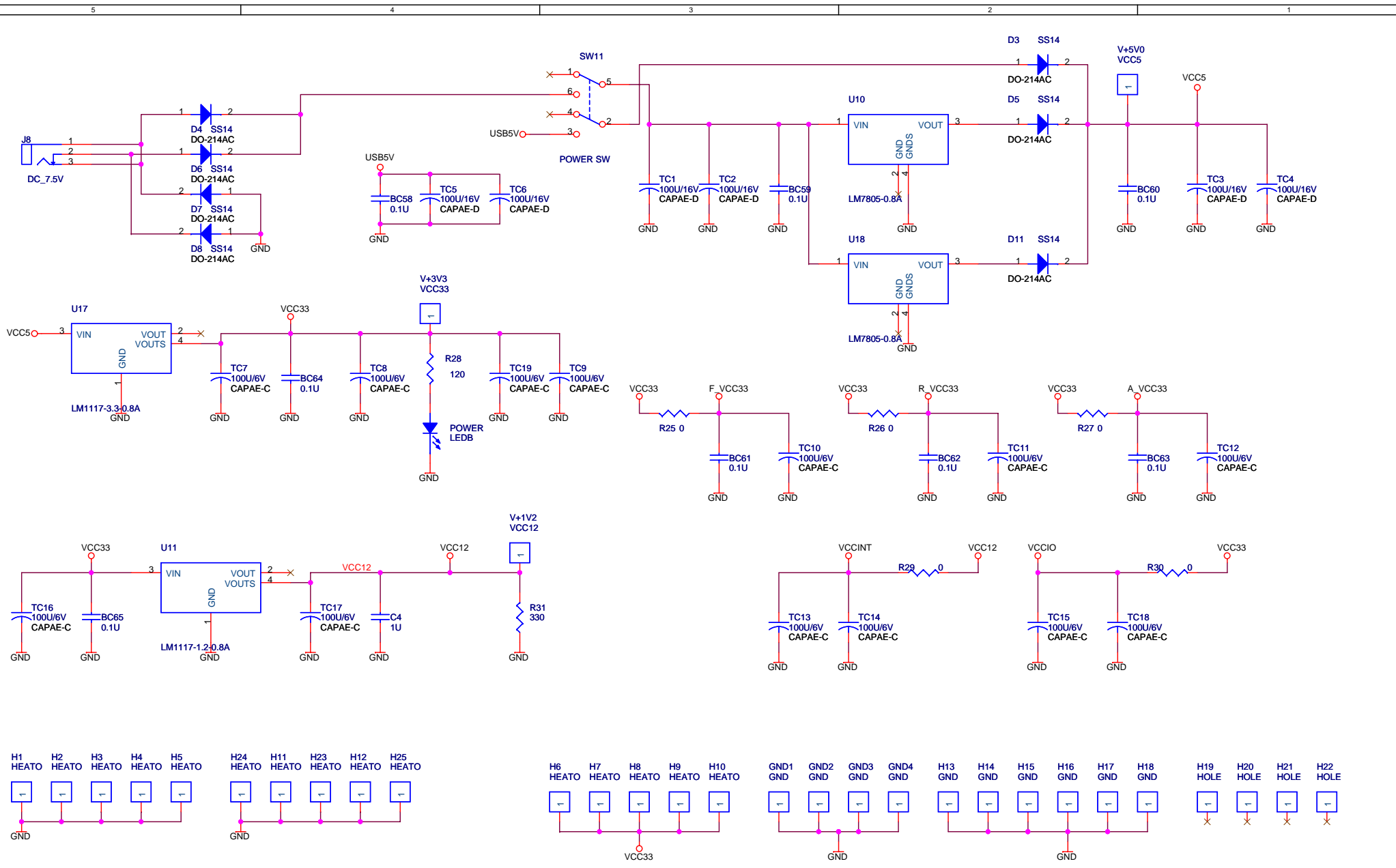
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B	POWER	1.1
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