

Figure 2.1 The Altera UP 3 board.

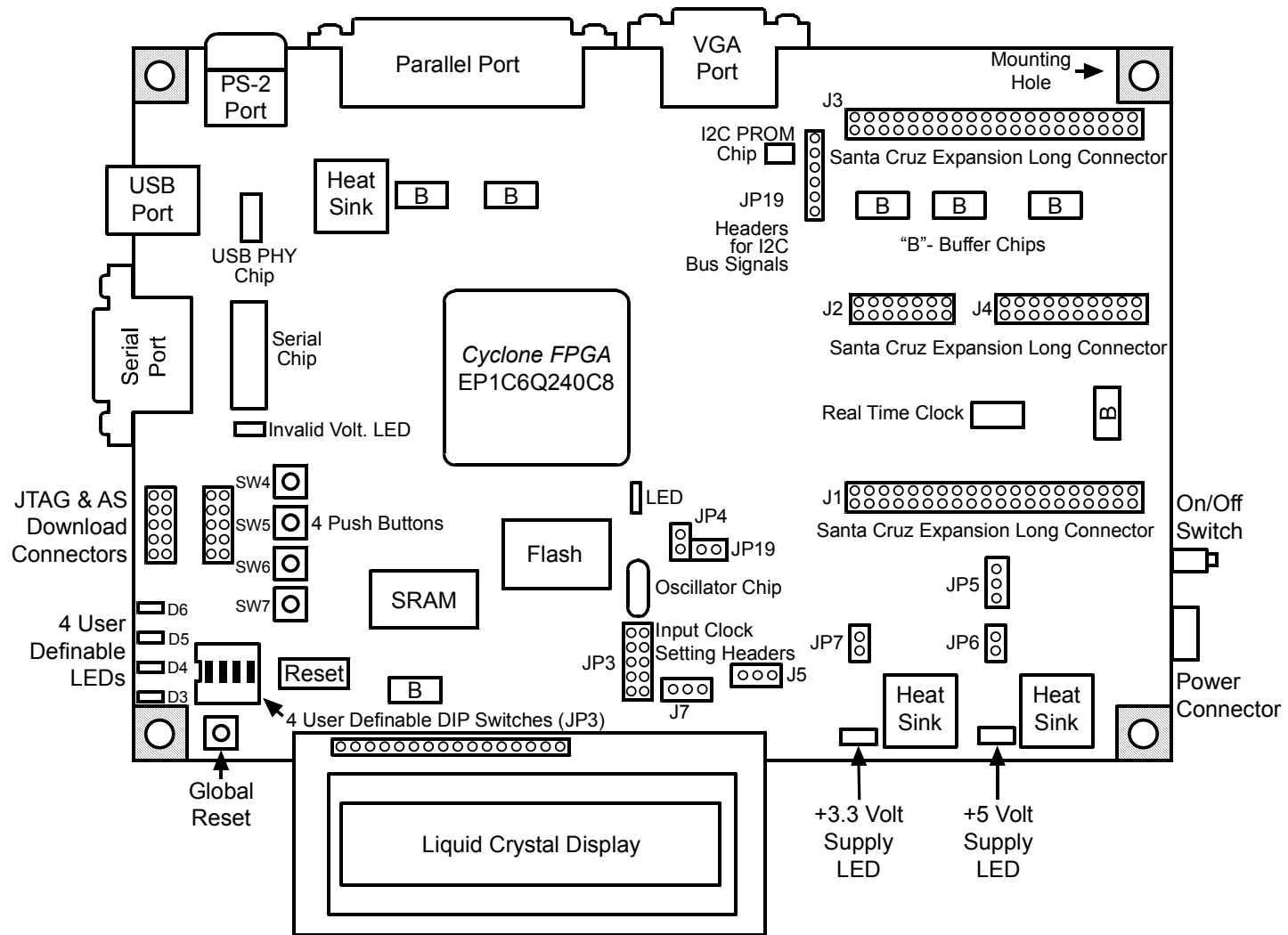


Figure 2.2 The Altera UP 3 board's features.

Table 2.1 UP 3 Board's Cyclone FPGA Features

Cyclone FPGA Feature	EP1C6Q240	EP1C12Q240
Logic Elements (LEs)	5,980	12,060
4K bit RAM blocks (M4Ks)	20	52
Total Internal RAM bits	92,160	239,616
Phase Locked Loops (PLLs)	2	2
User I/O pins	185	173

Table 2.2 UP 3 Board's Memory Features

Memory Device	Size	Part Number
SRAM	64K by 16 bits	ISSI IS61C6416
SDRAM	1M by 16 bits	ISSI IS42S16400B
Flash Memory	1M by 16 bits	Toshiba TC58FVB106AFT-70
I ² C EEPROM	16K by 1bit	ISSI IS24C16
Serial Flash Memory	1M by 1bit	Altera EPCS1

Table 2.3 Overview of the UP 3 Board's I/O Features

I/O Device	Description	Hardware Interface Needed
USB 1.1	Full Speed and Low Speed	Processor & USB SIE engine core
Serial Port	RS 232 Full Modem	UART to send and receive data
Parallel Port	IEEE 1284	State machine or Proc. for handshake
PS/2 Port	PC Keyboard or Mouse	Serial Data - PS/2 state machine
VGA Port for Video Display on Monitor	RGB three 1-bit signals provide 8 colors	State machine for sync signals & user logic to generate RGB color signals
IDE Port	Connector	Processor & IDE Device Driver
Reset Switch	Use for Global Reset	Must use a reset in design
Pushbutton Switches	4 Non-debounced (0=HIT)	Most applications will need a switch debounce Circuit
Expansion Card	Santa Cruz Long 72 I/O	Depends on expansion card used
LEDs	4 User Definable (1=ON)	None
LCD Display	16 Character by 2 line ASCII Characters	State machine or Processor to send ASCII characters and LCD commands
Real Time Clock	I ² C clock chip	Serial Data - I ² C state machine
DIP Switch	4 Switches (1=ON)	None or Synchronizer Circuit

Table 2.4 UP 3 Board's most commonly used FPGA I/O pin names and assignments

Pin Name	Pin#	Pin I/O Type	Function of Pin
PS2_CLK	12	Bidirectional	PS2 Connector
PS2_DATA	13	Bidirectional	PS2 Connector
RESET	23	Input	Power on or SW8 pushbutton reset (Reset = 0)
USB_CLK	29	Input	USB 48MHz Clock - jumper
USER_CLOCK	38	Input	External Clock from J2 Pin 2
PBSWITCH_4	48	Input	Pushbutton SW4 (non-debounced, 0 = button hit)
PBSWITCH_5	49	Input	Pushbutton SW5 (non-debounced, 0 = button hit)
LCD_E	50	Output	LCD Enable line
LED_D6	53	Output	LED D3 (0 = LED ON, 1= LED OFF)
LED_D5	54	Output	LED D4 (0 = LED ON, 1= LED OFF)
LED_D4	55	Output	LED D5 (0 = LED ON, 1= LED OFF)
LED_D3	56	Output	LED D6 (0 = LED ON, 1= LED OFF)
PBSWITCH_6	57	Input	Pushbutton SW6 (non-debounced, 0 = hit)
DIPSWITCH_1	58	Input	DIP Switch SW3 #1 (ON = 1, OFF = 0)
DIPSWITCH_2	59	Input	DIP Switch SW3 #2 (ON = 1, OFF = 0)
DIPSWITCH_3	60	Input	DIP Switch SW3 #3 (ON = 1, OFF = 0)"
DIPSWITCH_4	61	Input	DIP Switch SW3 #4 (ON = 1, OFF = 0)

Table 2.4 (continued) UP 3 Board's most commonly used FPGA I/O pin names and assignments

Pin Name	Pin#	Pin I/O Type	Function of Pin
PBSWITCH_7	62	Input	Pushbutton SW7 (non-debounced, 0 = hit)
LCD_RW	73	Output	LCD R/W control line
MEM_DQ[0]	94	Bidirectional	Memory/LCD Data Bus
MEM_DQ[1]	96(133)	Bidirectional	Memory/LCD Data Bus
MEM_DQ[2]	98	Bidirectional	Memory/LCD Data Bus
MEM_DQ[3]	100	Bidirectional	Memory/LCD Data Bus
MEM_DQ[4]	102(128)	Bidirectional	Memory/LCD Data Bus
MEM_DQ[5]	104	Bidirectional	Memory/LCD Data Bus
MEM_DQ[6]	106	Bidirectional	Memory/LCD Data Bus
LCD_RS	108	Output	LCD Register Select Line
MEM_DQ[7]	113	Bidirectional	Memory/LCD Data Bus
VGA_GREEN	122	Output	VGA Connector Green Video Signal
CPU_CLOCK	153	Input	CPU Clock 100 or 66MHz - jumper
VGA_BLUE	170	Output	VGA Connector Blue Video Signal
VGA_VSYNC	226	Output	VGA Connector Vert Sync Signal
VGA_HSYNC	227	Output	VGA Connector Horiz Sync Signal
VGA_RED	228	Output	VGA Connector Red Video Signal