

Jeffrey Alan Davis
Assistant Professor
School of Electrical and Computer Engineering
Georgia Institute of Technology
January 2005

I. Earned Degrees

Degree	Year	University	Field
B.E.E.	1993	Ga. Tech	Electrical Engineering
M.S.E.E.	1997	Ga. Tech	Electrical Engineering
Ph.D.	1999	Ga. Tech	Electrical and Computer Engineering

II. Employment

Title	Organization	Years
Assistant Professor	Georgia Institute of Technology School of Electrical & Computer Engineering (Atlanta, Georgia)	8/99 - present
Graduate Research Assistant	Georgia Institute of Technology School of Electrical & Computer Engineering (Atlanta, Georgia)	1/94-7/99
Engineering Intern	Lawrence Livermore National Laboratory (Livermore, CA)	6/92-9/92
Engineering Intern	International Business Corporation (Lexington, KY)	6/91-9/91
Resident Housing Assistant	Georgia Institute of Technology Housing Department (Atlanta, GA)	9/91- 6/93

III. Teaching

A. Individual Student Guidance

Ph.D. Students Supervised

Graduated Ph.D. Students

1. Raguraman Venkatesan
Began advising: Spring 2001 (co-advised with Prof. James Meindl)
Preliminary exam passed: Spring 1999
Proposal exam passed: Spring 2002
Graduated: Spring 2003
Research Topic: Optimal Multilevel Interconnect Architectures for Gigascale Integration (GSI)

Current Ph.D. Students

1. Pranav Anbalagan
Began advising: Fall 2000
Preliminary exam passed: Spring 2001
Research Topic: Limits and Opportunities for VLSI Interconnect Length Prediction
2. Ajay Joshi
Began advising: Fall 2001
Preliminary exam passed: Fall 2001
Research Topic: Two-slot TDMA Networks for VLSI Multilevel Interconnect Architectures
3. Vinita Deodhar
Began advising: Fall 2001
Preliminary exam passed: Fall 2001
Research Topic: Optimal Communication Throughput VLSI Interconnect Circuits
4. Gerald Lopez
Began advising: Spring 2002 (co-advised with Prof. James Meindl)
Preliminary exam passed: Fall 2002
Research Topic: Statistical Interconnect Fluctuations for Gigascale Integration (GSI)
5. Heather Luman
Began advising: Fall 2002
Preliminary exam passed: Spring 2004
Research Topic: On-chip Inductance Insertion for High Performance Clock Distribution Networks

Master's Student Guidance

Graduated Master's Students

1. Harshit Shaw
Began advising: Fall 2000
Graduated: Spring 2002
Preliminary exam passed: Spring 2001
Research Topic: Opportunities and Limitations of High-throughput Global Interconnect Networks

2. Mamie Aldridge
Began advising: Fall 2002
Graduated: Spring 2004
Research Topic: VLSI Global Power Distribution Networks

3. Alex Talpasanu
Began Advising: Fall 2003
Graduated: Fall 2004
Research Topic: Interconnect Modeling of Custom Bus Architectures

Undergraduate Student Guidance

1. Mamie Aldridge (Summer Undergraduate Research in Engineering (SURE) Program)
Advised: Summer 2000
Project Title: The Impact of On-chip Interconnect Communication Networks on Reducing Wiring Demand for Gigascale Integration

2. James Freedman (UROP)
Advised: Spring 2000
Project title: Interconnect Prediction for a Interconnect-centric VLSI Design Flow

3. Brian Bell (UROP)
Advised: Spring 2000-present
Project title: Maximizing Bandwidth per Unit Area for On-chip Networks

4. Chris Shoukry (UROP)
Advised: Spring 2000–Fall 2002
Graduated: Fall 2002
Project title: Quasi-Optimal High-Speed Repeater Networks for ULSI

5. Tim Cooper (UROP)
Advised: Spring 2000-Summer 2003
Project title: Quasi-Optimal High-Speed Repeater Networks for ULSI

6. Jonathan James (UROP)
Advised: Spring 2000
Project title: Interconnect Complexity Metrics for the Future of Computing

7. Vaibhav Jain (UROP)
Advised: Fall 2000
Project title: Cache Area Models

8. Garth Milford (UROP and special problems)
Advised: Spring 2000-present
Project title: Computer Engineering Education for K-12

9. Melissa Gravely (UROP and special problems)
Advised: Spring 2000
Project title: Computer Engineering Education for K-12

10. Arica Carter (UROP and special problems)
Advised: Spring 2000
Project title: Computer Engineering Education for K-12

11. Kevin Delk (UROP and special problems)
Advised: Spring 2000

Project title: High-Speed Interconnect Design

12. Jeet Shaw (UROP and special problems)

Advised: Spring 2001

Project title: Computer Engineering Education for K-12

13. Sekou Remy (UROP and SURE Program)

Advised: Spring 2000-Summer 2002

Project title: Statistical Properties of Logic Netlists

14. Kerron Miles (UROP and special problems)

Advised: Summer 2002-Summer 2003

Project title: Computer Engineering Education for K-12

15. Saunvit Pandya (UROP)

Advised: Spring 2003-Summer 2004

Project Title: Impact of Vias on Throughput-centric VLSI Wire Design

16. Nirav Bodiwali (UROP)

Advised: Spring 2003-Fall 2003

Project Title: VLSI Interconnect Statistical Extraction Methods

17. Reshma Parekh (PURA)

Advised: Spring 2003-Fall 2003

Project Title: Interconnect Limits for Current VLSI Designs

18. Aziza Rahman (PURA)

Advised: Spring 2004-present

Project Title: Extraction of Wiring Statistics Using SKILL Code

19. Ifiok Udowana (PURA)

Advised: Spring 2004-present

Project Title: Efficient HSPICE Models of VLSI Global Wires

IV. Scholarly Accomplishments

A. Published Books And Parts Of Books

1. J.A. Davis and J.D. Meindl, Eds., *Interconnect Technology and Design for Gigascale Integration*. Boston: Kluwer Academic Publishers, 2003.
2. J.A. Davis, A. Naeemi, and J. Meindl, "Distributed RC and RLC Transient Models," *Interconnect Technology and Design for Gigascale Integration*. Boston: Kluwer Academic Publishers, pp. 111-158, 2003.
3. J.A. Davis, R. Venkatesan, and J. Meindl, "Stochastic Multilevel Interconnect Modeling and Optimization," *Interconnect Technology and Design for Gigascale Integration*. Boston: Kluwer Academic Publishers, pp. 219-262, 2003.

B. Refereed Publications

Refereed Journal Papers

1. J. D. Meindl and J.A. Davis, "Interconnect Performance Limits of Gigascale Integration (GSI)," *Materials Chemistry and Physics*, vol. 41, no. 3, pp. 161-166, August 1995.
2. J. D. Meindl, J.A. Davis, and G. Vish, "A New Metric for GSI," *Pico Frontier*, June 1, 1996.
3. J.A. Davis, V.K. De, and J.D. Meindl, "A Stochastic Wire Length Distribution for Gigascale Integration (GSI) Part I: Derivation and Validation," *IEEE Transactions on Electron Devices*, vol. 45, no. 3, pp. 580-589, March 1998.

4. J.A. Davis, V.K De, and J.D. Meindl, "A Stochastic Wire Length Distribution for Gigascale Integration (GSI) Part II: Applications to Clock Frequency, Power Dissipation, and Chip Size Estimation," *IEEE Transactions on Electron Devices*, vol. 45, no. 3, pp. 590-597, March 1998.
5. J. A. Davis and J.D. Meindl, "Is Interconnect the Weak Link?" *Circuits and Devices Magazine*, pp. 30-36, March 1998.
6. J. D. Meindl and J.A. Davis, "The Fundamental Limit on Binary Switching Energy for Terascale Integration (TSI)," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 10, pp. 1515-1516, October 2000.
7. J. A. Davis and J. D. Meindl, "Compact Distributed RLC Interconnect Models Part I: Single Line Transient, Time Delay, and Overshoot Expressions," *IEEE Transactions on Electron Devices*, vol. 47, no. 11, pp. 2068-2077, November 2000.
8. J. A. Davis and J. D. Meindl, "Compact Distributed RLC Interconnect Models Part II: Coupled Line Transient Expressions and Peak Crosstalk in Multilevel Networks," *IEEE Transactions on Electron Devices*, vol. 47, no. 11, pp. 2078-2087, November 2000.
9. Q. Chen, J. A. Davis, P. Zarkesh-Ha, and J. D. Meindl, "A Compact Physical via Blockage Model," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 8, no. 6, pp. 689-692, December 2000.
10. P. Zarkesh-Ha, J. A. Davis, and J. D. Meindl, "Prediction of Net-Length Distribution for Global Interconnects in a Heterogeneous System-on-a-Chip," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 8, no. 6, pp. 649-659, December 2000.
11. J.A. Davis, R. Venkatesan, A. Kaloyeros, M. Bylansky, S.J. Souri, K. Banerjee, K.C. Saraswat, A. Rahman, R. Reif, and J.D. Meindl, "Interconnect Limits on Gigascale Integration (GSI) in the 21st Century," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 305-324, March 2001.
12. J.D. Meindl, Q. Chen, and J.A. Davis, "Limits on Silicon Nanoelectronics for Terascale Integration," *Science*, vol. 293, no. 5537, pp. 2044-2049, September, 2001.
13. R. Venkatesan, J. A. Davis, K. A. Bowman, and J. D. Meindl, "Optimal n-Tier Multilevel Interconnect Architectures for Gigascale Integration (GSI)," *IEEE Transactions on VLSI Systems*, vol. 9, no. 6, pp. 899-912, December 2001.
14. J. W. Joyner, R. Venkatesan, P. Zarkesh-Ha, J.A. Davis, and J. D. Meindl, "Impact of Three-dimensional Architectures on Interconnects in Gigascale Integration," *IEEE Transactions on VLSI Systems*, vol. 9, no. 6, pp. 922-928, December 2001.
15. R. Venkatesan, J.A. Davis, and J.D. Meindl, "Compact Distributed RLC Interconnect Models – Part III: Transients in Single and Coupled Lines with Capacitive Load Termination," *IEEE Transactions on Electron Devices*, vol. 50, no. 4, pp. 1081-1093, April 2003.
16. R. Venkatesan, J.A. Davis, and J.D. Meindl, "Compact Distributed RLC Interconnect Models – Part IV: Unified Models for Time Delay, Crosstalk and Repeater Insertion," *IEEE Transactions on Electron Devices*, vol. 50, no. 4, pp. 1094-1102, April 2003.
17. A. Naeemi, J. A. Davis, and J. D. Meindl, "Analysis and Optimization of Co-planar RLC Lines for GSI global interconnection," *IEEE Trans. Electron. Devices*, vol. 51, pp. 985-995, June 2004.
18. A. Naeemi, J. A. Davis, and J. D. Meindl, "Compact physical models for multilevel interconnect crosstalk in GSI," Letter of final acceptance received Sept. 9, 2004 to *IEEE Trans. Electron. Devices*.
19. V. Deodhar and J.A. Davis, "Optimization of Throughput performance for Low Power VLSI Interconnects," Letter of final acceptance received August 31, 2004 to *IEEE Transactions on VLSI Systems*.
20. A. Joshi and J.A. Davis, "Wave-Pipelined Time Division Multiplexing (TDM) Routing for Gigascale Integration," submitted October 2004 to *IEEE Transactions on VLSI Systems*.

Refereed Conference Publications

1. V.K. De, J.C. Eble, D.S. Wills, J.A. Davis, and J.D. Meindl, "A Generic System Simulator (GENESYS) for Microelectronics Technology and Applications," *Proceedings of the Government Microcircuit Application Conference (GOMAC'96)*, Orlando, FL, March 1996, pp. 439-442.
2. J. A. Davis, V. K. De, and J.D. Meindl, "A Priori Wiring Estimations and Optimal Multilevel Wiring Networks for Portable ULSI Systems," *Proceedings of 46th Electronic Components and Technology Conference*, Orlando, FL, May 1996, pp. 1002-1008.
3. J.C. Eble, V.K. De, J.A. Davis, and J.D. Meindl, "Optimal Multilevel Interconnect Technologies for Gigascale Integration (GSI)," *1996 Proceedings of the 13th Annual VLSI Multilevel Interconnection Conference (VMIC)*, Santa Clara, CA, June 1996, pp. 40-45.
4. J. A. Davis, J. C. Eble, V. K. De, and J. D. Meindl, "A Complete Stochastic Wiring Distribution for Gigascale Integration (GSI)," *Material Research Society Symposium Proceedings*, San Francisco, CA, vol. 427, 1996, pp. 23-34.
5. J. A. Davis, V. K. De, and J. D. Meindl, "Optimal Low Power Interconnect Networks," *Digest of Technical Papers of the 1996 Symposium on VLSI Technology*, Honolulu, HI, June 1996, pp. 78-79.
6. J.D. Meindl, V.K. De, D.S. Wills, J.C. Eble, X. Tang, J.A. Davis, B. Austin, and A.J. Bhavnagarwala, "Impact of Stochastic Dopant and Interconnect Distributions on Gigascale Integration," *Proceedings of the 1997 IEEE International Solid-State Circuits Conference*, San Francisco, CA, February 1997, pp. 232-233.
7. J.D. Meindl, J.A. Davis, X. Tang, J.C. Eble, A.J. Bhavnagarwala, and B. Austin, "Intrinsic Limits on Gigascale Integration due to Stochastic Dopant and Interconnect Placement," *Proceedings of the Government Microcircuit Application Conference (GOMAC '97)*, Las Vegas, NV, March 1997, pp. 305-308.
8. J. A. Davis, V. K. De, and J. D. Meindl, "A Stochastic Wire Length Distribution for Gigascale Integration," *Proceedings of the Custom Integrated Circuit Conference*, San Francisco, CA, pp.145-150, May 1997.
9. J.A. Davis and J.D. Meindl, "Interconnect Limits on Gigascale Integration (GSI)," *Material Research Society Symposium Proceedings*, San Francisco, CA , vol. 473, pp. 293-302, 1997.
10. P. Zarkesh-Ha, J.A. Davis, W. Loh, and J.D. Meindl, "On a Pin Versus Gate Relationship for Heterogeneous Systems: Heterogeneous Rent's Rule," *Proceedings of the Custom Integrated Circuit Conference*, San Francisco, CA, pp. 93-96, May 1998.
11. J.A. Davis and J.D. Meindl, "Length, Scaling, and Material Dependence of Crosstalk between Distributed RC Interconnects," *Proceedings of the 1999 International Interconnect Technology Conference*, San Francisco, CA, pp. 227-229, May 1999.
12. J.A. Davis and J.D. Meindl, "Compact Distributed RLC Models for Multilevel Interconnect Networks," *1999 VLSI Symposium on Technology Digest of Technical Papers*, Kyoto, Japan, pp. 165-166, June 1999.
13. R. Venkatesan, J.A. Davis, and J.D. Meindl, "Performance Enhancement Through Optimal N-tier Multilevel Interconnect Architectures," *Proceedings of the 12th IEEE ASIC/SOC Conference*, Washington, DC, pp. 19-23, Sept. 1999.
14. J. W. Joyner, P. Zarkesh-Ha, J. A. Davis, and J. Meindl, "Vertical Pitch Limitations on Performance Enhancement in Bonded Three-Dimensional Interconnect Architectures," *Proceedings of the International Workshop on System-Level Interconnect Prediction*, San Diego, CA, pp. 123-127, April 2000.
15. P. Zarkesh-Ha, J. A. Davis, W. Loh, and J. Meindl, "Prediction of Interconnect Fan-out Distribution Using Rent's Rule," *Proceedings of the International Workshop on System-Level Interconnect Prediction*, San Diego, CA, pp. 107-112, April 2000.
16. J. W. Joyner, P. Zarkesh-Ha, J. A. Davis, and J. D. Meindl, "A Three-Dimensional Stochastic Wire-Length Distribution for Variable Separation of Strata," *Proceedings of the International Interconnect Technology Conference*, San Francisco, pp. 1126-1128, June 2000.

17. R. Venkatesan, J.A. Davis, K. Bowman, and J. Meindl, "Optimal Repeater Insertion for N-tier Multilevel Interconnect Architectures," *Proceedings of the International Interconnect Technology Conference*, San Francisco, CA, pp. 132-134, June 2000.
18. Q. Chen, J. A. Davis, P. Zarkesh-Ha, and J. D. Meindl, "A Novel Via Blockage Model and Its Implications," *Proceedings of the International Interconnect Technology Conference*, San Francisco, CA, pp. 15-17, June 2000.
19. R. Venkatesan, J.A. Davis, K. A. Bowman, and J. D. Meindl, "Minimum Power and Area N-Tier Multilevel Interconnect Architectures Using Optimal Repeater Insertion," *Proceedings of the International Symposium on Low Power Electronics and Design*, Rapallo/Portofino Coast, Italy, pp. 167-172, July 26-27, 2000.
20. J. D. Meindl, R. Venkatesan, J. Davis, J. Joyner, A. Naeemi, P. Zarkesh-Ha, M. Bakir, T. Mule, P. Kohl, and K. Martin, "Interconnecting Device Opportunities for Gigascale Integration (GSI)," *Technical Digest of International Meeting on Electron Device Meeting*, Washington, DC, pp. 525-258, December 2001.
21. A. Naeemi, J. A. Davis, and J. D. Meindl, "Analytical Models for Coupled Distributed RLC Lines with Ideal and Non-Ideal Return Paths," *Technical Digest of International Meeting on Electron Devices Meeting*, Washington, DC, pp. 689-692, December 2001.
22. R. Venkatesan, J.A. Davis, and J.D. Meindl, "A Complete Physical Model for Distributed RLC Interconnects -- Transient Voltage, Time Delay and Crosstalk," *Proceeding of the IEEE/ACM Design Automation Conference (DAC)*, New Orleans, pp.763-766, June 2002.
23. R. Venkatesan, J.A. Davis and J.D. Meindl, "Time Delay, Crosstalk and Repeater Insertion Models for High Performance SoC's," *Proceedings of the IEEE ASIC/SOC Conference*, Rochester, NY, pp. 404-408, Sept. 2002.
24. H. Shah, P. Shiu, B. Bell, M. Aldredge, N. Sopory, and J.A. Davis, "Repeater insertion and wire sizing optimization for throughput-centric VLSI Global Interconnect," *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, pp. 280-284, Nov. 2002.
25. A. Naeemi, J.A. Davis, and J.D. Meindl, "Optimal Global Interconnect Devices for GSI," *Technical Digest of International Electron Device Meeting*, Washington, D.C. pp.319-322, Dec. 2002.
26. P. Anbalagan and J.A. Davis, "Maximum Multiplicity Distributions (MMD)," *International Workshop on System Level Interconnect Prediction*, Monterey, CA, pp. 107-113, April 2003.
27. A. Talpasanu, G. Milford, K. S. A. Miles, and J.A. Davis "Computer Educational Datapath (CED): Basic Computer Design for K-12 Education," *IEEE International Conference on Information Technology (ITCC)*, Las Vegas, Nevada, pp. 86-90, April 2003.
28. J.W. Joyner, R. Venkatesan, J.A. Davis, J.D. Meindl, "The limits of system improvements through liquid diagonal routing of interconnects," *Proceedings of the IEEE 2003 International Interconnect Technology Conference*, June 2003, pp.227-229.
29. V. Deodhar and J.A. Davis, "Voltage Scaling and Repeater Insertion for High-Throughput Low-Power Interconnect Networks," *Proceedings of the 2003 IEEE International Symposium on Circuits and Systems (ISCAS)*, Bangkok, Thailand, pp. 349-352, June 2003.
30. R. Venkatesan, J.A. Davis, and J.D. Meindl, "Optimal Multilevel Interconnect Architecture Aspect Ratios for GSOCs," *Proceedings of the 2003 IEEE SOC Conference*, Rochester, NY, pp. 17-20, September 2003.
31. A. Naeemi, J.A. Davis, J.D. Meindl, "Compact Physical Models for Multi-level Interconnect Crosstalk in Gigascale SoC," *Proceedings of the IEEE International SoC Conference*, Rochester, NY, pp. 199-202, September 2003.
32. A. Joshi and J.A. Davis, " A 2-Slot Time-Division Multiplexing (TDM) Interconnect Network for Gigascale Integration (GSI)" *2004 IEEE/ACM International Workshop on System Level Interconnect Prediction (SLIP)*, Paris, France, pp. 64-46, February 2004.
33. P. Anbalagan and J.A. Davis, "Maximum Multiplicity Distribution for Length Prediction Driven Placement," *17th International Conference on VLSI Design*, Mumbai, India, pp. 981-986, April 2004.

34. H. Luman and J.A. Davis, "Inductance Enhancement in Global Clock Distribution Networks," *2004 IEEE International Interconnect Technology Conference (IITC)*, San Francisco, CA, pp. 119-122, June 2004.
35. K.K. Ryu, A. Talpasanu, V. Mooney, and J.A. Davis, "Interconnect Delay Aware RTL Verilog Bus Architecture Generation for an SoC," *Asia-Pacific Conference on Advanced Systems Integrated Circuits (AP-ASIC 2004)*, Japan, pp.176-179, August 2004.
36. V. Deodhar and J. Davis, "Voltage Scaling, Wire Sizing and Repeater Insertion Design Rules for Wave-Pipelined VLSI Global Interconnect Circuits," *IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2005.
37. V. Deodhar and J. Davis, "Designing for Signal Integrity in Wave-Pipelined SoC Global Interconnects," *IEEE System-on-Chip Conference (SOCC)*, September 2005.
38. A. Joshi and J. Davis, "Gigascale ASIC/Soc Design Using Wave-Pipelined Multiplexed (WPM) Routing," *IEEE System-on-Chip Conference (SOCC)*, September 2005.
39. A. Joshi, V. Deodhar, and J. Davis, "Low Power Multilevel Interconnect Networks Using Wave-Pipelined Multiplexed (WPM) Routing," *IEEE VLSI Design Conference*, January 2006.

C. Other Publications

1. J.A. Davis, "Guest Editorial for Special Issue on System Level Interconnect Prediction (SLIP)", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 4, pp. 337-338, April 2004.
2. J. Davis, V. Deodhar, and A. Joshi, "Design Based Approaches vs. Process / Material Solutions for Interconnect," invited paper, *Advanced Metallization Conference (AMC)*, September 2005.

D. Presentations

1. J.A. Davis, R. Venkatesan, K. Bowman, and J.D. Meindl, "Gigascale Integration (GSI) Interconnect Limits and N-Tier Multilevel Interconnect Architectural Solutions," *Proceedings of the International Workshop on System-Level Interconnect Prediction*, San Diego, CA, pp. 147-148, April 8-9, 2000.
2. J.A. Davis, A. Naeemi, and V. Deodhar, "Compact Models for VLSI Interconnects", Tutorial Session at the *International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, March 22, 2004.

V. Service

A. Professional Contributions

Professional Society Activities

1. IEEE Member 2001-present
2. Committee Member of the 2001 International Technology Roadmap for Semiconductor Technical Working Group (TWG) for Design

Conference and Workshop Committees

1. Co-Program Chair 2001 and General Chair for 2002 System Level Interconnect Prediction (SLIP) Workshop
2. Review Committee Member for IEEE Symposium on Circuits and Systems 2004 (5 papers)

Editorial and Reviewer Activities

1. Reviewer for *IEEE Transactions on VLSI Systems* (17 papers) 2000-present

2. Reviewer for IEEE International Symposium on Circuits and Systems (6 papers) 2001-present
3. Reviewer for International Workshop on SLIP (17 papers) 2000-present
4. Reviewer for *IEEE Proceedings* (1 paper total) 2001-present
5. Reviewer for *IEEE Transactions on CAD* (2 papers total) 2003-present
6. Reviewer for *IEEE Transactions on Nanotechnology* (1 paper total) 2003-present
7. Guest Editor for Special Section of the *IEEE Transactions on VLSI Systems* on System-Level Interconnect Prediction Issue (April 2004).

B. Campus Contributions

Service on Graduate Student Committees

Student	Ph.D. Qualifying Exam	Ph.D. Thesis Proposal	Ph.D. Thesis Defense
1. Jennifer English			SPRING 2000
2. Mondira Deb Pant		SPRING 2000	SUMMER 2000
3. Payman Zarkesh-Ha		SUMMER 2000	SPRING 2001
4. Sasikumar P. Cherubal		FALL 2000	SPRING 2002
5. William Robinson		SPRING 2000	SUMMER 2003
6. Mark Wolfe	SPRING 2001		
7. Martin Saint-Laurent		SPRING 2001	
8. James Joyner		FALL 2002	SUMMER 2003
9. Raguraman Venkatesan		FALL 2002	SUMMER 2003
10. Qiang Chen		SUMMER 2002	SPRING 2003
11. Azad Naeemi		FALL 2002	SUMMER 2003
12. Muhannad Bakir		FALL 2002	FALL 2003
13. Alfred Gnomes		FALL 2001	FALL 2003
14. Kyeong Keol Ryu		FALL 2003	SUMMER 2004
15. Steve Nugent		FALL 2003	
16. Amer Atrash		FALL 2003	SPRING 2004
17. Steve Nugent			SPRING 2005
18. Martin St. Lawrence			SPRING 2005
19. Yuvrag Dhillon			SPRING 2005

Service on School Committees

1. ECE Student Faculty Committee (ECESFC) Member (1999-present) and Chair (2000-present)
As chair, the ECESFC help to organize a set of yearly activities that include: ECE Family Day, ECE Student Awards, TIG Week, Freshman-Sophomore Class meetings, Take-A-Professor to lunch, Undergraduate Research Opportunity Program (UROP) Paper Competition, and outreach through FIRST LEGO League.
2. COE representative on Institute Undergraduate Curriculum Committee (IUCC) (2002-present)
3. COE representative on the Campus Undergraduate Research Committee (2004-present)

C. Other Contributions

1. FIRST LEGO League Tournament Partner for the State of Georgia (2001-present)

As tournament partner, Jeff Davis established the FIRST LEGO Robotic Competition in the state of Georgia. In November 2003 over 260 elementary and middle school students participated in this event. On January 15th,

2005 over 420 elementary and middle school children participated in this event at Georgia Tech Campus Recreational Center (CRC).

2. NSF Fast Student Mentor (2002-present)
3. Intel Undergraduate Research Advisor (2003-present)

VI. Grants and Contracts

A. As Principal Investigator or Co-Principal Investigator

1. Title: "A Hierarchy of Limits for Gigascale Integration" co-principal investigator with James Meindl and Scott Wills
Organization: Semiconductor Research Corporation
Contract Period: February 2000 – February 2001
Total Amount Funded: \$200,000
Amount Allocated to Jeff Davis: \$70,000
2. Title: NSF CAREER Award: "Interconnect Dominant ULSI Design: A New Paradigm for 21st Century IC Design and Education"
Organization: National Science Foundation
Contract Period: January 2001 - January 2006
Amount Requested: \$306,367
Amount Funded: \$306,367
3. Title: "Interconnect Length Prediction and Length Prediction Driven Placement"
Organization: National Science Foundation
Contract Period: April 2001 - February 2005
Amount Requested: \$274,992
Amount Funded: \$171,467
4. Title: SRC Educational Alliance for Undergraduate Research
Organization: Semiconductor Research Corporation
Contract Period: Gift (GTF) 2000-2001
Amount Funded: \$18,000
5. Title: SRC Educational Alliance for Summer Undergraduate Research
Organization: Semiconductor Research Corporation
Contract Period: Gift (GTF) Summer 2001
Amount Funded: \$18,000
6. Title: SRC Educational Alliance for Undergraduate Research
Organization: Semiconductor Research Corporation
Contract Period: Gift (GTF) 2001-2002
Amount Funded: \$18,000
7. Title: SRC Educational Alliance for Undergraduate Research
Organization: Semiconductor Research Corporation
Contract Period: Gift (GTF) 2002-2003
Amount Funded: \$12,000
8. Title: Cross-Disciplinary Learning Inspired Through Example
PI: Narayanan M. Komerath (School of AE)
Organization: Georgia Tech College of Engineering
Contract Period: Gift (GTF) 2003-2004

Amount Funded: \$23,000

Amount Allocated to Jeff Davis: \$2,453

VII. Honors and Awards

1. Georgia Institute of Technology, School of Electrical and Computer Engineering's 1993 Faculty Award.

This award was received as a student in the ECE department for dedication and service to the school.

2. Georgia Institute of Technology President's Fellow, 1994-1997
3. Best Student Paper Award of the 1999 International Interconnect Technology Conference
4. NSF CAREER Award (January 2001)
5. School of Electrical and Computer Engineering Outstanding Junior Faculty Award (April 2003)