Fabrication of CMOS ICs

ECE6130
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Outline

• Overview of Silicon Processing
• Material Growth and Deposition
• Lithography
• CMOS Process Flow
Integrated Circuits created on Silicon Wafers (100-300mm)

The wafer is subjected to 1000s of individual processing steps to make each IC!!
Fabrication Yield

\[ Y = \frac{N_G}{N_T} \times 100\% \]

\( N_G = \text{Number of good working die} \)
\( N_T = \text{Total number of die sites} \)

Yield enhancement is complex and time consuming!!
Total # of Die ($N_T$) Estimation

\[
N_T = \left( \frac{(d - d_e)^2}{4A_{\text{die}}} \right)
\]

\[d = \text{wafer diameter}\]
\[d_e = \text{wasted edge distance}\]

\textit{note that this indicates floor function}
$d_e$ calculation?
More exact calculation.

$$N_T = \prod_{i=0}^{1} \frac{2b}{a} \text{Min}(R_i, R_{i+1})$$

$$R_j = \sqrt{R_w^2 \left( \frac{jab - R_w}{b} \right)^2}$$

$R_w$ = radius of wafer

$a$ & $b$ = dimensions of the wafer
Square Die Approximation?

\[ N_T = \frac{2R_w^2}{A_{\text{die}}} + 4\frac{\sqrt{2R_w}}{\sqrt{A_{\text{die}}}} \]

\[ \hat{c} = 2R_w - 2R_w A_{\text{die}} ^{1/2} \]

\[ \hat{d} = \frac{2R_w}{\sqrt{A_{\text{die}}}} \cdot R_w \sqrt{2} \]

\[ \hat{e} = \frac{2\sqrt{A_{\text{die}}}}{2} \]
$Y = e^{-\sqrt{DA}}$

Yield and Die Size

Yield (AMD (180nm) Athlon XP) vs. Chip Area

Intel (180nm) P4
Yield over product lifetime

Lesson for VLSI Designer?

**Keep die size SMALL!!!**

Example AMD vs. Intel:
AMD Athlon XP (180nm) 129mm² (200mm wafers)
Intel’s P4 (180nm) 217mm² (200mm wafers)

AMD Athlon XP (130nm) 80mm² (200mm wafers)
Intel’s P4 (130nm) 116mm² (300mm wafers)
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Thermal Oxide Growth

(a) Growth phase

(b) Final structure

\[ x_{Si} \equiv 0.46 x_{ox} \]
Dry vs. Wet Oxidation

Dry Oxidation: Slow but high quality: Heat accelerates reaction

\[ Si + O_2 \rightarrow SiO_2 \]

Wet Oxidation: Fast but high quality: Heat accelerates reaction

\[ Si + H_2O \rightarrow SiO_2 + 2H_2 \]
Wet/Dry Combo Example

START (100) p-type 10 ohm cm wafers
CLEAN in H2(SO)4-H2O2 piranha etch, 2 min ; clean, rinse, dry
RINSE 1, 4 min
RINSE 2, 4 min
DRY
OXIDIZE 1 hr at 1000 C in Wet Oxygen
place wafers in quartz oxidation boat
insert into furnace ante-chamber
push at 1/2" per sec at 800 C in Oxygen
ramp to 1000 C (10 C/min), 20 min
turn on steam, 60 min
ramp down to 800 C in Oxygen
pull at 1/2" per sec
unload into plastic carriers
CVD Oxide Process

Deposited SiO$_2$ on a surface where no Si is present

Silane

\[ \text{SiH}_4(gas) + 2\text{O}_2(gas) \rightarrow \text{SiO}_2(solid) + 2\text{H}_2\text{O(gas)} \]

LTO = Low Temperature Oxides!
Silicon Nitride (Si$_3$N$_4$)

- Often called nitride only
- Strong barrier to most items
- Use as an overglass layer to protect chip

$$3\text{SiH}_4(\text{gas}) + 4\text{NH}_3(\text{gas}) \rightarrow \text{Si}_3\text{N}_4(\text{solid}) + 12\text{H}_2(\text{gas})$$

Silane  Ammonia  Silicon Nitride
Polysilicon Silicon

• Depositing silicon on Silicon Dioxide produces small crystallites areas
• Called poly for short
• Used for gate eletrode in FETs
• Even heavily doped this has high sheet resistance
• Refractory metals (such Ti) coating on poly to decrease sheet resistance ... this is called a silicide

\[
SiH_4 \rightarrow Si + 2H_2 \quad @ 500-600 \, ^\circ C
\]

Silane
Metals

• Aluminum vs. Copper
  • aluminum bulk resistivity = 2.86e-6 $\Omega$-cm
  • copper bulk resistivity = 1.67e-6 $\Omega$-cm

• Electromigration
  • Current flow displace metal ions in metals

High current density moves the dent!
Electromigration

Design Rules limit current density

Hillocks

Voids

Aluminum

Design Rules limit current density
Doping Silicon Layers

selective doping is very important!!
Ion Implantation
Boron Trifluoride ($BF_3$)

Ion Source

Ion Implantation

magnet

wafer target
Physics 101: One electron-volt is equal to the amount of energy gained by an electron dropping through a potential difference of one volt, which is $1.6 \times 10^{-19}$ joules.
Gaussian Implant Profile

\[ N_{\text{ion}}(x) = N_p e^{-\frac{(x-R_p)^2}{2R_p^2}} \]

Projected Range

\[ N_{\text{ion}}(x) \]

\[ N_p \]

\[ \Delta R_p \]

Straggle
Chemical Mechanical Polish (CMP)

(a) After oxide deposition

(b) After CMP
Epitaxial Layer Growth (EPI)

Trichlorosilane (TCS) @ 1000-1180 °C

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Photo = light!

Excimer Laser Sources

- (250-130nm) Krypton Fluoride (KrF) 248nm
- (90nm) Argon Fluoride ArF (193nm)
- (65nm?) Fluorine F2 (157nm)
Reticle or Mask Definition

Remember: During Layout using CAD tools this is what you are designing!!!
Photoresist Application

(a) Resist application
Vacuum chuck
Photoresist spray
Spinning wafer

(b) Coated wafer
Photoresist coating

(c) Beading
Edge bead
Flat resist
Wafer
Edge bead
Exposure Step

UV

Reticle

Projection optics (not shown)

Reticle shadow

resist-coated wafer surface
Characteristics of positive photoresist

Negative photoresist works in opposite way!!
Etching an Oxide Layer

(a) Initial patterning of resist
(b) After etching process
Reactive Ion Etching

RIE Etching work well with both ion bombardment and chemical reaction etching!!!
Reactive Ion Etch (RIE)

*Source: www.atechsystem.co.kr/custom/rie.pdf

**Source: www.atechsystem.co.kr/custom/rie.pdf**
Ion Implantation of Doped Si Patterns

(a) Incoming ion beam

(b) Doped n-type regions

note: lateral doping
Step-and-Repeat Process

registration targets for alignment between masking steps!
Clean Room Definitions

• Use HEPA filters that are 99.97% effective of removing particles that are 0.5 microns or larger.

• Class X clean rooms means that there are less than X particles per cubic foot with diameter greater than 0.5 micron

• Typical clean room facilities have various class levels
  
  • e.g. TSMC Fab 6 (190,000 sqft 32,000 wafer-per-month)
  
  • Class 100 ballroom has Class 0.1 SMIF minienviroments
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nWell and Active Area Masking Steps

(a) Starting wafer with epitaxial layer

(b) Creation of n-well in p-epitaxial layer

(c) Active area definition using nitride/oxide

*Needed to define oxide electrical isolation between devices!*
Field Oxide (FOX) growth

Field Oxide needed to define oxide electrical isolation between devices!
Self-Aligned Gate Process

*Gate/Drain/Source Regions are automatically aligned*

(a) Gate oxide growth

(b) Poly gate deposition and patterning
Self-Aligned Gate Process

(c) pSelect mask and implant

(d) nSelect mask and implant
Source/Drain Contacts

(a) After anneal and CVD oxide

(b) After CVD oxide active contact, W plugs
Metal Masking Steps

(c) Metal1 coating and patterning

Metal 1 Mask
Via Mask
Metal 2 Mask
Bonding Pad Structure

(a) Top view

(b) Side view
Lightly Doped Drain (LDD) nFET

(a) Light (n-) implant

(b) Oxide coating

Sidewall spacers

Oxide etch to create sidewall spacers (no additional mask needed)

(d) After etching

(d) Heavy donor implant
Lightly Doped Drain (LDD) nFET

Oxide etch to create sidewall spacers (no additional mask needed)
Silicides

- Defined as a refractory metal (e.g. Ti, Ta, Pt, etc) coated over silicon or polysilicon
- Reduce sheet resistance of gate from 25 Ω to 10s mΩ!!

Silicide reduces contact resistance of Tungsten Contact
Copper Interconnect: Damascene

Copper needs a barrier layer (e.g. TiN) to block diffusion to SiO₂!
Dual-Damascene Process

Dual-Damascene structure with copper vias

Copper vias ... 

1) lower resistance than Tungsten

2) Electromigration better!