Option 1: Bail out
Take your grade as is from Test #1 and Test #2 (Available Thursday 7/28)

Option 2: Individual Project
5-7 page term paper on any one of the following subjects:
- Origins of phase noise in CMOS oscillators
- Origins of phase noise in PFDs and frequency dividers
- Derivation of phase noise for an ideal negative resistance oscillator
- Modern all digital PLL implements and performance comparison
- Carrier and symbol recovery using software PLLs
- Comparison of analog and digital phase detectors for lock-in and pull-in in when operating at low SNR
- Chaos generation in PLLs and systems of coupled PLLs
- Phase and frequency locking multiple PLLs
- Any other topic related to frequency synthesis, subject to my approval

Option 3: Group Project (2 min / 3 max):

Design a PLL to meet the following specifications:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Frequency Range</td>
<td>2 – 4 GHz</td>
<td></td>
</tr>
<tr>
<td>Frequency Resolution</td>
<td>200 kHz</td>
<td></td>
</tr>
<tr>
<td>Single Sideband Phase Noise</td>
<td>-75 dBC/Hz</td>
<td>@ 10 kHz Offset</td>
</tr>
<tr>
<td></td>
<td>-100 dBC/Hz</td>
<td>@ 100 kHz Offset</td>
</tr>
<tr>
<td></td>
<td>-120 dBC/Hz</td>
<td>@ 1 MHz Offset</td>
</tr>
<tr>
<td>Reference Spurious</td>
<td>- 80 dBC</td>
<td>At f_{ref} and harmonics</td>
</tr>
<tr>
<td>Acquisition Time</td>
<td>10 msec</td>
<td>Pull-in + Lock</td>
</tr>
</tbody>
</table>

You may assume the following specifications for the loop components:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Detector/Divider Noise Floor</td>
<td>-140 dBC/Hz</td>
<td></td>
</tr>
<tr>
<td>VCO Phase Noise</td>
<td>-100 dBC/Hz @ 100 KHz</td>
<td>Goes as 1/f^2 below and above until the noise floor is met</td>
</tr>
<tr>
<td>VCO Noise Floor</td>
<td>-150 dBC/Hz at 10 MHz</td>
<td></td>
</tr>
<tr>
<td>Reference Phase Noise</td>
<td>-85 dBC @ 10 kHz</td>
<td>Goes as 1/f^2 below and above until phase detector phase noise dominates</td>
</tr>
</tbody>
</table>

Using numerical simulation, validate all specifications are met. Generate 5-7 page report that summarizes results.