1. Describe in mathematical terms the difference between coherent frequency synthesis and incoherent frequency synthesis. Give an example of each.

Let $v(t) = A\cos(\omega t + \theta(t))$, where $\theta(t)$ is a random process. Phase incoherence implies that $\theta$ is uniformly distributed between $-\pi$ and $\pi$. In contract, if $v(t)$ is considered coherent, $\theta$ is distributed with a small variance around some known reference phase.

Coherent synthesis: Phase locked-loop, frequency multiplier, frequency divider

Incoherent synthesis: Combination of free running oscillators mixed to produce a desired output frequency.

2. Illustrate in a block diagram the difference between direct frequency synthesis and indirect frequency synthesis. Give an example of each.

Direct:

$V_S = A\cos(\omega_0 t)$ → $X2$ → $V_{out} = B\cos(2\omega_0 t)$

Indirect:

$A\cos(\omega_{ref} t)$ → PD → $\int$ → $\div N$ → $V_{out} = B\cos(N\omega_{ref} t)$
3. Ferroelectric materials are dielectrics that change their permittivity with an applied static electric field. In this manner, they operate much like semiconductor varactor diodes. However, they have a symmetric \( C-V \) characteristic of the form

\[
C(V_c) = C_0 - C_2 V_c^2
\]

Show that the following circuit is a **frequency tripler**.

4. **Digital phase detectors** come in two varieties: multiplying, and sequential (i.e. edge-triggered). Give an example of each, and calculate the integrated output voltage for the each example for following input waveforms. You may assume that \( k \phi = 1 \), and that sequential logic is negative edge triggered:

**Multiplying:** XOR, XNOR followed by a LPF.

**Sequential:**
a. Symmetric squarewave inputs:

\[ V_{out} = k\phi(\theta_{in} - \theta_{ref}) = \pi/4 = 0.785 \text{ V} \]

b. Asymmetric squarewave inputs:

Sequential: \( V_{out} = 0.785 \text{ V} \)

Multiplying: Unfiltered waveform:

From waveform: \( V_{out} = \pi/8 = 0.393 \text{ V} \)

5. Plot transfer function for a **phase-frequency detector** with a \( k_{\phi} = 1 \).
6. Name one advantage that synchronous frequency dividers have over asynchronous dividers, and vice-versa.

Synchronous dividers have an advantage over asynchronous dividers in that they do not accumulate propagation delays, which could lead to loop instabilities.

Asynchronous dividers can run at higher clock frequencies than synchronous dividers.

7. Dual Modulus Dividers:

a. Draw the block diagram for a dual modulus $\div P/P+1$ frequency divider, label counters as synchronous or asynchronous.

b. Describe its operation step-by-step. If $P = 8$, and $N = 256$, what are the maximum and minimum divide ratios that may be obtained?

1. $\div P+1$ for $(P+1)A$ cyclers
2. Switch to $\div P$.
3. Continue to $\div P$ for $N-A$ cycles.
4. Repeat step 1 and continue.

Maximum division ratio: $NP+A$.
Minimum division ratio: $P+A$