Additive noise contributes to \( \text{rms} \) phase jitter by increasing the variance of the oscillator frequency.

a. Calculate the phase jitter due to the additive noise of a loop amplifier with noise figure \( NF = 3\text{dB} \), and a resonator bandwidth of 100 \( kHz \) operating at 290 \( ^\circ \text{K} \) with a 1 mW output power.

\[
\Delta \phi^2 = \frac{kTBF}{2} \cdot P_s = -174 \text{ dBm/Hz} + 50 \text{ dB} + 3 \cdot -3 = -125 \text{ dB}, \text{ or } 4.0 \cdot 10^{-13} \text{ rad}^2
\]

So, \( \Delta \phi = 6.3 \cdot 10^{-7} \text{ rad} \)

b. Suppose that the oscillator is used as a clock with an output frequency of 1 \( GHz \), calculate the \( \text{rms} \) time jitter of the clock edges.

\[
\Delta t = \Delta \phi / \omega = 6.3 \cdot 10^{-7} / 2\pi \cdot 10^9 = 0.1 \text{ fsec}
\]

2. Show using an analytic derivation or a numerical simulation of the circuit below that the close-in (\text{i.e.} multiplicative) phase noise is independent of the oscillator output power.

\[
e_a^2 = \frac{4kTFR_L}{R_L}
\]
3. Consider the Type-II second order loop shown below.
   a. Derive an expression for the closed loop transfer function \( H(s) = \theta_{\text{out}} / \theta_{\text{ref}} \).

   See next page for derivation.

   b. Let \( k_{\phi} = 2 \pi \text{V/rad} \), \( k_v = 2 \pi \cdot 10 \text{ MHz/V} \), \( \tau_1 = 10 \mu\text{sec} \), \( \tau_2 = 1 \mu\text{sec} \), and \( N = 1500 \).

   Calculate the damping factor \( \zeta \), natural frequency \( \omega_n \), and loop BW \( \omega_c \) of the PLL.

   \[
   K = 2 \pi \cdot 2 \pi \cdot 10^7 / 1500 = 2.6 \cdot 10^5 \text{ sec}^{-1}
   \]

   \[
   \omega_n = \left(\frac{K}{\tau_1}\right)^{1/2} = 1.6 \cdot 10^5 \text{ rad/sec} = 26 \text{ kHz}
   \]

   \[
   \zeta = \frac{1}{2} \left( \frac{\tau_2}{\tau_1} + 1 \right) \omega_n = 0.39 \text{ (under damped)}
   \]

   \[
   \Rightarrow \omega_c \approx \omega_n \cdot 1.55 \Rightarrow f_c \approx 40 \text{ kHz} \text{ (exact calculations shown on MCAD file)}
   \]

   c. Determine the settling time \( t_s \) for the PLL to recover to within 5% of its steady state value if a unit step error is applied to the PD input \( \theta_{in} \).
\[ H(s) = \frac{k_0 k_u H_u(s)}{s + \frac{k_1}{k_0} k_4 k_u H_u(s)} = \frac{k \frac{1 + s \tau_2}{1 + s \tau_1}}{s^2 + s \tau_1 + k \left( 1 + s \tau_2 \right)} \]

\[ \omega_n^2 = \frac{k}{\tau_1}, \quad s = \frac{1}{\tau_1} \left( 1 + \frac{1}{\omega_n^2} \right) \omega_n \]

\[ \therefore \quad H(s) = N \frac{s \left( 1 + s \tau_2 \right)}{s^2 + 2 \frac{k}{\tau_1} s + k \omega_n^2} \]

By normalizing frequency,

\[ H(s) = \frac{1 + s \tau_2}{\left( \frac{s}{\omega_n} \right)^2 + 2 \frac{k}{\omega_n^2} \frac{s}{\omega_n}} \]
4. Suppose that a reference oscillator and VCO that will be used in a PLL that have a phase noise spectra described by the following expressions:

\[ L_{\text{ref}}(f_m) = kTF \quad L_{\text{VCO}}(f_m) = kTF \left( 1 + \frac{f_c^3}{f_m^3} \right) \]

For a given multiplication ratio \( N \), derive an expression for the cut-off frequency \( \omega_c \) that optimizes the phase noise if the PLL transfer function and error transfer functions are respectively given by

\[
H(j\omega) = \begin{cases} 
N & \text{for } \omega \leq \omega_c \\
0 & \text{for } \omega > \omega_c 
\end{cases} \quad H_e(j\omega) = \begin{cases} 
0 & \text{for } \omega \leq \omega_c \\
1 & \text{for } \omega > \omega_c 
\end{cases}
\]

See next page for derivation.
Definition 4:

\[ z_{\text{lim}} = \begin{cases} \frac{12}{K} & \text{if } K < 3.1 \\ 12.04 \log N & \text{if } K \geq 3.1 \end{cases} \]

\[ F_{\text{opt}} = \frac{F_c}{F_{\text{opt}}} = \left( N^2 - 1 \right)^{-1/3} \]

\[ F_{\text{opt}} = F_c \left( N^2 - 1 \right)^{-1/3} \]

Large \( N \)