

## Kedar K. Karandikar

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**OBJECTIVE:** Seeking a competitive full time position in Computer Engineering or related fields

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### EDUCATION

- **Master of Science** – Electrical and Computer Engineering (Expected Dec 08)  
Georgia Institute of Technology, Atlanta GPA: 3.37/4.0  
Relevant Coursework:  
Software & Hardware Co-operative Computing, Advanced VLSI, Advanced Computer Architecture, Multiprocessor Interconnection Networks.  
**Research:** “Hyper Transport Switch Design with Interval Routing” in the Computer Architecture and Systems Lab (CASL) with Prof. Yalamanchili
  - **Bachelor of Engineering** – Electronics and Telecommunication Engineering (Jul 07)  
University of Mumbai, India GPA: 3.8/4.0  
Relevant Coursework: Computer Architecture and Organization, Digital Logic Design, Computer Communication Networks, Internet Communication Engineering
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### WORK EXPERIENCE

- Graduate Student Internship (May 08 – Aug 08)  
**Simulation Acceleration Team – Intel Corporation, Folsom**
    - Code coverage Analysis of the internal tool set
    - Memory leak Detection of the tools and fixing of the leaks
    - Perl scripts written to interface the coverage analysis tools with the internal environment
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### PUBLICATIONS

- **Multi-core Image processing System using Network on Chip Interconnect** at the 50th IEEE International Midwest Symposium on Circuits and Systems on Circuits and Systems, Aug 5-8, 2007, Montreal, Canada
  - **Reconfigurable Architecture for a Network on Chip router towards Multiprocessor application** at National Conference on Recent advances in Electronics and Communication Technology-2006, Nov 9-10, 2006, Ludhiana, India.
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### PROJECTS

- Hyper Transport Switch Design with Interval Routing (Jan 08 – April 08)
  - CUDA Implementation of Parsec Benchmark Suite (Jan 08 – April 08)  
*Parallelization of the ‘fluidanimate’ and ‘swaptions’ benchmarks in the suite using CUDA*
  - VLSI Design of 4x4 SRAM Cell Array (Jan 08 – April 08)  
*Design and Layout of the SRAM cell array and its peripheral circuits using Cadence Virtuoso*
  - Fast Interval Router – An Interval router for Mesh Networks (Sept 07 – Nov 07)  
*Implementation of interval routing mechanism for 4x4 mesh topology using Verilog and C*
  - MOESI Cache Coherence Protocol (Nov 07)  
*Developed a generic MOESI Cache Coherence Protocol Simulator for SA and DM cache in C++*
  - Tomasulo Algorithm Implementation – Done in Verilog (Nov 07)
  - Tournament Branch Predictor  
*Modified existing Gshare Predictor simulator to simulate Tournament branch predictor. Coding was in C++*
  - Network on Chip Router to Enhance Interprocessor Communication (Jul 06 – Jul 07)  
*Implemented a network on chip router in VHDL and further tested using Spartan FPGAs*
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### SKILLS

- **Hardware Description Language:** VHDL, Verilog/SystemVerilog
- **Software skills:** C, C++, Perl, OpenMP, CUDA
- **Tools:** Bullseye Code Coverage, Valgrind, Modelsim, Xilinx ISE 9.2, Cadence Virtuoso
- **Operating System:** Windows, Linux (Ubuntu and SUSE)
- **Hardware Experience:** Worked with Spartan 2 and Spartan 3 FPGA kits