

ECE2030A Fall 2008
Introduction to Computer Engineering
Exam #3

50 min in-class exam.
Close books, close notes.
NO calculator.

This exam is given under the Georgia Tech Honor Code System. You must observe and sign the Honor Pledge: "I have neither given nor received aid on this exam." Your print name and signature below signifies your compliance with this honor code.

Name (Print): _____ **SOLUTION** _____

Signature: _____

1. _____ (30 pts)
2. _____ (30 pts)
3. _____ (40 pts)

Total (100 pts) _____

1. (30%) General Questions. (Circle **one** of the answers)

1.1. How many output bits will be generated when performing 5-bit by 5-bit integer multiplication?

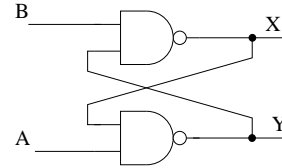
- (a) 5 bits
- (b) 10 bits
- (c) 25 bits
- (d) 32 bits

ANSWER

1.2. Given the latch shown below, which of the following could cause an unstable state?

- (a) $A = B = 0$
- (b) $A = 1, B = 0$
- (c) $A = 0, B = 1$
- (d) $A = B = 1$

ANSWER (X=Y=1)



1.3. Which of the following memory contains the least number of transistors?

- (a) One bit DRAM **ANSWER**
- (b) One bit RS Latch (2nd most)
- (c) One bit Register (most)
- (d) One bit SRAM (2nd least)

1.4. What is the capacity of $2^k \times N$ where $k=21, N=32$?

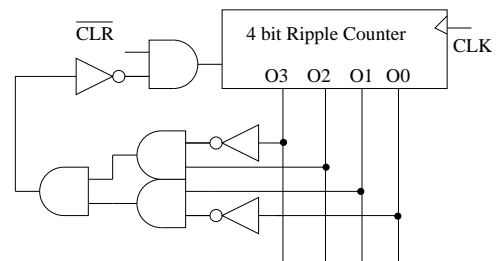
- (a) 8 M Bytes **ANSWER ($2^{21} \times 2^5 = 2^{26} = 64 \text{ M Bits} = 8 \text{ M Bytes}$)**
- (b) 64 M Bytes
- (c) 2 M Bytes
- (d) 32 M bits

1.5. Which type of the following memory requires periodic refreshing to not lose data?

- (a) D Flip-Flop
- (b) DRAM **ANSWER (has a capacitor that needs to be refreshed)**
- (c) SRAM
- (d) On-chip L1 Cache

1.6. Given the Mod-N counter shown below, what is N?

- (a) 6
- (b) 7 **ANSWER**
- (c) 8
- (d) 9

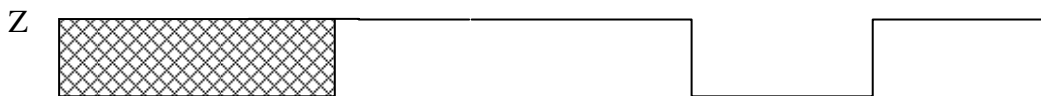
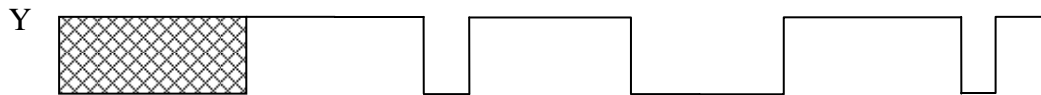
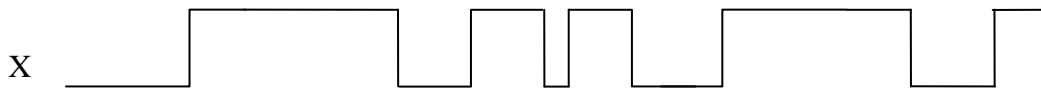
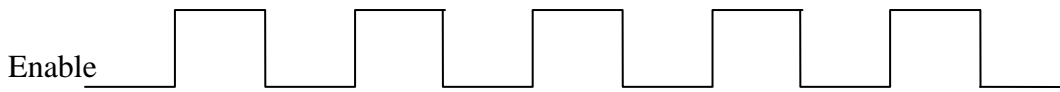
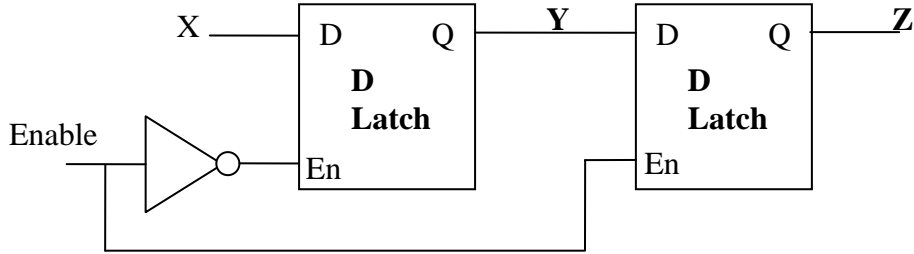


O3:O1 = 0110, therefore resets after 6. Counts from 0 to 6, therefore is modulo-7 counter.

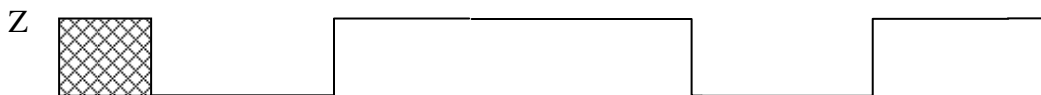
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2. (30%) **Latch and Flip Flops.**

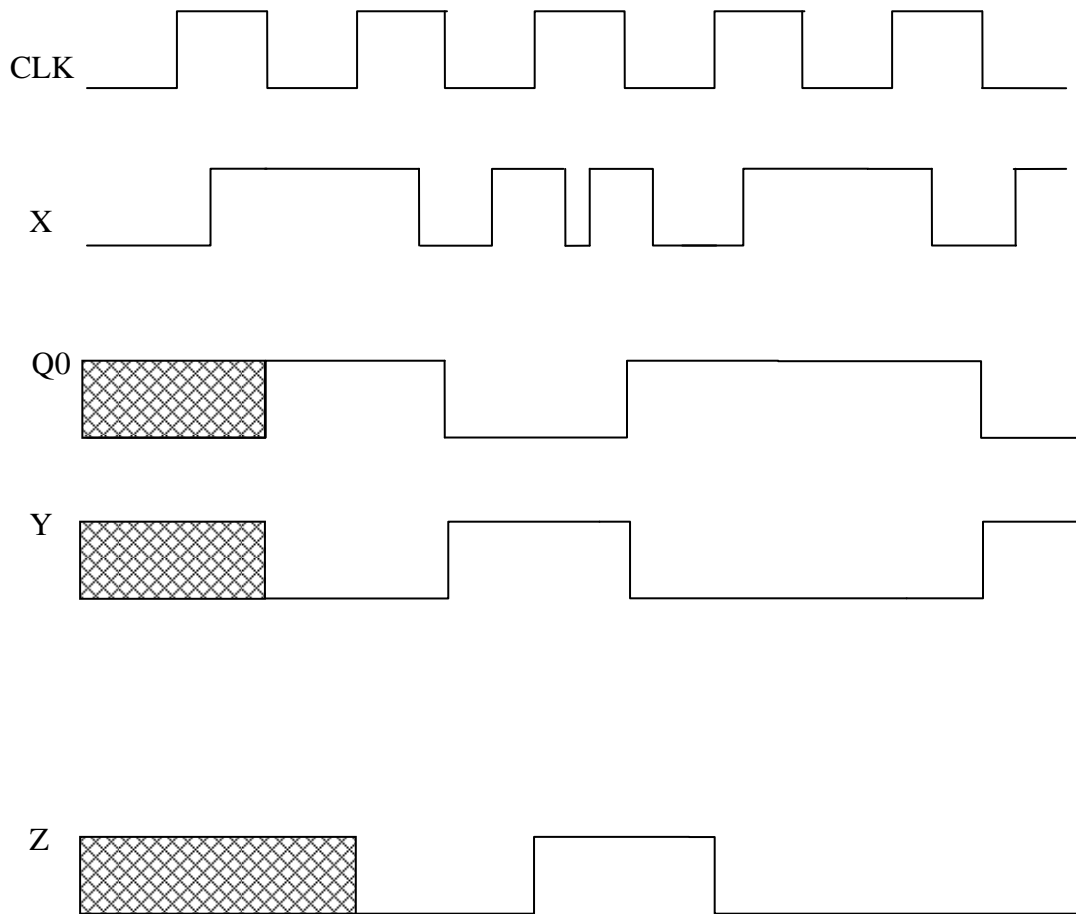
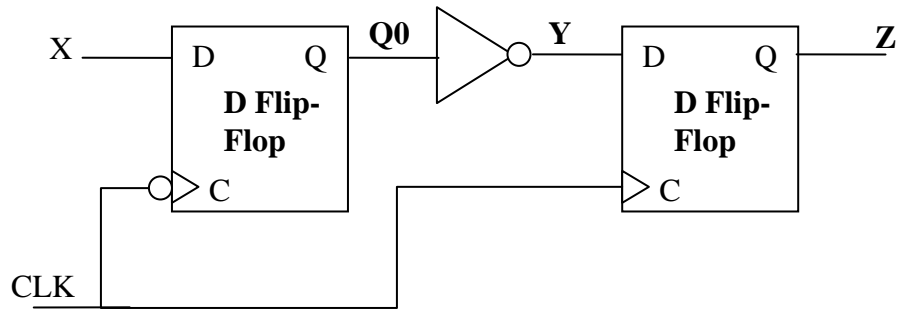
2.1. (10%) Given the following input waveforms Enable and X, please draw the corresponding timing diagrams (or waveform) of **Y** and **Z** for each of the following circuits. Assume the initial states of all latches or flip-flops are **unknown**.



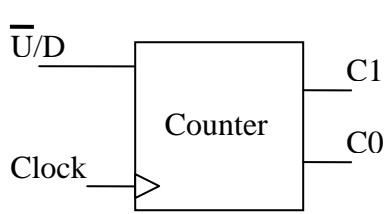
If you recognize this was a positive edge triggered flip flop, you would get:



2.2. (10%) Given the following input waveforms CLK and X, please draw the corresponding timing diagram (or waveform) of Y and Z for each of the following circuits. Assume the initial states of all latches or flip-flops are **unknown**.



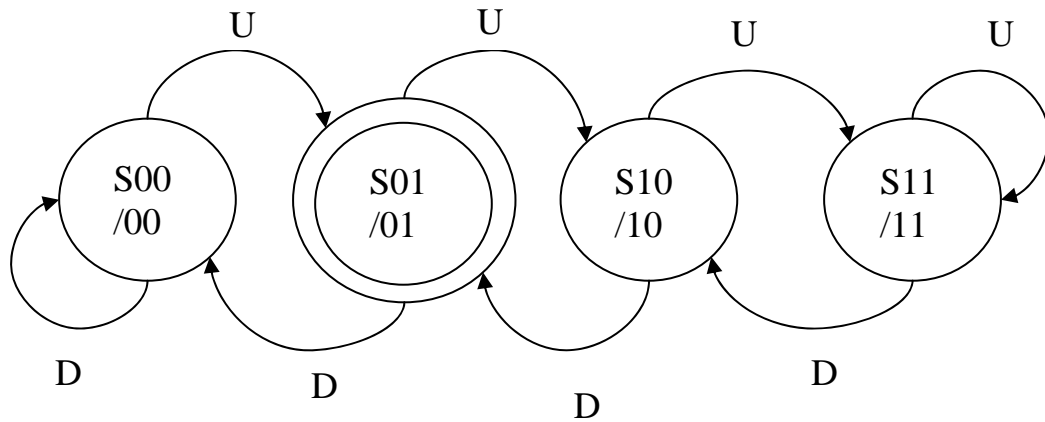
3. (40%) State machine design. Design a **2-bit up/down saturating counter** using the **Finite State Machine** method: derive the state diagram, state table, and draw the circuits. The counter consists of 2 inputs (one for controlling direction, the other one is the clock) and 2 outputs that represent the current count value. The functionality of this counter is described in the pseudo code on the right.



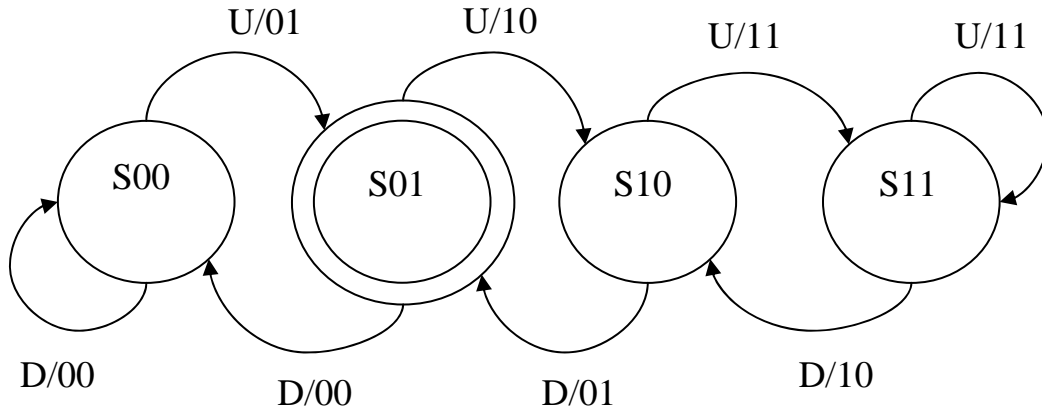
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if ( $\overline{U/D} == 0$ ) then
    if ( $C1C0 \neq 11$ )
        increment the counter;
else /*  $\overline{U/D} == 1$  */
    if ( $C1C0 \neq 00$ )
        decrement the counter;
    
```

3.1. (10%) Draw the State Diagram.



Alternate:



This is the elevator problem. You get in on a floor, and you have two options Up/Down. If you are on the top floor, hitting up keeps you on the top floor. If you are on the bottom floor, hitting down keeps you on the bottom floor. On every positive clock edge, you arrive at the next floor. The output is the floor you are on, and the input is your selection and the time it takes to transfer you to the next floor (clock).

3.2. (15%) Derive the State Table and simplify the equations with Karnaugh maps.

Present State		Input (X)	Next State		Output	
P1	P0	U'/D	N1	N0	C1	C0
0	0	0	0	1	0	0
0	0	1	0	0	0	0
0	1	0	1	0	0	1
0	1	1	0	0	0	1
1	0	0	1	1	1	0
1	0	1	0	1	1	0
1	1	0	1	1	1	1
1	1	1	1	0	1	1

$C1 = P1.$

$C0 = P0.$

Alternate:

Present State		Input (X)	Next State		Output	
P1	P0	U'/D	N1	N0	C1	C0
0	0	0	0	1	0	1
0	0	1	0	0	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	0	1	0	1	0	1
1	1	0	1	1	1	1
1	1	1	1	0	1	0

$C1 = N1.$

$C0 = N0.$

The Next State logic for either method is the same.

For N1:

P1 \ P0 X	00	01	11	10
0	0	0	0	1
1	1	0	1	1

For N0:

P1 \ P0 X	00	01	11	10
0	1	0	0	0
1	1	1	0	1

$$N1 = P0 \cdot \bar{X} + P1 \cdot \bar{X} + P1 \cdot P0$$

$$= (P0 + P1) \cdot \bar{X} + P1 \cdot P0$$

$$N0 = \bar{P0} \cdot \bar{X} + P1 \cdot \bar{X} + P1 \cdot \bar{P0}$$

$$= (\bar{P0} + P1) \cdot \bar{X} + P1 \cdot \bar{P0}$$

3.3. (15%) Draw the sequential logic of this counter of your design. You do not need to draw the internals of the D Flip-Flop, simply draw each D Flip-Flop as a block.

The diagram below shows the answer for when $C1 = N1$, and $C0 = N0$.

The diagram for the other solution is the same, except $C1$ is pulled from $P1$, and $C0$ from $P0$.

