

# Michael B. Healy

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## Address:

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## EDUCATION

### Georgia Institute of Technology, Atlanta, GA

**2001 - 2010**

- Ph.D in Electrical and Computer Engineering 08/2010 GPA: 3.77
- MS in Electrical and Computer Engineering 05/2006 GPA: 3.85
- BS in Computer Engineering with **Highest Honor** 05/2004 GPA: 3.71

### Texas Academy of Mathematics and Science

**1999-2001**

- Two-year residential early admissions university program
- Graduated with honors and 74 semester hours 05/2001 GPA: 3.83

## HONORS

- Member of Eta Kappa Nu National Electrical and Computer Engineering Honor Society
- Member of Pi Mu Epsilon National Mathematics Honor Society
- Received Presidents Undergraduate Research Award, Spring 2004
- Member of the National Honor Society, 2001

## SKILLS

### Programming:

C++, Perl, MATLAB, JAVA, BASIC

### Research Experience:

- Led an 11-member physical design team on the implementation of a 64-core memory-on-processor 3D-integrated system sent for fabrication using 130-nm technology in March of 2010.
- Experience with usage and modification of microarchitectural simulators.
- Experience with thermal and power-supply-network modeling and simulation.
- Focus on 3D integration technologies and consideration throughout research career.
- Thorough knowledge of a variety of physical design algorithms for partitioning, placement, floorplanning, and routing.
- Familiarity with Cadence physical design tools, including Encounter, VoltageStorm, Library Characterizer, and Virtuoso.

## WORK EXPERIENCE

### Intel Corporation – Architecture Team for World’s First 45-nm Processor

Folsom, California

Graduate Intern

05/2006 – 01/2007

- Generated large datasets for the Compiler Dungeon using a large number of custom-made Perl scripts.
- Updated the Coho architectural simulator with Penryn-specific architectural features written in C++.
- Researched new branch prediction schemes for the Penryn architecture using a custom-made Perl-based trace-driven branch predictor simulator.
- Gained experience collaborating with large groups in a corporate environment.

## PUBLICATIONS – continued on reverse

**Journal:**

1. M. Ekpanyapong, **M. B. Healy**, and S. K. Lim, "Profile-driven instruction mapping for dataflow architectures," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 12, pp. 3017-3025, December 2006.
2. **M. B. Healy**, M. Vittes, M. Ekpanyapong, C. Ballapuram, S. K. Lim, H.-H. S. Lee, and G. H. Loh, "Multi-objective microarchitectural floorplanning for 2D and 3D ICs," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 1, pp. 38-52, January 2007.
3. **M. B. Healy**, F. Mohamood, S. K. Lim, and H.-H. S. Lee, "Integrated microarchitectural floorplanning and runtime controller for inductive noise mitigation," submitted to *ACM Transactions on Design Automation of Electronic Systems*, 2010.
4. **M. B. Healy** and S. K. Lim, "Temperature and power-supply-noise scaling in many-tier 3D systems," submitted to *ACM Journal of Emerging Technologies in Computing Systems*, 2010.
5. **M. B. Healy** and S. K. Lim, "Novel through-silicon-via topology for power-supply-noise reduction," to be submitted to *IEEE Transactions on Very Large Scale Integrated Systems*, 2010.

**Conference:**

6. **M. B. Healy**, S. Ravindran, and D. Anderson, "Effects of varying parameters in asymmetric adaboost on the accuracy of a cascade audio classifier," in *IEEE Southeast Regional Conf.*, pp.169-172, March 2004.
7. M. Ekpanyapong, **M. B. Healy**, and S. K. Lim, "Placement for configurable dataflow architecture," in *IEEE/ACM Asia South Pacific Design Automation Conf.*, pp. 1127-1130, January 2005.
8. **M. B. Healy**, M. Ekpanyapong, and S. K. Lim, "MILP-based placement and routing for dataflow architecture," in *International Conf. on Field Programmable Logic and Applications*, pp. 71-76, August 2005.
9. **M. B. Healy**, M. Vittes, M. Ekpanyapong, C. Ballapuram, S. K. Lim, H.-H. S. Lee, and G. H. Loh, "Microarchitectural floorplanning under performance and temperature tradeoff," in *Design, Automation and Test in Europe*, pp. 1298-1293, March 2006.
10. F. Mohamood, **M. B. Healy**, S. K. Lim, and H.-H. S. Lee, "A floorplan-aware dynamic inductive noise controller for reliable processor design," in *ACM/IEEE International Symp. on Microarchitecture*, pp. 3-14, December 2006.
11. F. Mohamood, **M. B. Healy**, S. K. Lim, and H.-H. S. Lee, "Noise-Direct: A technique for power supply noise aware floorplanning using microarchitecture profiling," in *IEEE Asia South Pacific Design Automation Conf.*, pp. 786-791, January 2007.
12. **M. B. Healy**, F. Mohamood, H.-H. S. Lee, and S. K. Lim, "A unified methodology for power supply noise reduction in modern microarchitecture design," in *IEEE Asia South Pacific Design Automation Conf.*, pp. 611-616, January 2008.
13. **M. B. Healy**, H.-H. S. Lee, G. H. Loh, and S. K. Lim, "Thermal optimization in multi-granularity multi-core floorplanning," in *IEEE/ACM Asia South Pacific Design Automation Conf.*, pp. 43-48, January 2009.
14. **M. B. Healy** and S. K. Lim, "A study of stacking limit and scaling in 3D ICs: An interconnect perspective," in *IEEE Electronic Components and Technology Conf.*, pp. 1213-1220, May 2009.
15. Y.-J. Lee, **M. B. Healy**, and S. K. Lim, "Co-design of reliable signal and power interconnects in 3D stacked ICs," in *IEEE International Interconnect Technology Conf.*, pp. 56-58, June 2009.
16. **M. B. Healy** and S. K. Lim, "Power delivery system architecture for many-tier 3D systems," in *IEEE Electronic Components and Technology Conf.*, pp. 1682-1688, June 2010.
17. **M. B. Healy**, S. K. Lim, et al., "Design and analysis of 3D-MAPS: A many-core 3D processor with stacked memory," in *IEEE Custom Integrated Circuits Conf.*, September 2010.

References available upon request.