Switched Capacitor Band-Pass Filter

0.1 Object

The object of this experiment is to design and implement a fourth-order Chebyshev band-pass filter using a switched-capacitor realization. The specifications of the filter are: passband ripple 1.8 dB, center frequency $f_C = 4\,\text{kHz}$, $-3\,\text{dB}$ bandwidth $f_{3\,\text{dB}} = 2\,\text{kHz}$, gain at the center frequency $H_{BP} = 1$. The transfer function is to be realized as the product of a second-order high-pass filter in cascade with a second-order low-pass filter.

To obtain the transfer function for the filter, see page 13 of the Filter Potpourri. Follow the example for the $8th$ order band-pass filter to solve for the required value of x and B in the frequency transformation from a low-pass filter function to a band-pass filter function. The frequency transformation for the band-pass filter is given on page 6 of the Filter Potpourri. Use it to solve for the transfer function.

After you obtain the band-pass transfer function, use Mathcad or any math program to plot the dB gain versus frequency for the function. If you use Mathcad, be sure to use a range variable for the frequency that gives equal x-axis spacings on a log scale. Check to see if the center frequency and the $-3\,\text{dB}$ bandwidth are correct. If they are correct, use Mathcad to factor the denominator of the transfer function into the product of two second-order transfer functions.

Rewrite the factored transfer function as the product of a high-pass filter function and a low-pass filter function. Realize the two filter functions using the methods and hardware described below. The parts will be supplied by our laboratory support staff. The information below is from the lab manual for ECE 3042. It describes the devices available and how to use them. Other that that, it contains more information than is needed for this experiment.

0.2 Switched Capacitor Theory

Active filter design with op amps is a robust mature discipline. All of the classical filter types that were implemented in bygone eras with resistors, capacitors, and inductors may now be implemented solely with resistors, capacitors, and op amps. The accuracy of these filters is limited by only the precision of the components and the properties of the physical op amps employed. If discrete resistors and capacitors are used, variations within the manufacturer's stated tolerance may produce unacceptable error in the design unless extremely expensive components are employed.

The resistors and capacitors required for filter design may be fabricated on monolithic integrated circuits along with the op amps but they usually require a large amount of area and are subject to temperature drift and other annoying effects such as parasitic capacitance. Resistors fabricated on integrated circuits are usually restricted to values less than $10\,\text{k}\Omega$

while the upper limit for capacitors is approximately 100 pF. Also, it is quite difficult to obtain precise values of passive components fabricated on integrated circuits. Such dedicated analog filter integrated circuits are available but they are rather expensive.

The problem of component variation may be overcome with switched capacitor filters. These use small integrated circuit capacitors whose terminals are switched by a high frequency clock signal using MOSFET switches to simulate large values of resistance. The MOSFETs are fabricated on the same integrated circuit while the clock may be external or also resident on the integrated circuit.

Switched capacitor filters are not a panacea. They are digital circuits and are, therefore, subject to aliasing. The Nyquist criterion requires that the waveform be sampled at a rate at least twice its bandwidth to prevent aliasing. Normally the clock frequency is picked to be large compared to the critical frequencies of the filter (50 to 100 times larger) to prevent aliasing. Also, the output is a discrete rather than continuous waveform. To minimize both of these defects it is customary to precede the digital switched capacitor filter with an anti-aliasing analog low-pass filter to limit the bandwidth and to follow the digital filter with an analog deglitching filter. The break frequencies of these analog filters are not crucial so this use of analog filters at the input and output is not a major impediment.

0.2.1 Switched Capacitor Integrator

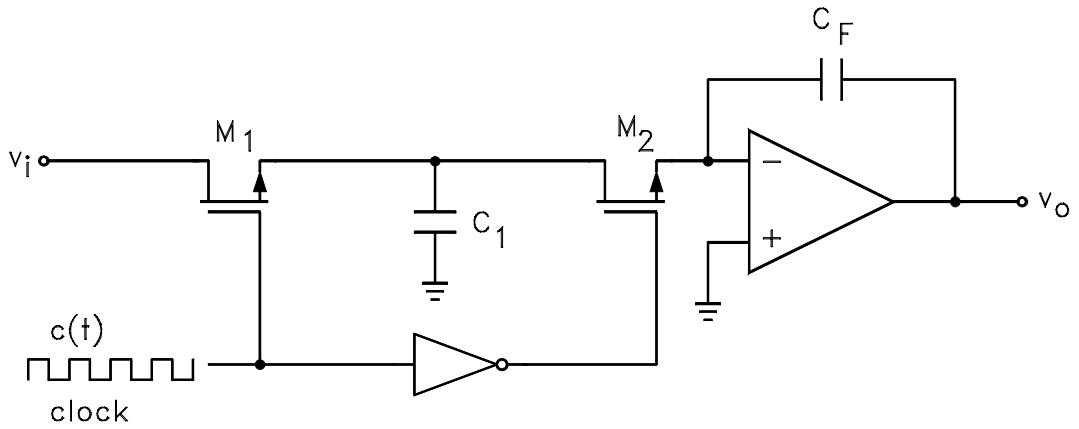

Figure 0-1 Switched capacitor integrator.

A switched capacitor integrator is shown in Fig. 0-1. The clock signal $c(t)$ with frequency f_c and period $T_c = 1/f_c$ is applied to both the gate input of MOSFET M_1 and the digital

INVERTER. The signal applied to the gate of MOSFET M_2 is the complement of the clock. Hence, excepts for the switching transient, one MOSFET is on while the other is off.

When the clock is high MOSFET M_1 is on and M_2 is off. Capacitor C_1 has a charge $\Delta q = C_1 v_i$ placed on it by the input to the filter. If the clock frequency is large compared to the bandwidth of v_i the input may be considered to be constant during the sampling interval $T_c/2$. During the next clock half cycle M_1 is off and M_2 is on which places the top node of the capacitor C_1 at the virtual ground of the op amp which causes the charge on it to be transferred to C_F. The average current flowing into capacitor C_1 is

$$i(t) = \frac{\Delta q}{T_c} = \frac{C_1}{T_c} v_i = C_1 f_c v_i \tag{1}$$

which means that it is equivalent to a resistor $R_{eq} = 1/C_1 f_c$. The output of the op amp is then given by

$$v_o = -\frac{1}{C_F}\int_{-\infty}^{t} i(u)\,du = -\frac{C_1 f_c}{C_F}\int_{-\infty}^{t} v_i(u)\,du = -\frac{1}{C_F R_{eq}}\int_{-\infty}^{t} v_i(u)\,du \tag{2}$$

which makes this circuit an integrator. Integrators are the heart of the state variable filter which means that any of the classical filters may be realized with this switched capacitor arrangement. Other more elaborate topologies are also employed in switched capacitor filters but the circuit in Fig. 0-1 illustrates the basic principle.

Because charge is transferred in spurts from capacitor C_1 to capacitor C_F this makes the output voltage discrete rather than continuous. The voltage increments are reduced to acceptable values by picking the clock frequency to be large which is also required to prevent aliasing. A deglitching analog low-pass filter cascaded with the output may also be used to smooth the output voltage.

Since the output of the switched capacitor integrator depends on the ratio of two capacitances, this can easily be fabricated on an integrated circuit. Although precise values of components are difficult to control, maintaining ratios is relatively simple.

Anent the equivalent resistance being set as $R_{eq} = 1/C_1 f_c$, this makes controlling the critical frequencies of the filter elementary. The system clock sets the critical frequencies. Therefore, such filters may be easily electronically tuned.

When a MOSFET is on the drain to source resistance is not zero but has a certain value know as the on-resistance R_{on} which is normally several hundred ohms. This means that the charging and discharging of capacitor C_1 is not instantaneous but limited by an RC time constant $\tau_{on} = R_{on} C_1$. This sets the upper limit for the system clock. Proper operation requires that the period of the system clock be large compared to the charging time constant. With current MOS technology this makes operation of switched capacitor filters above a few hundred kilo-hertz impossible.

0.2.2 Second Order Filter Categories

Because switched capacitor filters are digital circuits, the appropriate mathematical artifice to analyze them is the z transform. However, classical frequency domain analysis is sufficiently accurate and more amendable to a mathematical tractable analysis. This discussion

will be limited to second order filters because that is what is implemented in the device that will be ultimately employed in this experiment.

Low-Pass Filter

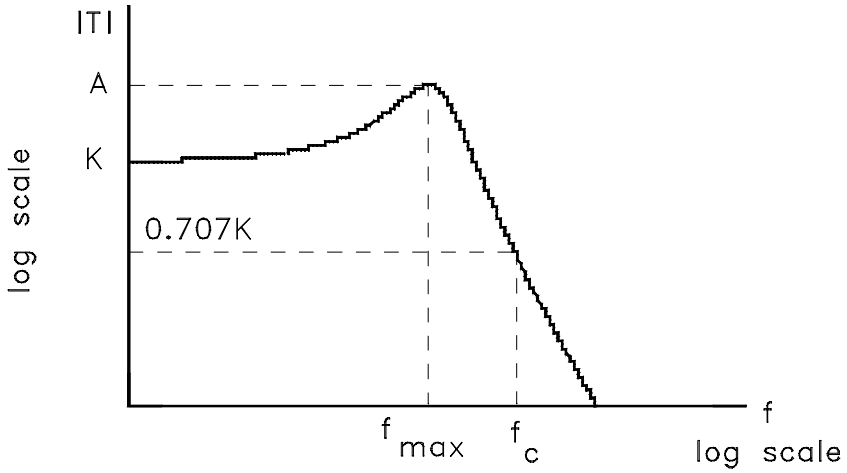

Figure 0-2 Second-order low-pass filter.

The complex transfer function for a second-order low-pass filter is

$$T(s) = K \frac{1}{\left(\frac{s}{\omega_0}\right)^2 + \frac{1}{Q}\left(\frac{s}{\omega_0}\right) + 1} \tag{3}$$

where K is the DC gain of the filter, Q is the quality factor, and ω_0 is the resonant frequency of the filter. The magnitude of the complex transfer function is plotted in Fig. 0-2. The $-3\,\mathrm{dB}$ or half-power cutoff frequency f_c is the frequency at which the gain is reduced to $K/\sqrt{2}$ and is given by

$$f_c = f_0 \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}} \tag{4}$$

which is a frequency larger than f_0. The maximum value of the magnitude of the complex transfer function A occurs at the frequency $f_{\max}$ where

$$A = \frac{K}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}} \tag{5}$$

and

$$f_{\max} = f_0\sqrt{1 - \frac{1}{2Q^2}} \tag{6}$$

which is a frequency smaller than f_0.

The proper selection of Q will produce any of the classical filter configurations such as Butterworth, Chebyshev, and Bessel. The choice of Q is given in Table 1.

Filter Type	**Pass-Band Ripple**	**Q**	f_c/f_0
Bessel	—	0.577	0.786
Butterworth	—	0.707	1.000
Chebyshev	0.1 dB	0.767	1.078
Chebyshev	0.2 dB	0.797	1.111
Chebyshev	0.3 dB	0.821	1.136
Chebyshev	0.5 dB	0.864	1.176
Chebyshev	1 dB	0.957	1.246
Chebyshev	2 dB	1.129	1.333
Chebyshev	3 dB	1.305	1.389

Table 1 Second-Order Low-Pass Filter Parameters

High-Pass Filter

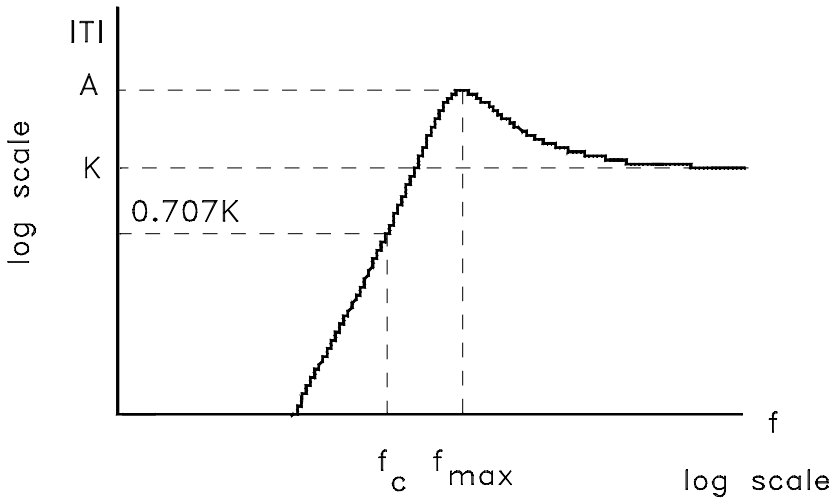

Figure 0-3 Second-order high-pass filter.

The complex transfer function for a second-order high-pass filter is

$$T(s) = K\frac{\left(\frac{s}{\omega_0}\right)^2}{\left(\frac{s}{\omega_0}\right)^2 + \frac{1}{Q}\left(\frac{s}{\omega_0}\right) + 1} \tag{7}$$

where K is the high-frequency gain of the filter, Q is the quality factor, and ω_0 is the resonant frequency of the filter. The magnitude of the complex transfer function is plotted in Fig. 0-3. The minus 3 dB, half-power, critical, or cutoff frequency f_c is the frequency at which the gain is reduced to $K/\sqrt{2}$ and is given by

$$f_c = \frac{f_0}{\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}} \tag{8}$$

which is a frequency smaller than f_0. The maximum value of the magnitude of the complex transfer function A occurs at the frequency $f_{\max}$ where

$$A = \frac{K}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}} \tag{9}$$

and

$$f_{\max} = \frac{f_0}{\sqrt{1 - \frac{1}{2Q^2}}} \tag{10}$$

which is a frequency larger than f_0.

Band-Pass Filter

The complex transfer function for the second-order band-pass filter is

$$T(s) = K\frac{\frac{1}{Q}\left(\frac{s}{\omega_0}\right)}{\left(\frac{s}{\omega_0}\right)^2 + \frac{1}{Q}\left(\frac{s}{\omega_0}\right) + 1} \tag{11}$$

where f_0 is the resonant frequency and also the center frequency, Q is the quality factor, and K is the gain at the center frequency. The plot of the magnitude of the complex transfer function as a function of frequency is shown in Fig. 0-4. This circuit has both an upper, f_U , and lower, f_L, half-power frequencies given by

$$f_U = f_0\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right) \tag{12}$$

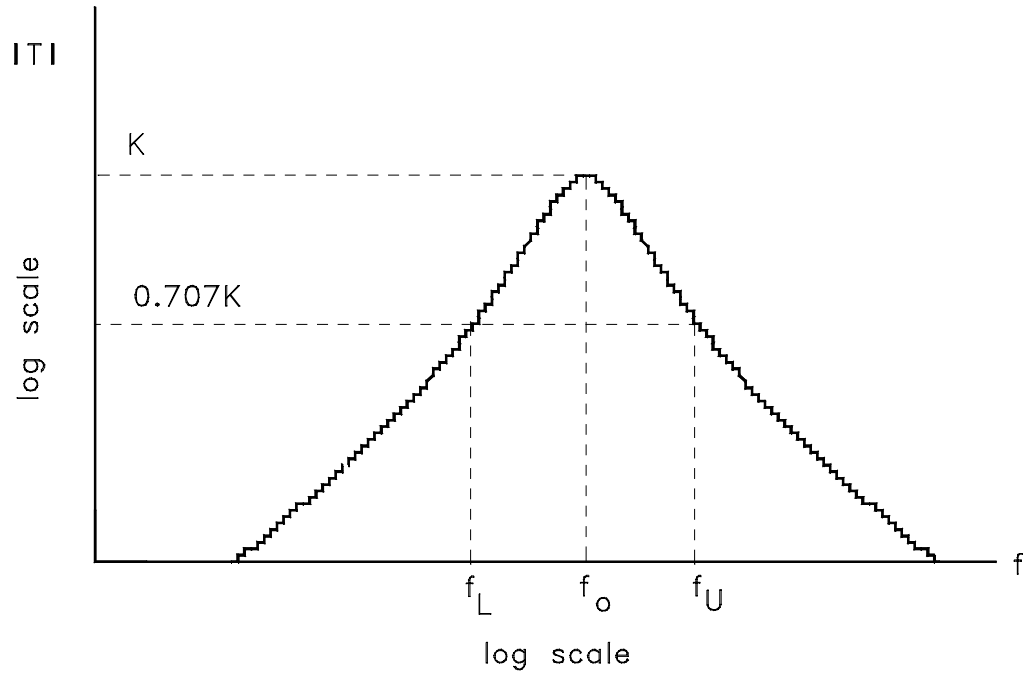

Figure 0-4 Band-pass filter.

and

$$f_L = f_0 \left(-\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right) \tag{13}$$

The difference between these two half-power frequencies is known as the half-power bandwidth, Δf, which is given by

$$\Delta f = f_U - f_L = \frac{f_0}{Q} \tag{14}$$

which reveals that

$$Q = \frac{f_0}{\Delta f} \tag{15}$$

which is the reason why Q is called the quality factor, i.e. the larger Q is the sharper the peak in the filter becomes. The center frequency is also the geometric mean of the half-power frequencies, i.e.

$$f_0 = \sqrt{f_U f_L} \tag{16}$$

Notch Filter

The complex transfer function of the second order notch filter is given by

$$T(s) = K \frac{\left(\frac{s}{\omega_0}\right)^2 + 1}{\left(\frac{s}{\omega_0}\right)^2 + \frac{1}{Q}\left(\frac{s}{\omega_0}\right) + 1} \tag{17}$$

where ω_0 is the notch frequency in radians/sec, Q is the quality factor, and K is both the high and low frequency gain. A plot of the magnitude of the complex transfer function for the notch filter is shown in Fig. 0-5.

All of the equations for the upper and lower half-power frequencies as well as the quality factor for the band-pass filter are equally applicable for the notch filter. This is because the transfer function of the notch filter, $T_N(s)$, is related to that of the band-pass filter, $T_B(s)$, by

$$T_N(s) = K - T_B(s) \tag{18}$$

Thus, either filter may be obtained by summing the other with a gain constant.

All-Pass Filter

The transfer function of the second-order all-pass filter is given by

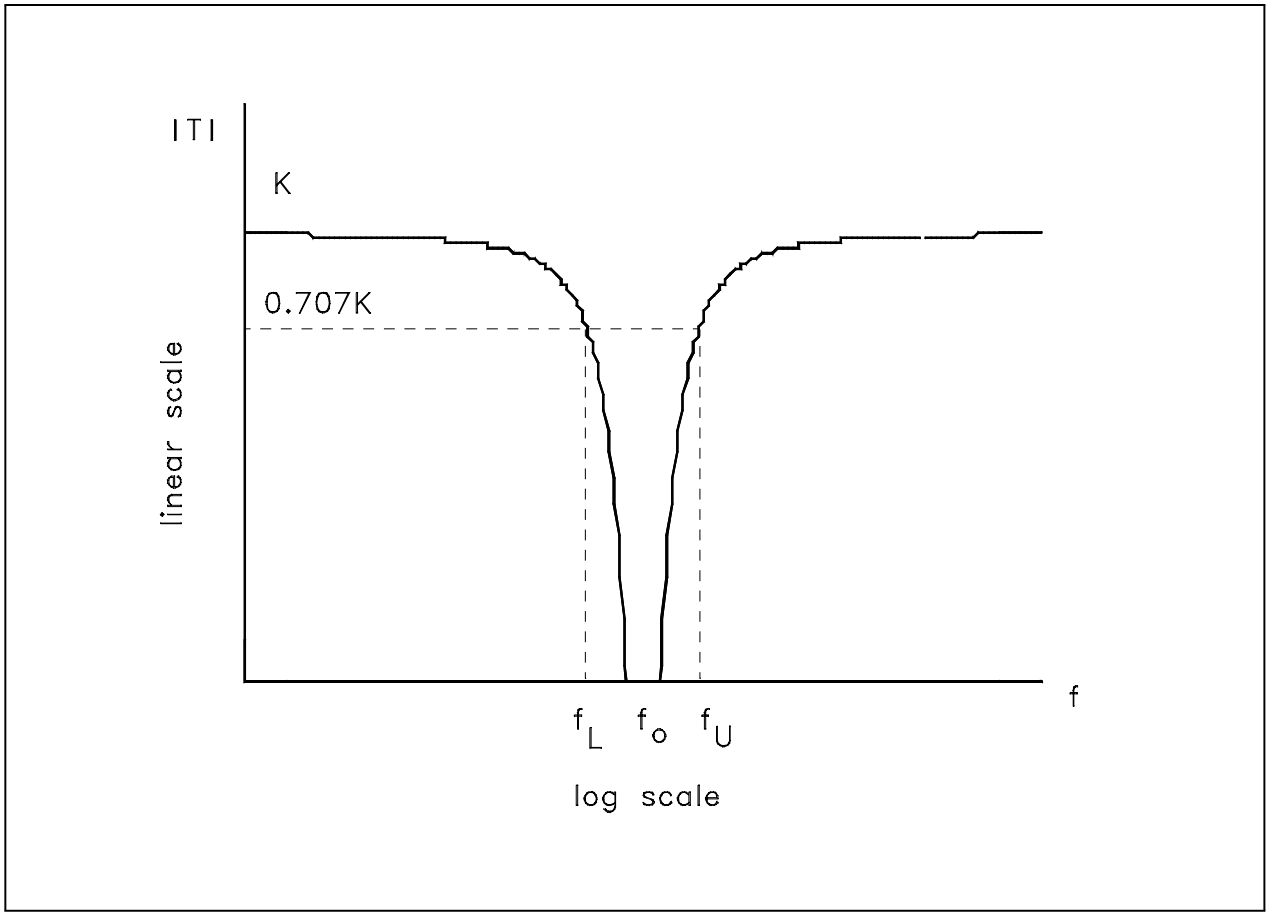

Figure 0-5 Notch filter.

$$T(s) = K\frac{\left(\frac{s}{\omega_0}\right)^2 - \frac{1}{Q}\left(\frac{s}{\omega_0}\right) + 1}{\left(\frac{s}{\omega_0}\right)^2 + \frac{1}{Q}\left(\frac{s}{\omega_0}\right) + 1} \tag{19}$$

which has a constant amplitude and a phase that varies with frequency. The magnitude of the complex transfer function is K at all frequencies whereas the angle of the complex transfer function is given by

$$\phi(j\omega) = \angle T(s)|_{s=j\omega} = -2\arctan\left[\frac{\frac{1}{Q}\frac{\omega}{\omega_0}}{1-\left(\frac{\omega}{\omega_0}\right)^2}\right] \tag{20}$$

Biquadratic Filter

The second order biquadratic filter has the complex transfer function

$$T(s) = K\frac{\left(\frac{s}{\omega_z}\right)^2 + \frac{1}{Q_z}\left(\frac{s}{\omega_z}\right) + 1}{\left(\frac{s}{\omega_p}\right)^2 + \frac{1}{Q_p}\left(\frac{s}{\omega_p}\right) + 1} \tag{21}$$

which has a DC gain of K and a high frequency gain of $K\left(\omega_p/\omega_z\right)^2$. A special case of the biquadratic filter is obtained by letting the quality factor for the numerator become infinite (which puts the zeroes on the imaginary axis as is the case for the notch filter)—these are known as elliptic filters. If $\omega_p > \omega_z$ it is a high-pass elliptic filter and if $\omega_p < \omega_z$ it is a low-pass elliptic filter (and, of course, if $\omega_p = \omega_z$ it is a notch filter). Elliptic filters feature the fastest transition from the pass to the stop band but, unlike the garden variety high- and low-pass filters, do not have a gain that is a monotonic function of frequency.

0.3 Devices

A plethora of switched capacitor devices are available as off-the-shelf integrated circuits from a variety of manufacturers. Prominent among these are the devices from Motorola which are primarily intended for telecommunications applications such as the MC145432 which features a six pole notch filter operated by a highly stable crystal oscillator internal clock or the MC145414 which is a fifth-order elliptic filter. Some filters are totally digital in that both the clock frequency and the filter parameters are directly set by input digital codes.

The device that will be employed in this experiment in the MF10 Universal Monolithic Dual Switched Capacitor Filter because it is the cheapest switched capacitor device available and it offers a degree of flexibility to the user. A functional block diagram is shown in Fig.

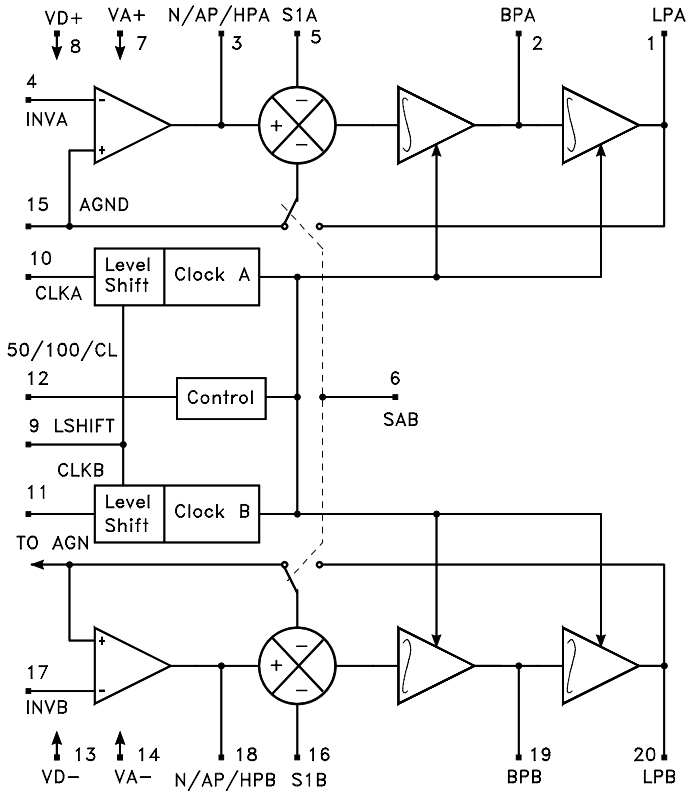

Figure 0-6 MF10 switched capacitor filter.

0-6. The square symbols indicate that these are pin numbers on the integrated circuit. It has two identical filters known and A and B. Separate clocks are provided for each of the two filters. The circuit components shown in this figure are internal to the integrated circuit. Each of the symbols show as a triangle with an integral symbol inside are switched capacitor integrators of the type discussed in 0.2.1. Because there are two integrators and op amp summers, this makes this a second order state variable filter.

The symbol with a one plus and two minus signs in a circle with an X is a summer with two inverting and one non-inverting inputs. One of the inverting inputs is a pin on the IC while the other is controlled by the S_{AB} input on pin 6; the position of this switch determines whether the feedback is closed around the input op amp or the triple input summer.

The level shift input on pin 9 determines the type of clock being used. This pin is grounded for TTL clock signals or $\pm$ 5 V CMOS clock signals. The same type of clock must be applied to both filter A and B but different frequency clocks may be used at the two inputs. The 50/100/CL input on pin 12 determines whether the critical frequencies are obtained as the clock frequency divided by 50 or 100 or whether the filter is turned off; if this pin is connected to the positive power supply the clock frequency is divided by 50, if it is grounded the clock frequency is divided by 100, and if it is connected to the negative supply filtration is inhibited.

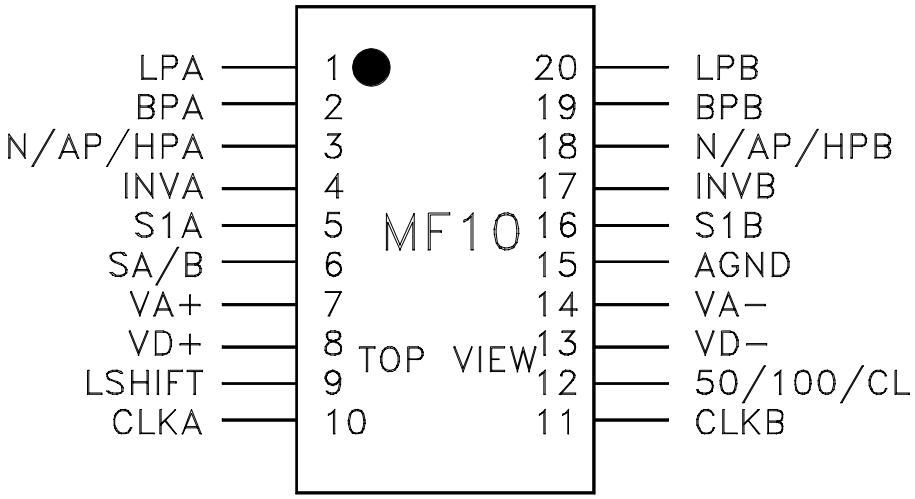

Figure 0-7 Pinouts for MF10

The pinouts for the MF10 are given in Fig. 0-7. A more complete description of this device is given in the manufacturer's data sheet in the appendix to this experiment. The notation used in the manufacturer's data sheet differs slightly from that used in this experiment.

The manufacturer defines several modes or circuit topologies for the MF10. The one that

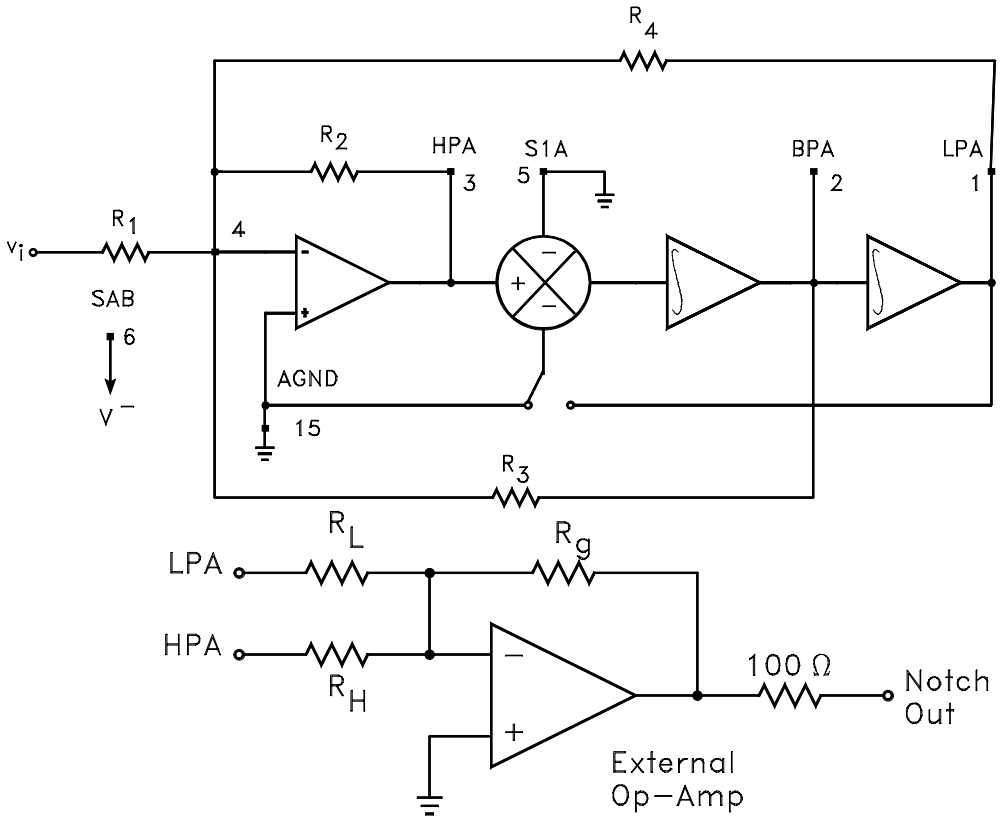

Figure 0-8 Mode 3A for MF10

will be used in this experiment is Mode 3a shown in Fig. 0-8. The resistors $R1$, $R2$, $R3$, and $R4$ are external resistors that are connected to the pins shown. There are three outputs low-, high-, and band-pass at pins 1, 3, and 2 respectively. One external op amp summer with resistors R_L, R_U,and R_g is used to sum the high- and low-pass outputs to produce a notch output. The input is v_i.

The resonant frequency f_0 is given by

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \qquad \text{or} \qquad \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}} \tag{22}$$

depending on whether the clock is being divided by 100 or 50; this is center frequency of both the band-pass and notch filter. The quality factor is given by

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2} \tag{23}$$

The DC gain of the low-pass filter is

$$K_{LP} = -\frac{R4}{R1} \tag{24}$$

The high-frequency gain of the high-pass filter is

$$K_{HP} = -\frac{R2}{R1} \tag{25}$$

The gain at the center frequency of the band-pass filter is

$$K_{BP} = -\frac{R3}{R1} \tag{26}$$

The gain of the notch filter at the notch frequency f_0 is given by

$$A_n = \left| Q \left(\frac{R_g}{R_L} K_{LP} - \frac{R_g}{R_H} K_{HP} \right) \right| \tag{27}$$

which would normally be picked to be zero. The gain of the notch filter at DC is

$$K_N = \frac{R_g}{R_L} \times K_{LP} \tag{28}$$

while the gain at the frequency which is half of the clock frequency is

$$K_{\frac{CLK}{2}} = -\frac{R_g}{R_H} \times K_{HP} \tag{29}$$

0.4 Experimental Procedures

0.4.1 Preparation

Prepare the electronic breadboard to provide buses for the positive and negative power supply rails and the circuit ground. Three power supplies will be used in this experiment: $+5\,\mathrm{V}$, and $-5\,\mathrm{V}$. Each power supply rail should be decoupled with a $100\,\Omega$, $25\,\mathrm{V}$ (or greater) capacitor. The resistors are connected in series with the external power supply leads and the capacitors are connected from the power supply rails to ground on the circuit side of the resistor. The capacitor must be installed with the proper polarity to prevent reverse polarity breakdown.

0.4.2 Clock

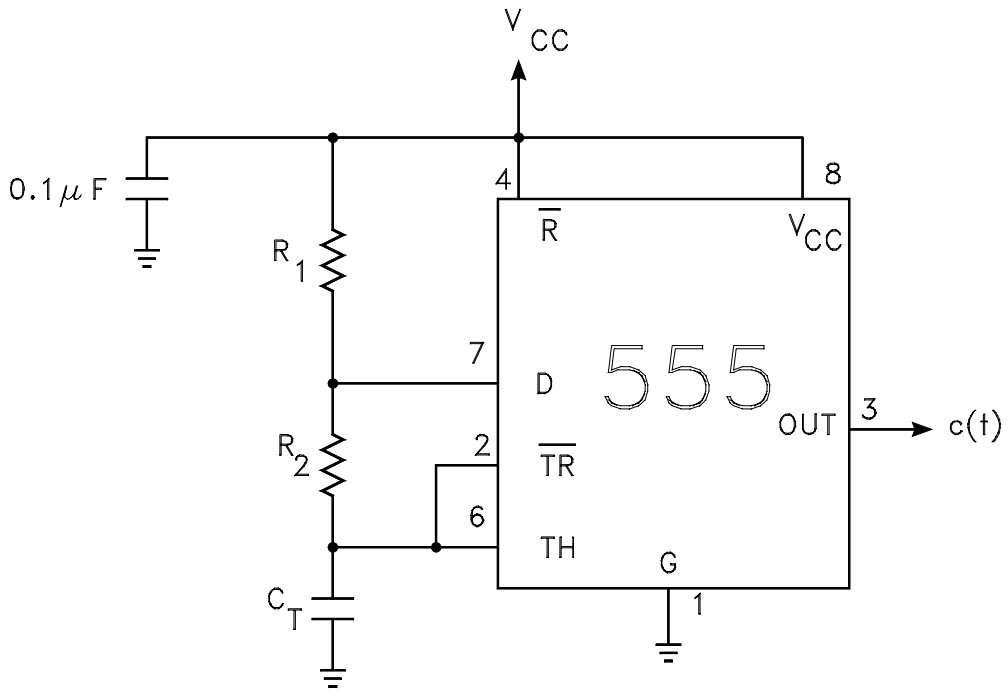

Figure 0-9 555/MC1555 Timer

The clock that will be used for the experiment in the MC1555/555 timer shown in Fig. 0-9. The power supply voltage for this IC will be + 5 V so that it will produce a TTL clock. The clock frequency is

$$f_{CLK} = \frac{1.44}{(R_1 + 2R_2)\, C_T} \tag{30}$$

and the duty cycle is

$$\text{Duty Cycle} = \frac{R_1 + R_2}{R_1 + 2R_2} \tag{31}$$

Design the timer so that the clock frequency is either $f_0 \times 100$ or $f_0 \times 50$. Pick the duty cycle to be close to 50%. The lower of the two frequencies is the most judicious choice; although the higher clock frequency would produces fewer glitches in the output of the filter, if the timer were operated at this high frequency on an untidy breadboard, the waveform might be distorted and degrade the performance of the filter.

0.4.3 Second-Order Filter

Assemble the second-order state variable filter shown in Fig. 0-8 using the component values computed in the preliminary calculations section with the power off. This is the mode of the filter labeled 3a by the manufacturer.

Pins 5, 9, and 15 should be connected to ground.

Pins 7, 8, and 12 should be connected to the positive power supply, +5 V. (Connecting pin 12 to the positive power supply sets the filter to the $f_{CLK}/50$ mode. If the $f_{CLK}/100$ mode is desired, pin 12 should be grounded.)

Pins 6, 13, and 14 should be connected to the negative power supply, −5 V.

Standard connections should be made for the external op amp. An LF351 would be a better choice than a 741 since the 741 requires power supply voltages of at least ±8 V which would incinerate the MF10.

The clock input is pin 3 of the MC1555 timer which is connected to pin 10 of the MF10 for filter A.

Turn the power on and measure the frequency response of the filter. Data should be taken of the four outputs as the frequency of the input is varied one decade above and below f_0.

Increase the frequency of the input until it is approximately equal to the clock frequency. Explain why the low- and band-pass outputs are nonzero in the laboratory report.

0.4.4 Fourth-Order Filter

Assemble the fourth-order filter with the characteristics specified by the laboratory instructor. This is obtained by cascading the two second-order filters found in the MF10. Repeat the measurement of the frequency response.