A Voltage Controlled Amplifier

In this circuit, you will need an n-channel JFET which is to be operated as a voltage variable resistor. The lab has a supply of 2N5457 JFETs which can be used for the experiment. In general, the JFET drain current is given by

$$i_D = \beta \left(v_{GS} - V_{TO} \right)^2$$

where β is the transconductance parameter and V_{TO} is the threshold voltage (which is negative). It will be necessary to know numerical values for β and V_{TO} for your JFET. This information can be obtained from the curve tracer. Dr. Brewer can assist with this.

The object of this experiment is to assemble and test a voltage controlled amplifier (VCA) that might be used as a variable gain stage in a compressor, a limiter, or a guitar effects box. The variable gain element in the VCA is a JFET operated in its linear or triode region. The basic circuit is shown in Figure 1. The drain-to-source voltage of the JFET is labeled v_A in the figure. It is given by

$$v_A = v_I \frac{R_2}{R_1 + R_2}$$

For op-amp circuits powered by $\pm 15\,\mathrm{V}$ power supplies, a practical upper limit on the peak input voltage might be taken to be $10\,\mathrm{V}$. For the JFET to be operated in its linear region, its drain-to-source voltage should not exceed V_{TO}, where V_{TO} is its threshold voltage (which is negative for the n-channel JFET). To be on the safe side, the limit might be taken to be $V_{TO}/2$. Thus, a design specification for the circuit is

$$|v_A|_{max} = 10 \frac{R_2}{R_1 + R_2} \leq \frac{|V_{TO}|}{2} \qquad \text{or} \qquad \frac{R_1}{R_2} \geq \frac{20}{|V_{TO}|} - 1$$

When the JFET is pinched off, i.e. when it is an infinite resistance, the circuit is to be designed so that it has a voltage gain that is 5% to 10% greater than unity (in the range of 1.05 to 1.10). This requires

$$1.05 \leq \frac{R_3}{R_1 + R_2} \leq 1.10 \qquad \text{or} \qquad \frac{R_3}{1.1} \leq R_1 + R_2 \leq \frac{R_3}{1.05}$$

When the JFET is operated in its linear region, it exhibits a resistance from its drain to source. Let this be denoted by r_{ds}. The gain of the circuit is given by

$$\frac{v_O}{v_I} = -\frac{R_3}{R_2} \frac{r_{ds} \| R_2}{R_1 + r_{ds} \| R_2}$$

Let the minimum value of r_{ds} be denoted by $r_{ds(min)}$. It is given by

$$r_{ds(\mathrm{min})} = \frac{1}{2\beta \left| V_{TO} \right|}$$

At this value, the circuit is to exhibit an attenuation that is 26 dB (a linear factor of 1/20) lower than the gain when the JFET is pinched off. This condition requires

$$\frac{R_3}{R_2} \frac{r_{ds(\mathrm{min})} \| R_2}{R_1 + r_{ds(\mathrm{min})} \| R_2} = \frac{1}{20} \frac{R_3}{R_2} \frac{R_2}{R_1 + R_2} \qquad \text{or} \qquad R_1 = \left[\frac{1}{19 r_{ds(\mathrm{min})}} - \frac{1}{R_2} \right]^{-1}$$

To solve for R_1 and R_2, assume a standard 5% value for R_3. Calculate the two values of R_2 for which

$$\left[\frac{1}{19r_{ds(\min)}} - \frac{1}{R_2}\right]^{-1} + R_2 = \frac{R_3}{1.1} \qquad \text{and} \qquad \left[\frac{1}{19r_{ds(\min)}} - \frac{1}{R_2}\right]^{-1} + R_2 = \frac{R_3}{1.05}$$

Calculate the corresponding values of R_1. Repeat for several 5% standard values of R_3 until values for both R_1 and R_2 that are closest to standard 5% values are obtained.

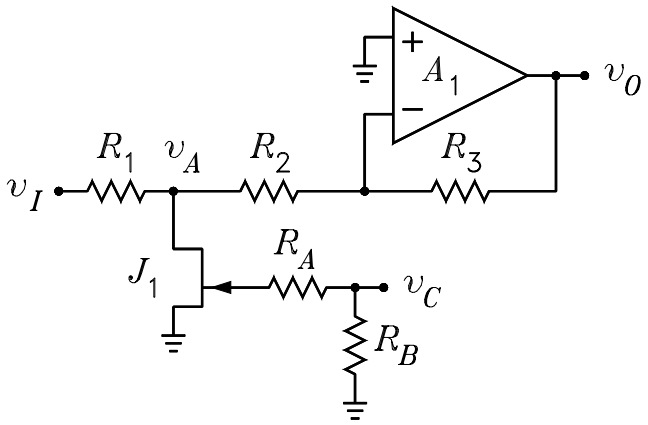

Figure 1: Basic VCA circuit.

Assemble the circuit using a TL071, TL081, or LF351 op amp. Use $R_A = R_B = 10\,\text{k}\Omega$. Apply a sine wave to the input and a negative dc voltage to v_C. Verify that that gain of the circuit can be varied between unity and 1/20 by varying v_C over the range $V_{TO} \le v_C \le 0$. Do not apply a dc voltage outside this range for the JFET could be damaged, and remember that V_{TO} is negative. If you have oscillation problems, put a small value capacitor (hopefully no larger than 10 pF to 20 pF) in parallel with R_3.

Once the circuit is operational, apply a triangle wave having a peak voltage of 10 V to v_I. Connect the x input to the oscilloscope to v_I and the y input to v_O. You should observe a straight line having some curvature on the oscilloscope whose slope at $v_I = 0$ can be varied approximately between -1 and $-1/20$ by varying v_C. Note and record the curvature in this line. This curvature adds undesired distortion to the signal which is to be eliminated in the next step.

The next step is to linearize the circuit to remove the curvature by feeding the voltage $v_A/2$ back into the JFET gate. A suitable circuit is shown in Figure 2. The output voltage of A_2 must be negative to prevent the flow of gate current in the JFET. When this is the case, the gate-to-source voltage of the JFET is given by

$$v_{GS} = v_A \frac{R_3}{R_2}\frac{R_6}{R_5} - v_C \frac{R_6}{R_4}$$

The resistors are to be chosen so that

$$v_{GS} = \frac{v_A}{2} - v_C$$

With R_5 chosen to be some convenient value (e.g. $R_5 = 10\,\mathrm{k}\Omega$), calculate values for R_4 and R_6. Use $R_7 = 10\,\mathrm{k}\Omega$. Note that there is no current through R_7 when $v_{GS} < 0$ so that this resistor has no effect on v_{GS}.

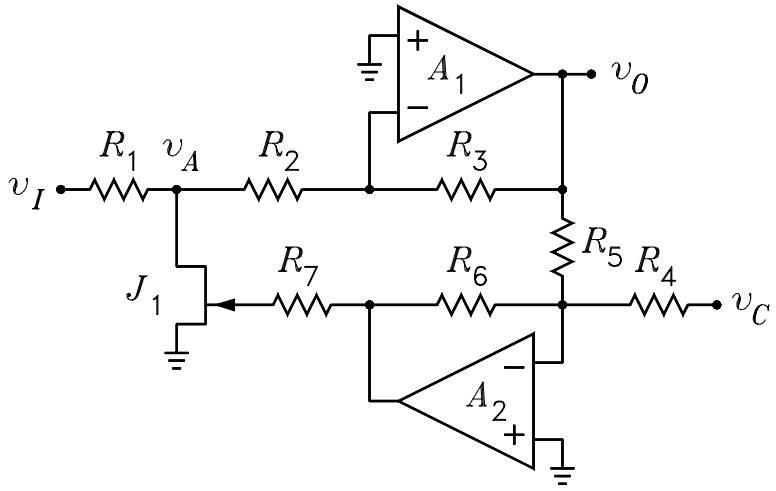

Figure 2: Circuit with the linearization voltage added to the JFET gate voltage.

Assemble the circuit in Figure 2 using the values calculated above. Note that v_C must be positive in this circuit because A_2 inverts the control voltage. Perform the same tests as for the circuit in Figure 2 and record the waveforms. In the following weeks, the VCA will be used as the control element in a compressor circuit. You should neaten up the circuit so that it occupies no more room on the electronic breadboard than is necessary. This is because the circuits to be added will occupy more area than this part of the experiment.