JFET Noise

1 Object

The objects of this experiment are to measure the spectral density of the noise current output of a JFET, to compare the measured spectral density to the theoretical spectral density, and to determine the lower flicker noise corner frequency below which excess noise generated by generation-recombination centers in the JFET intrinsic region dominates.

2 Theory

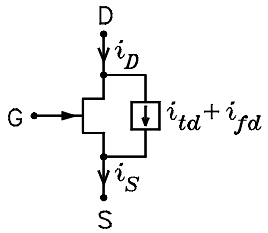


Figure 1: JFET noise equivalent circuit.

The noise equivalent circuit of a JFET is shown in Fig. 1, where $\overline{i_{td}^2}$ is the mean-square thermal drain noise current and $\overline{i_{fd}^2}$ is the excess or mean-square flicker noise current. These are given by

$$\overline{i_{td}^2} = 4kT\left(\frac{2g_m}{3}\right)\Delta f \tag{1}$$

$$\overline{i_{fd}^2} = \frac{K_f I_D}{f}\Delta f \tag{2}$$

where g_m is the small-signal transconductance and K_f is the flicker noise coefficient. The small-signal transconductance is given by either of the two relations

$$g_m = \frac{-2}{V_{TO}}\sqrt{I_D I_{DSS}} = 2\sqrt{\beta I_D} \tag{3}$$

where V_{TO} is the threshold or pinch-off voltage, I_D is the quiescent drain current, I_{DSS} is the drain-to-source saturation current, and β is the transconductance coefficient. In the active mode or saturation region, the drain current is given by either of the two relations

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{TO}}\right]^2 = \beta\left(V_{GS} - V_{TO}\right)^2 \tag{4}$$

I_{DSS} is related to β by

$$I_{DSS} = \beta V_{TO}^2$$

and β is a function of the drain-to-source voltage V_{DS} given by

$$\beta = \beta_0\left(1 + \lambda V_{DS}\right)$$

where β_0 is the value of β for $V_{DS} = 0$. For the n-channel JFET, both V_{GS} and V_{TO} are negative. The small signal transconductance g_m is positive.

The flicker noise coefficient K_f is related to the flicker noise corner frequency f_{flk} by

$$K_f = \frac{16kT}{3} f_L \sqrt{\frac{\beta}{I_D}} \tag{5}$$

Thus the mean-square flicker noise current can also be expressed as

$$\overline{i_{fd}^2} = 4kT\left(\frac{2g_m}{3}\right)\frac{f_L}{f}\Delta f \tag{6}$$

This illustrates that the flicker noise corner frequency f_{flk} is the frequency at which the mean-square thermal and flicker currents are equal in magnitude. Thus f_{flk} may be experimentally determined by measuring the frequency at which the total noise current increases by 3 dB over the value in the region at which thermal noise dominates, i.e. the region where the noise is flat or white.

3 Laboratory Procedure

3.1 Curve Tracer Measurements

Circuits can be biased with either the bench power supply or batteries. If the bench power supply is used, choose $V^+ = 15$ V and $V^- = -15$ V. For the batteries, $V^+ = 9$ V and $V^- = -9$ V.

Use the transistor curve tracer to measure I_D at $V_{GS} = 0$ for $V_{DS} = V^+/2$. If the JFET is in its saturation region, this drain current is I_{DSS}. Measure the channel length modulation factor. Pick a point on the characteristic and determine the threshold voltage.

3.2 Biasing

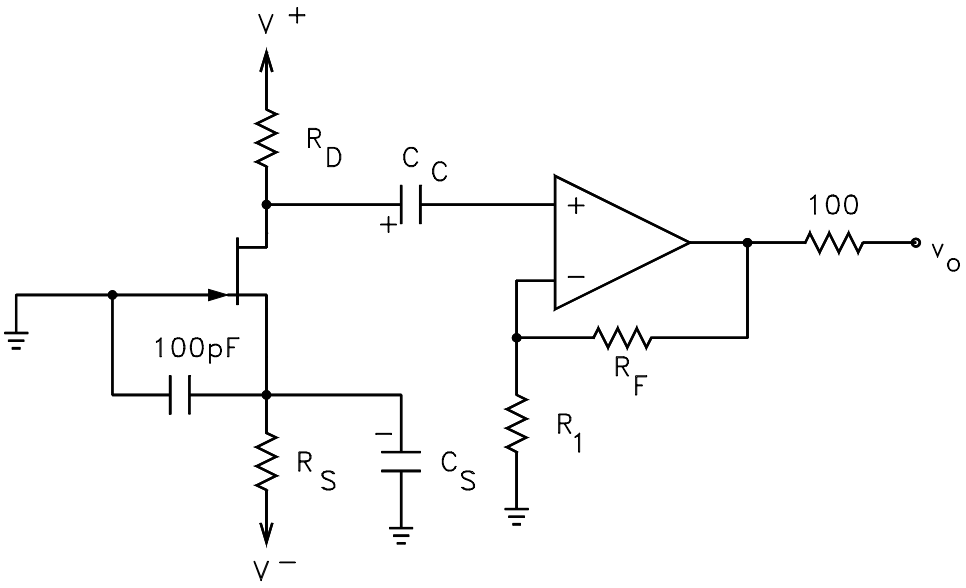
The circuit shown in Fig. **??** is the test circuit for measuring the JFET noise. When this circuit is assembled on the solderless breadboard, the power supply rails should be decoupled with a 100 Ω resistor and a 100 μF capacitor. If available, use batteries as the power supply and use the shielded boxes to enclose the breadboard. The JFET is to be operated at a drain-to-source voltage of $V^+/2$ and a drain current of $I_{DSS}/10$. For this current, the correct value of R_S is given by

$$R_S = \frac{-V^- - V_{GS}}{I_D} \tag{7}$$

where V_{GS} is the gate-to-source voltage for $I_D = I_{DSS}/10$. (Remember that both V^- and V_{GS} are negative for the n-channel JFET.) To bias the drain-to-source voltage at $V^+/2$, the correct value of R_D is given by

$$R_D = \frac{V^+/2 + V_{GS}}{I_D} \tag{8}$$

With the calculated values of R_S and R_D, assemble the circuit on the breadboard and verify that the bias current and voltages are correct, i.e. that they are within 5% of the design values.



JFET Noise Measurement.

Make the gain of the op amp stage 101. Use $C_S = 330\,\mu$F and $C_C = 10\,\mu$F.

3.3 Frequency Response

Experimentally determine the frequency response of the JFET and op amp in combination. To do this, disconnect the short from the gate to ground, place a resistor (10 kΩ) from the gate to ground and connect the function generator output to the gate. The theoretical value of the voltage gain is

$$A_v = \frac{V_o}{V_g} = -g_m R_F \tag{9}$$

where V_g is the generator voltage. Note that the amplitude of V_g must be small enough so that the output is not distorted.

Assemble the circuit again as shown in Fig. **??**. Namely, remove the function generator and resistor from the gate and connect the gate to circuit ground.

3.4 Background Noise, JFET Noise, and Corner Frequency

After it has been verified that the circuit is functioning properly, remove the JFET from the circuit and connect the Dynamic Signal Analyzer to the output of the op amp. Using a total analysis band of 100 kHz, measure the spectrum of the background noise generated by R_D, R_F, R_1, and the op amp. After doing this, reconnect the JFET to the circuit and measure the noise spectrum. For accuracy in the calculations, the noise with the JFET should be several dB higher than the noise without the JFET. If it is not, a larger op amp gain should be used, as long as the circuit does not oscillate. From the spectrum obtained, decide on an optimum frequency to measure the noise so that the midband white noise generated by the JFET is not affected by excess or flicker noise. Plot the spectrum obtained. From the display, determine the flicker noise corner frequency f_{flk} at which the noise voltage increases by 3 dB from the value in the white noise region.

4 Laboratory Report

4.1 Formula Verification

Verify the formulas for g_m, R_S, and R_D that are given in the **THEORY** and **PROCEDURE** sections.

4.2 Comparison of Experimental and Theoretical Spectra

Compare the measured noise spectral densities for the white noise region of the spectrum to that predicted by the theoretical formula for $\overline{i_{td}^2}$. What is the lower corner frequency below which the excess noise dominates? A major source of error in this calculation is the excess noise in the measurement system. If this dominates, the excess noise generated by the JFET may be difficult to determine.

4.3 Computation of $\overline{v_n^2}$

Reflect the $\overline{i_{td}^2}$ and $\overline{i_{fd}^2}$ noise sources to the JFET gate and compute $\overline{v_n^2}$. Use the experimental data from 3.3 of the procedure. (Divide the voltage at the output of the op amp by $g_m R_F$

to obtain $\sqrt{\overline{v_n^2}}$.) Compare the experimental values with the theoretical values predicted by the equation

$$v_n^2 = \frac{\overline{i_{td}^2} + \overline{i_{fd}^2}}{g_m^2} = 4kT\left(\frac{2}{3g_m}\right)\Delta f + \frac{K_f I_D \Delta f}{g_m^2 f} \tag{10}$$