

## Low-Noise Monolithic Amplifier Design: Bipolar versus CMOS

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**Abstract.** Design of monolithic low-noise amplifiers in bipolar and CMOS technologies for matching a given signal source is presented. Noise matching conditions are derived for three different types of source impedance, i.e., resistive, capacitive, and inductive. Emphasis is put on the comparison of the best noise performance obtainable by the use of bipolar and CMOS approaches. It is shown that for a resistive source, low-noise amplifiers can easily be designed in both bipolar and CMOS technologies. While for capacitive and inductive sources, a CMOS approach yields better noise performance than a bipolar one. Measurement and simulation results on some amplifiers are presented which confirm the theoretical considerations.

### 1. Introduction

It is a well known fact that noise in an integrated circuit (IC) determines the ultimate accuracy with which the IC can process weak signals without significant deterioration in the signal quality. Therefore, low-noise design forms one of the most important design objects for low-level signal processing ICs such as transducer interface circuits. AM/FM receivers, detector readout electronics, etc. Although the noise performance of such systems depends in general on the noise behavior of the basic building blocks comprising the systems, low-noise design in practice is focused on the front end circuits of the systems. Because in a well designed system the system noise performance is always dominated by the noise performance of the preamplifier.

For a given signal source, the noise performance of the preamplifier is determined by two factors, i.e., the noise generated within the amplifier itself and the signal impedance seen by the amplifier input. This means that low-noise amplifier design generally constitutes two steps. First, design the amplifier input stage in such a way that an optimal noise matching is obtained for the given source impedance. Secondly, design the rest of the amplifier so that their noise contributions are kept sufficiently lower with respect to the input stage. Noise matching is concerned with optimal choice of the basic design parameters of the input stage so that the total equivalent input noise is minimal for the given signal source impedance. The second step involves minimizing transfer functions associated with each signal source and thus relies on deep insights into the circuit

response with respect to each noise source. Circuit techniques, such as emitter or source degeneration in current sources [1], [2], adding a dc bypass to the input stage [3], inserting an emitter follower in the places where current noise is dominant [4], etc., are essential for accomplishing the second step.

It is important to note that monolithic noise matching differs from the classical discrete one in the methods of approach. In discrete realizations, noise matching has been obtained by such means as transformer coupling, input reactive tuning, paralleling several specially selected input devices such as low-noise JFET transistors [5], [6]. In the monolithic case, optimal noise matching can only be obtained by the appropriate choice of transistor dimensions and dc bias conditions. The inconsistency of the classical noise matching methods with the monolithic approaches makes low-noise monolithic amplifier design very cumbersome. In this paper, detailed noise analyses and some circuit techniques are presented for low-noise amplifier design using bipolar or CMOS technologies.

In section 2, the noise behaviors of MOS and BJT transistors are reviewed from the practical design point of view. Emphasis is put on the relationships of each noise source to the process and design parameters. Based upon the noise models, general noise matching conditions are derived for three possible source types (i.e., resistive, capacitive, and inductive) in the three subsequent sections. These noise matching conditions enable circuit designers to design the amplifier input stage so as to obtain the best noise performance. Design examples will be given to verify the analytical results.

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2. Noise sources in MOSFET and BJT

2.1. Noise Sources in MOS Transistors

To better understand the monolithic noise matching mechanism, it is desirable to review the basic noise characteristics of MOSFET and BJT transistors. In a MOS transistor, the two well known noise sources are the thermal noise associated with the inverse conducting channel and the 1/f noise. On the basis of the elementary MOS theory and Nyquist theorem, it can easily be calculated that the short circuit drain current noise spectral density under saturation condition is given by [7], [8]:

$$i_d^2 = 4kT \frac{2}{3} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) = 4kT \frac{2}{3} g_m \quad (1)$$

where  $k$  is the Boltzman constant,  $T$  is the absolute temperature and  $g_m$  is the transconductance of the MOSFET. Since the transconductance  $g_m$  depends on the  $W/L$  ratio and the dc bias current  $I_{DS}$ , the channel thermal noise can be minimized by a proper choice of these two design parameters.

In contrast to the channel thermal noise, the mechanism involved in the 1/f noise has not been fully understood. A large number of theoretical and experimental studies show that the 1/f noise in MOSFET is caused by the random trapping and detrapping of the mobile carriers in the traps located at Si-SiO<sub>2</sub> interface and within the gate oxide. On the basis of this model, it can be calculated that the short circuit drain current noise spectral density under saturation condition is given by [9]:

$$i_d^2(f) = \frac{\mu q^2 I_{DS}}{L^2 C_{ox}} \frac{k T N_t}{\alpha f} \frac{1}{16} \ln \left[ \frac{\sqrt{2} n_{so}}{n_i} \right] = \frac{K_F I_{DS}}{C_{ox} L^2 f} \quad (2)$$

where  $K_F$  is a technological dependent constant proportional to the effective trap density  $N_t(F_n)$ . Dividing (2) by the square of the transconductance, the equivalent input 1/f noise can easily be calculated as given by

$$v_i^2(f) = \frac{K_F}{2\mu C_{ox}^2 W L f} = \frac{K_f}{C_{ox}^2 W L f} \quad (3)$$

From a circuit design point of view, it is important to note that the 1/f noise voltage depends only on the gate area and is independent of any dc bias parameters.

In addition to the channel thermal and the 1/f noise, MOS transistors exhibit also parasitic noise due to the resistive poly-gate and substrate resistance. These parasitic noise sources can be taken into account by intro-

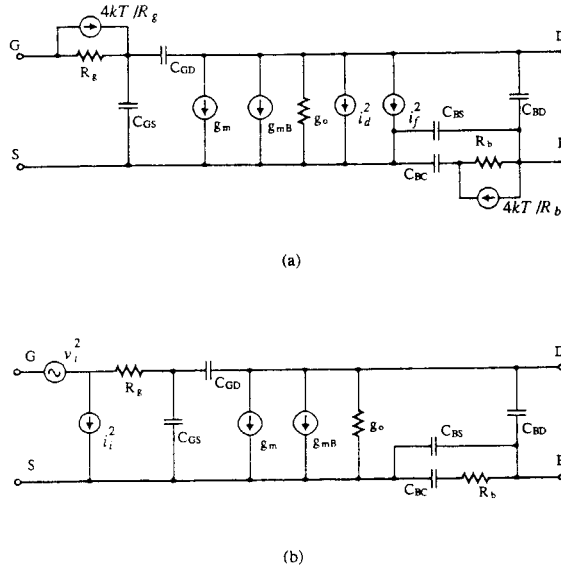


Fig. 1. (a) Small signal noise model of MOS transistor. (b) The equivalent input noise generator model.

ducing two white noise generators  $4kT/R_g$  and  $4kT/R_b$  in the small signal schema of a MOS transistor as shown in figure 1a. Since the equivalent poly-gate resistance  $R_g$  and substrate resistance  $R_b$  depend mainly on the layout structure of MOS transistors, good layout techniques are of great importance [9].

For sake of convenience for noise analyses, the equivalent input noise generator models are widely used. These models are based on the fact that the noise performance of any two port network can be represented by two equivalent noise generators at the input port of the network [10]. For a MOS transistor this representation is shown in figure 1b. The two equivalent input noise generators are calculated from figure 1a as given by

$$v_i^2 = \frac{(i_d^2 + i_f^2 + i_{dB}^2)}{|g_m - j\omega C_{GD}|^2} + 4KTR_g \quad (4)$$

$$i_i^2 = |j\omega(C_{GS} + C_{GD})|^2 \frac{(i_d^2 + i_f^2 + i_{dB}^2)}{|g_m - j\omega C_{GD}|^2} \quad (5)$$

where  $i_{dB}^2$  represents the noise contribution of the substrate resistance and is given by  $i_{dB}^2 = 4kTR_b g_{mB}^2$ . Since  $g_m/2\pi C_{GD}$  is much higher than the transistor cut-off frequency  $f_T$ , the term  $j\omega C_{GD}$  can be neglected with respect to  $g_m$  for all practical cases of interest. It is important to note that the first term of  $v_i^2$  and  $i_i^2$  depends on the same set of noise sources, which means that these two terms are 100% correlated.

2.2. Noise Source

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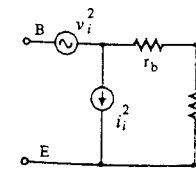
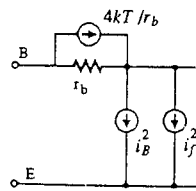


Fig. 2. (a) Small signal noise model of BJT transistor. (b) Equivalent input noise generator model for BJT transistor.

2.2. Noise Sources in BJT Transistors

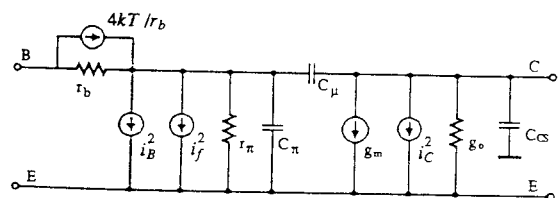
In contrast with a MOSFET transistor where the drain source current  $I_{DS}$  is dominated by the drift current under the  $\text{SiO}_2$  surface, the current in a bipolar junction transistor is mainly composed of diffusion currents within the bulk of the device. The difference in the basic conduction mechanism between both kinds of device results in differences in noise mechanism associated with the terminal currents. So, for instance, the noise associated with the base and collector current in a BJT transistor is of the shot noise type and they are given by

$$i_B^2 = 2qI_B \quad (6)$$

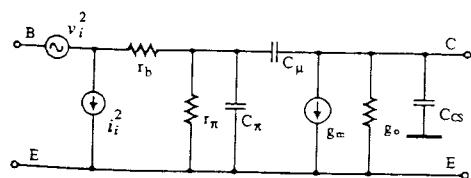
$$i_C^2 = 2qI_C \quad (7)$$

Furthermore, due to the bulk conduction mechanism, the  $1/f$  noise in BJT transistors has been found to be several order of magnitudes lower than that in MOS transistors. Therefore, in most cases, the  $1/f$  noise can be neglected in noise calculations.

BJT transistors show also thermal noise due to the series resistances associated with three terminals. For practical low noise design, the effect of the emitter and collector resistances can always be neglected with respect to the base resistance. With this approximation, the noise behavior of a BJT transistor can be described by the network as shown in figure 2a. The corresponding equivalent input noise generator model is given in



(a)



(b)

Fig. 2. (a) Small signal noise model of BJT transistor. (b) The equivalent input noise generator model.

figure 2b. Under the assumption that the base resistance is small with respect to  $r_\pi$  the two equivalent noise generators are given by [9]:

$$i_i^2 = i_B^2 + i_f^2 + \frac{i_C^2}{\beta_o^2} \left| 1 + \frac{j\omega}{\omega_\beta} \right|^2 \quad (8)$$

$$v_i^2 = i_f^2 r_b^2 + 4kT \left( r_b + \frac{1}{2g_m} \right) \quad (9)$$

where  $i_f^2$  represents the  $1/f$  noise power spectrum,  $\beta_o$  the dc value of  $\beta$  and  $\omega_\beta = 1/r_\pi (C_\pi + C_\mu)$ , which is related to the transistor cut off frequency  $f_T$  by:  $\omega_\beta = 2\pi f_T/\beta_o$ .

It is important to note that only at very low frequencies, where the  $1/f$  noise dominates, and at very high frequencies, where transistor current gain  $\beta(j\omega)$  falls off, the correlation effects are significant. In the middle frequency range, the correlation is not important so that it can be neglected which results in dramatic simplification in noise calculations.

3. Low-Noise Amplifiers with Resistive Sources

On the basis of the equivalent input noise generator models derived for MOSFETs and BJTs, low-noise design of bipolar and CMOS amplifiers can be easily performed. Since the noise performance of amplifiers depends strongly on the impedance of the signal source, design efforts will depend on the type of source impedance. In this section, the noise performance and optimization are presented of transimpedance amplifiers with a resistive source, which is the simplest type of source impedances.

Transimpedance amplifiers are widely used to amplify a signal current coming from a high impedance source [11], [12]. The basic feedback configuration and its associated noise sources are shown in figure 3. It is easily seen that to guarantee the loop stability the

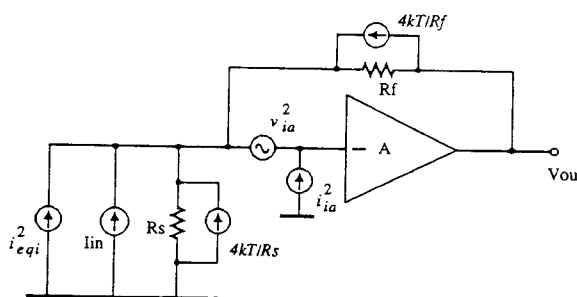


Fig. 3. Noise sources in transimpedance amplifier with a resistive source.

core amplifier A must have an opamp transfer characteristic. Also, as long as the loopgain is much larger than unity, the transimpedance (i.e.,  $V_{out}/I_{in}$ ) is simply given by the feedback resistance  $R_f$ , independent of the source impedance.

Since the signal is in a current form, the noise performance of a transimpedance amplifier is generally described by the total equivalent input current noise in parallel with the current source  $I_{in}$ . Taking into account all noise sources, the total equivalent input current noise  $i_{eqi}^2$  is easily calculated as given by

$$i_{eqi}^2 = \frac{4kT}{R_s} + \frac{4kT}{R_f} + i_{ia}^2 + \frac{v_{ia}^2}{(R_s // R_f)^2} + 2Re \left\{ i_{ia}^* \frac{v_{ia}}{R_s // R_f} \right\} \quad (10)$$

where the last term represents the correlation effect of the voltage and current noise generators of the core amplifier. Depending on the type of technology used, the above expression can explicitly be written as functions of the basic design parameters of the input device.

### 3.1. BJT Technology

In this case, neglecting the  $1/f$  noise and the correlation effect of the two equivalent input noise generators, the general expression (10) becomes:

$$i_{eqi}^2 = \frac{4kT}{R_s // R_f} + \frac{2qI_C}{\beta} + \frac{2qI_C}{\beta^2} \left( 1 + \frac{\omega^2}{\omega_B^2} \right) + \frac{4kTr_b}{(R_s // R_f)^2} + \frac{2(kT)^2}{qI_C(R_s // R_f)^2} \quad (11)$$

From this expression, some general conclusions can be drawn for low-noise transimpedance amplifiers design. First, the noise current of the feedback resistance  $R_f$  contributes directly to the total input current noise and this noise contribution can always be kept lower than that of the source resistance  $R_s$  by choosing  $R_f > R_s$ . Secondly, the noise contribution of the base resistance  $r_b$  of the input BJT transistor is not significant as long as  $r_b \ll R_f // R_s$ . The key issue in minimizing the base and collector shot noise contributions is the optimal choice of the collector bias current  $I_C$ . Neglecting the frequency dependent term, the optimal collector current can easily be obtained from (11) as given by

$$C_{C_{opt}} = \frac{kT}{q} \sqrt{\beta} \frac{1}{R_s // R_f} \quad (12)$$

$\uparrow$   
 $I_{C_{opt}}$

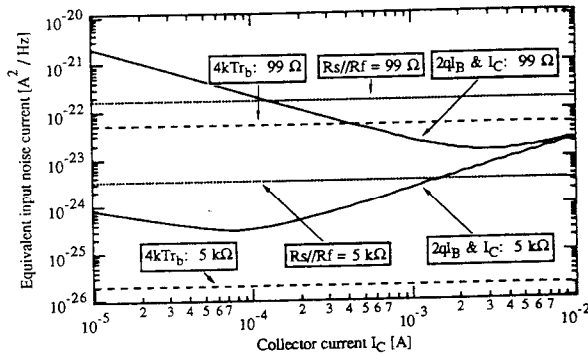


Fig. 4. Effect of collector current on the noise performance of transimpedance amplifiers.

Under this optimal bias condition, the noise contributions due to base and collector shot noise are given by  $4kT/(R_f // R_s \sqrt{\beta})$ , which is a factor  $1/\sqrt{\beta}$  lower than the noise of  $R_f // R_s$ . Therefore, it can be concluded that the noise performance of transimpedance amplifiers with a resistive source can always be made to be dominated by the resistive source itself. This is illustrated in figure 4 for two cases of source resistances. The upper three curves are for the case  $R_f // R_s = 99$  Ohm. The  $4kTr_b$  represents the contribution of  $r_b$ ;  $R_f // R_s$  the one of the resistors, and  $2qI_B \& I_C$  one of the base and collector current of the transistor. As can be seen the  $4kTR_s // R_f$  noise dominates by far the amplifier noise above biasing currents in the range 100  $\mu$ A up to 10 mA. The three lower three curves are for the case  $R_f // R_s = 5$  kOhm. Also in this case the  $4kTR_s // R_f$  noise dominates by far the amplifier noise in a wide biasing range, namely from 10  $\mu$ A up to 1 mA. Furthermore, for both cases the minimum of  $2qI_B \& I_C$  curve is a factor  $1/\sqrt{\beta}$  lower than the noise  $4kTR_s // R_f$ .

### 3.2. CMOS Technology

For the case of a MOSFET input, the general noise expression (10) can be by virtue of (4) and (5) explicitly written as:

$$i_{eqi}^2 = \frac{4kT}{R_s // 9R_f} + \left( \frac{8}{3} kT \frac{1}{g_m} + \frac{K_f}{C_{ox}^2 WLf} \right) \frac{[1 + (\omega C_{in} R_s // R_f)^2]}{(R_s // R_f)^2}$$

where the  $\omega C_{in} R_s // R_f$  term is the result of the equivalent input current noise generator of the MOS input. Since the bandwidth of the transimpedance amplifier must be lower than the  $\omega_{-3dB} < 1/C_{in} R_s // R_f$  due to the

stability constraint, the noise performance of the amplifier (13) the contribution of the feedback resistance is omitted. As (13) shows, the noise contribution of the feedback resistance is negligible. As (13) shows, the noise contribution of the feedback resistance is negligible. As (13) shows, the noise contribution of the feedback resistance is negligible.

### 4. Low-Noise A

In many applications, the noise performance of a photodetector system is often limited by the noise of the feedback resistor. In the first case, the noise of the feedback resistor can be represented by a voltage source. For such applications, the noise of the feedback resistor dominates the sensitivity of the front end circuit.

The front end circuit can be represented by a capacitive feed

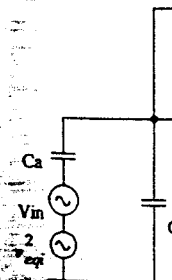


Fig. 5. Feedback topology with a resistive source.

stability constraint, the effect of this term on the amplifier noise performance is not significant. Note that in (13) the contributions of poly-gate and substrate resistance is omitted, as they are mainly concerned with layout techniques.

As (13) shows, the noise contribution of the core amplifier is inversely proportional to  $(R_s // R_f)^2$ . Therefore, for a large source resistance, the core amplifier noise contribution can easily be made negligible with respect to that of the source resistance, making a MOS input preferable to a BJT input. For a low source resistances, the thermal noise contribution of the core amplifier can be minimized by choosing an input MOSFET with a minimal channel length and a maximal channel width, and using a dc bias current as high as possible. Practically, the channel thermal noise contribution is less than that of  $R_s // R_f$  if the following condition is met:  $1.5g_m R_s // R_f > 1$ . Since the  $1/f$  noise depends only on the transistor dimensions, the only way to reduce the  $1/f$  noise contribution is to increase the gate area  $WL$ .

#### 4. Low-Noise Amplifiers with Capacitive Sources

In many applications such as car radio receivers and photodetector systems, the electrical signals to be processed are obtained by a signal conversion in a capacitive source. In the first case, the signal source is the capacitive antenna while in the second case it can be a photo sensitive diode. The network equivalent of such sources can be represented by a current signal source in parallel with or by a voltage signal source in series with a capacitor. For such applications, the noise performance of the front end circuits are of a great importance, as it determines the sensitivity or the resolution of the systems.

The front end amplifier for both applications uses a capacitive feedback configuration as shown in figure 5

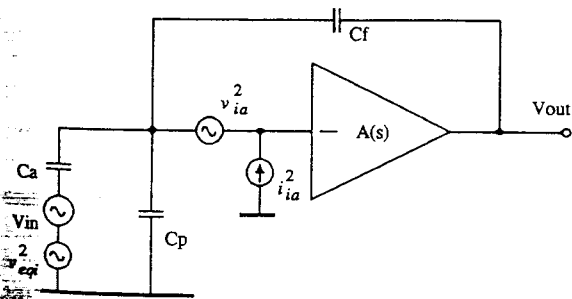


Fig. 5. Feedback topology and noise model of amplifier with capacitive source.

to obtain the best noise performance.  $C_s$  can be the capacitance of an antenna or the junction capacitance of a detector,  $C_p$  is the parasitic capacitance and  $C_f$  is the feedback capacitance. Since the capacitances do not generate any noise, the noise performance of the amplifier is determined by the noise contributions of the two noise generators of the core amplifier. Irrespective of what type of input transistor is used, the total equivalent input noise voltage is given by

$$v_{eqi}^2 = \left[ \frac{C_a + C_p + C_f}{C_a} \right]^2 v_{ia}^2 + \left| \frac{1}{j\omega C_a} \right|^2 i_{ia}^2 + 2 \operatorname{Re} \left\{ \frac{C_a + C_p + C_f}{C_a} v_{ia} \frac{i_{ia}^*}{-j\omega C_a} \right\} \quad (14)$$

where the last term accounts for the correlation effect between the two equivalent input noise generators. Depending on the type of technology used, the above expression can explicitly be written as functions of the basic design parameters of the input device.

##### 4.1. BJT Input Stage

Filling the expressions for the two equivalent input noise generators of a BJT in (14), the above equation is explicitly expressed as

$$v_{eqi}^2 = \left[ \frac{C_a + C_p + C_f}{C_a} \right]^2 4kT \left( r_b + \frac{kT}{2qI_C} \right) + \left| \frac{1}{j\omega C_a} \right|^2 \frac{2qI_C}{\beta} \quad (15)$$

As is generally the case, to minimize the noise contributions of the base resistance and the base shot noise, the input transistor must be designed to have a small base resistance  $r_b$  and a large current gain  $\beta$ . Since for a given technology the base resistance is mainly concerned with layout techniques, good layout such as the use of a multibase configuration is of considerable importance. Under the normal operating conditions the current gain  $\beta$  is more or less constant and depends only on technological parameters so that little can be done about it by circuit designers. On the other hand, the collector bias current is a free parameter for circuit designers. Therefore, the noise optimization is equivalent to the optimization of the collector current. By taking the derivative of (15) with respect to  $I_C$  the optimal collector current is obtained:

$$I_{C_{opt}} = \frac{kT}{q} \omega (C_a + C_p + C_f) \sqrt{\beta} \quad (16)$$

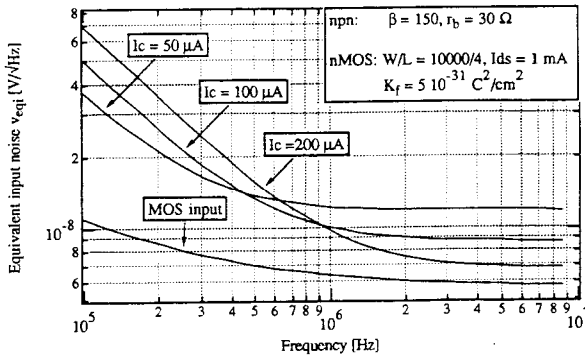


Fig. 6. Equivalent input noise spectrum for bipolar and MOS input.

In contrast with the case of resistive source, the optimal collector current is not constant and is directly proportional to the frequency. This makes it inadequate for realizing noise matching within a wide frequency band as is required for wide-band radio receivers [3], [13].

Figure 6 gives the equivalent input voltage noise density  $v_{eqi}$  for three collector bias currents. This figure is made for a practical radio receiver where  $C_a = 15$  pF,  $C_p = 60$  pF and  $C_f = 7.5$  pF. Clearly, a lower noise density at the lower frequency end corresponds always with higher noise density at the high frequency end and vice versa. At low frequencies the noise comes mainly from the base shot noise, while at the high frequency end the equivalent voltage noise generator turns out to be dominant. As a result, in order to minimize the equivalent input noise density in the whole frequency band, a compromised collector current of about  $50 \mu\text{A}$ – $100 \mu\text{A}$  should be chosen.

#### 4.2. CMOS Input Stage

In this case, the general expression (14) is reduced to

$$v_{eqi}^2 = \left[ \frac{C_a + C_p + C_f + C_{in}}{C_a} \right]^2 v_{ia}^2 \quad (17)$$

where  $C_{in} = C_{GSI} + C_{GDI}$  is the input capacitance of the core amplifier. Note that the factor  $C_{in}$  in the above equation is the result of the correlation effect between the two equivalent input noise generators of MOS transistors. Compared to the BJT case the frequency dependent term in  $1/j\omega C_a$  disappears in (17). It can thus be expected that in the CMOS case, the noise matching can be realized is a wide frequency band.

Since the  $1/f$  noise in a MOS transistor can be significant up to MHz range, both thermal and  $1/f$  noise must be taken into account in the noise optimization.

In order to avoid too elaborate calculation, each noise source is optimized separately. The key issue in optimizing the channel thermal noise and the  $1/f$  noise is the optimal choice of the input transistor dimensions to match the source capacitance. For the thermal noise, it can be shown that an optimal gate width exists for which expression (17) is minimal [9]:

$$W_{opt} = \frac{C_a + C_p + C_f}{2C_{ox}\alpha L} \quad (18)$$

where  $\alpha$  is defined as  $\alpha L = (L + 3L_D)$ ,  $L_D$  is the underdiffusion. For long channel devices the value of  $\alpha$  is always close to unity, as  $L_D$  is much smaller than the effective channel length  $L$ . Equation (18) is the general noise matching condition for CMOS amplifiers with capacitive sources. It is important to realize that this noise matching condition is equivalent to the condition  $C_{in} = (C_a + C_p + C_f)/3$ . This interpretation is found to be more convenient for detector readout applications which emphasize the matching requirement of the input capacitance to the detector capacitance. Fill the optimal gate width in (17), the corresponding minimal equivalent input thermal noise voltage is obtained as given by

$$v_{eqimin}^2 = \left[ \frac{4}{3} \frac{C_a + C_p + C_f}{C_a} \right]^2 \frac{8}{3} kT \frac{\sqrt{\alpha} L}{\sqrt{\mu I_{DS}(C_a + C_p + C_f)}} \quad (19)$$

Expression (19) is the theoretical minimal equivalent input thermal noise level that can be achieved by using a CMOS technology. For a given capacitive source (i.e.,  $C_a$  and  $C_p$ ), its lower limit is determined by the minimal gate length  $L$  and the maximal possible dc bias current of the input transistor. In addition, a nMOS input device is preferred to a pMOS due to its high mobility.

For the  $1/f$  noise, it can be shown that an optimal gate area  $WL_{opt}$  exists for which the  $1/f$  noise contribution is minimal.

$$WL_{opt} = \frac{3(C_a + C_c + C_f)}{2\alpha C_{ox}} \quad (20)$$

Note that this equation can also be interpreted as  $C_{in} = C_a + C_p + C_f$ . The existence of the optimal gate area rather than the gate width stems from the fact that the  $1/f$  noise source depends on the gate area  $WL$  and is independent of the  $W/L$  ratio as (3) shows. It means that as far as the  $1/f$  noise is the only concern, either the  $W$  or the  $L$  may be chosen freely to meet the

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optimal noise matching condition (20). However, taking into account the thermal noise and other design requirements such as the *GBW* and the response speed, etc., the minimal transistor gate length should be chosen. The corresponding minimal 1/f noise contribution is

$$v_{eqiminf}^2 = \frac{8\alpha(C_a + C_c + C_f)K_f}{3C_{ox}C_d^2f} \quad (21)$$

As expected, the minimal 1/f noise  $v_{eqiminf}^2$  is inversely proportional to the frequency. In contrast with the theoretical minimum of the thermal noise contribution, this minimum is independent of any transistor geometrical parameters and dc bias levels. It sets thus the lowest limit of the noise level that can be achieved by a CMOS technology for any capacitive feedback amplifiers with a capacitive source. Its value can only be reduced by improving the CMOS technology with a lower  $K_f$  and a higher  $C_{ox}$ .

For the final choice of the input transistor dimension, it is important to see that the optimal noise matching condition for the 1/f noise requires an input transistor dimension which is just three times larger than for the thermal noise. This difference results in a situation where the optimal input dimension must be solved numerically. As a simple rule of thumb, one can approximate the optimal gate dimension simply as the average of both optima.

Under the optimal noise matching condition, the noise density for the case of using the MOS input is also shown in figure 6. It is clearly seen that whatever the collector current is, superior noise performance can be obtained by the MOS input rather than with a bipolar one.

This important conclusion has been confirmed by the experimental results on two integrated amplifiers. The bipolar realization is presented in [13] and its circuit schematic is given in figure 7. The input transistor Q1 uses a compromised collector current of 50  $\mu$ A to realize the best noise matching. The gain stage Q2 is biased at a much higher current level so that its noise contribution is negligible. The circuit schematic of CMOS version is shown in figure 8 [3]. The input transistor dimension is derived from the optimal noise matching condition. A dc bypass branch formed by MP and RP is added to increase the input transistor transconductance and thereby reducing the total equivalent input noise. At the same time, this branch reduces also the current noise of the active load of the input stage. With this circuit technique, the total noise contribution of all devices other than the input transistor M1 is only

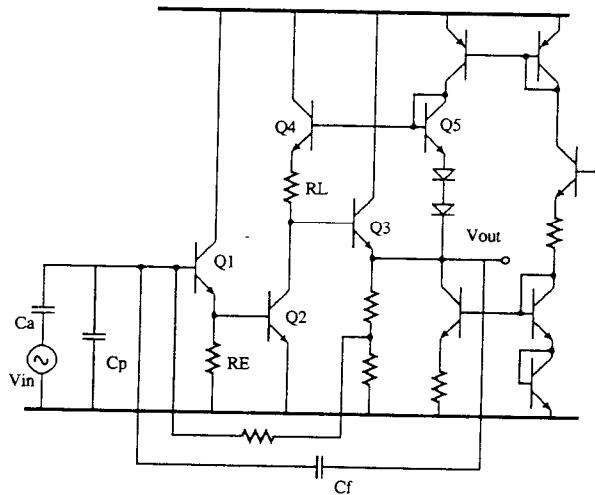


Fig. 7. Circuit schematic of capacitive antenna amplifier in bipolar technology [13].

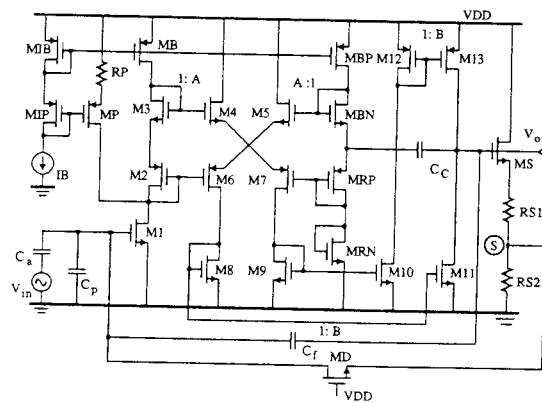


Fig. 8. Circuit schematic of capacitive antenna amplifier in CMOS technology.

5%. The measured equivalent input noise of bipolar version is 1  $\mu$ V<sub>rms</sub> and that of the CMOS version amounts to 0.7  $\mu$ V<sub>rms</sub>.

### 5. Low-Noise Amplifiers with Inductive Sources

In the previous section, low-noise design techniques are presented for amplifiers with capacitive sources. In this section, design of amplifiers with inductive sources are described. Inductive type signal sources can be found in many communication applications such as ferrite antennas in radio receivers and magnetic heads of video cassette recorders. In these systems, electrical signals are obtained by the signal conversion from electromagnetic

fields into electrical currents in an inductive coil. In general, the converted electrical signal can be very small (i.e., 1...nA) so that a very low-noise preamplifier is necessary to amplify the signal to a high level for further processing.

For such applications, a flat output response is generally required. Since the converted signal current in an inductive source is constant independent of frequency, the required flat response can easily be realized by means of a constant transimpedance amplifier. The simplest and widely used approach to the transimpedance amplifier employs a resistive feedback structure as discussed in section 3. However, the noise performance of such amplifiers is not adequate to fulfill the noise requirement because the noise current of the feedback resistor stands in parallel with the signal source. A new approach is proposed where a combined resistive and capacitive feedback configuration is used [2], [9]. The use of this configuration results in much better noise performance and at the same time realizes a constant transimpedance.

Figure 9 shows the proposed feedback configuration where A is the core amplifier,  $I_{in}$  represents the signal current generated by an electrical field in the inductive source  $L_a$  and  $C_a$  is the parasitic capacitance of the source, the feedback network is formed by  $R$ ,  $C_1$  and  $C_2$ . It can easily be calculated that the transimpedance is given by  $H(s) = -R \frac{(1 + \frac{1}{sRC_1}) \frac{C_2}{C_1}}{1 + \frac{C_2}{sRC_1}}$

No  $f(s) = \frac{-sC_1}{s(C_1 + C_2)R + 1}$  (22)

In the frequency range of interest where  $2\pi f(C_1 + C_2)R \gg 1$ , it can be further reduced to

✓  $H(s) = -\frac{C_2}{C_1} R$  (23)

Thus a constant transimpedance is realized using this combined feedback configuration. In expression (23) it is assumed that  $C_2 \gg C_1$ , which is necessary to limit the noise contribution of the feedback network.

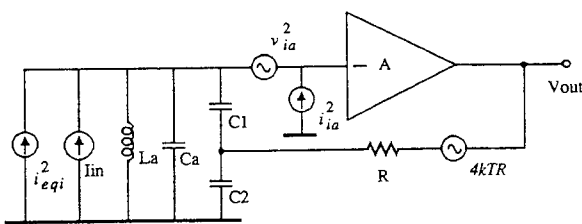


Fig. 9. Feedback topology and noise model of amplifier with inductive source.

As for all transimpedance amplifiers, the noise performance of the amplifier in figure 9 is characterized by the total equivalent input current noise  $i_{eqi}^2$  in parallel with the current source  $I_{in}$ . Since ideal inductors and capacitors do not generate noise, the total equivalent input current noise  $i_{eqi}^2$  is determined by the core amplifier noise. As for the previous two types of amplifiers, the noise performance of amplifiers with an inductive source will depend on the technology used.

5.1. BJT Technology

Neglecting the correlation effect between the two noise generators  $v_{ia}^2$  and  $i_{ia}^2$ , the total equivalent input noise current spectrum  $i_{eqi}^2$  is given by

$$i_{eqi}^2 = i_{ia}^2 + \left| \frac{1 + (j\omega)^2 L_a (C_1 + C_a)}{j\omega L_a} \right|^2 \times v_{ia}^2 + \frac{4kT}{R} \left( \frac{C_1}{C_2} \right)^2$$
 (24)

where the first two terms are the noise contributions of the core amplifier, and the last term represents the increase in noise current due to the feedback network. From expression (24) it is clear that the use of an antenna with large inductance  $L_a$  reduces the contribution of  $v_{ia}^2$ , especially at the low frequency end, while a small feedback capacitor  $C_1$  is desirable to reduce the  $v_{ia}^2$  contribution at high frequencies. Therefore, it is of great importance to keep the feedback capacitance  $C_1$  as small as possible.

The significance of the capacitive feedback on the noise performance can be evaluated from the last term. If the same transimpedance is realized by a purely resistive feedback amplifier, the noise contribution of the feedback network, which is simply a resistor  $R$  in this case, will be  $4kT/R$ . This is a factor  $C_2/C_1$  larger than the last term in (24). It is thus possible to reduce the noise contribution of the feedback network by increasing the capacitance ratio  $C_2/C_1$ . In practice a capacitance ratio of 30 is sufficient to make the noise contribution of resistor  $R$  negligible compared to the current noise of the core amplifier, even for the case where the input transistor is biased with a relative small current, for example,  $I_C = 50 \mu A$ .

Just as for the amplifiers with resistive and capacitive sources, the noise minimization for amplifiers with inductive sources also consists of making the input BJT base resistance  $r_b$  as small as possible and the current gain  $\beta$  as large as possible and of choosing an optimal collector current. By taking the derivative of (24) with

respect to  $I_1$ , it c  
rent  $I_1$  exists for  
current  $i_{eqi}^2$  is m  
frequency deper  
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5.2. CMOS Tech

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CMOS approach

$$i_{eqi}^2 = \left| \frac{1 + (j\omega)^2 L_a (C_1 + C_a)}{j\omega L_a} \right|^2 \times v_{ia}^2 + \frac{4kT}{R} \left( \frac{C_1}{C_2} \right)^2$$

where  $v_{ia}^2$  is the e  
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In contrast with th  
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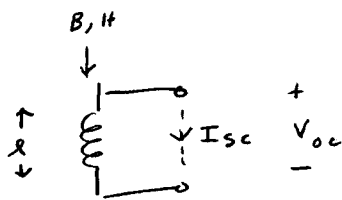
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an optimal gate w  
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quency, the optim  
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gate width  $W_{opt}$  is

$$W_{opt} = \frac{3[1 - \omega^2]}{2\omega^2 c}$$

for



### Inductive Pickup



$N$  turns, Area  $A$

$$V_{oc} = j\omega N A \mu H$$

$$I_{sc} = \frac{l}{N} H$$

$$Z = \frac{V_{oc}}{I_{sc}} = j\omega L$$

$$L = \frac{\mu A N^2}{l}$$

respect to  $I_1$ , it can be shown that an optimal bias current  $I_1$  exists for which the total equivalent input noise current  $i_{eqi}^2$  is minimum. However, this minimum is frequency dependent, as the source impedance and feedback network depend on frequency. As a result, the noise optimization in a wide frequency band is not possible by using a bipolar approach and therefore a compromised collector current must be taken [2], [9].

## 5.2. CMOS Technology

From the above discussion, it becomes clear that the obstacle to the best noise performance of bipolar amplifiers with reactive sources is the base shot noise. For the case of capacitive source, it is shown that better noise performance can be obtained by using a CMOS approach rather than a bipolar one. It will be shown now that the same is also true for the case of an inductive source. Taking into account the correlation between the two equivalent input noise generators  $v_{ia}^2$  and  $i_{ia}^2$ , the total equivalent input current noise for the case of CMOS approach is given by [9]:

$$i_{eqi}^2 = \left| \frac{1 + (j\omega)^2 L_a (C_1 + C_a + C_{GS} + C_{GD})}{j\omega L_a} \right|^2 \times v_{ia}^2 + \frac{4kT}{R} \left( \frac{C_1}{C_2} \right)^2 \quad (25)$$

where  $v_{ia}^2$  is the equivalent input voltage noise generator of the input MOS transistor, and is given by (4). In contrast with the case of a BJT input where a constant current noise term due to the base current noise exists in  $i_{eqi}^2$  in (24), with a MOS input device this term is eliminated. It is the disappearing of this constant current noise term that makes the MOS input preferable over the BJT input. Similar to the case of capacitive sources, the above expression can be minimized by the optimal design of the input MOS transistor.

For the channel thermal noise, it can be shown that an optimal gate width exists for which equation (25) is minimal. Since the coefficient of  $v_{ia}^2$  depends on frequency, the optimal transistor dimensions depend on the frequency as well. For frequencies lower than the resonant frequency  $\omega_r = 1/\sqrt{L_a(C_a + C_1)}$  the optimal gate width  $W_{opt}$  is given by

$$W_{opt} = \frac{3[1 - \omega^2 L_a (C_a + C_1)]}{2\omega^2 \alpha L C_{ox} L_a} \approx \frac{3}{2\omega^2 \alpha L C_{ox} L_a} \quad (26)$$

$$\text{for } \omega \ll \omega_r = \frac{1}{\sqrt{L_a(C_a + C_1)}}$$

It can be easily shown that this optimal gate width corresponds with the classical reactive noise matching condition which reduces the noise at a specific frequency exactly to zero by making the impedance to be infinite at that frequency. However, for wide-band noise matching, the strong frequency dependence of  $W_{opt}$  in (26) makes it not valuable. On the other hand, for frequencies higher than the resonant frequency  $\omega_r$ , the optimal  $W_{opt}$  is given by

$$W_{opt} = \frac{\omega^2 L_a (C_a + C_1) - 1}{2\omega^2 \alpha L C_{ox} L_a} \approx \frac{C_a + C_1}{2\alpha L C_{ox}}$$

$$\text{for } \omega \gg \omega_r = \frac{1}{\sqrt{L_a(C_a + C_1)}} \quad (27)$$

which is approximately independent of frequency allowing realization of the noise matching in a wide frequency band. Under this noise matching condition, it can be shown that a factor of two lower noise voltage can be obtained by the CMOS approach instead of the bipolar one.

However, as CMOS exhibits much 1/f noise, its effect must be investigated as well. Since 1/f noise depends on the gate area  $WL$ , it is anticipated that an optimal gate area exists for which the 1/f noise contribution to the total  $i_{eqi}^2$  is minimal. It can be shown that for  $\omega < \omega_r$  the optimal gate area is given by exactly the same expression (26) as for the thermal noise making the 1/f noise contribution to zero. While for  $\omega > \omega_r$ , the value of the optimal  $WL$  is approximately independent of frequency and is just three times larger than the value given by (27) [9]. Obviously, for the final choice of the input transistor dimensions, both the thermal and 1/f noise must be considered at the same time.

To verify the above analysis, both bipolar and CMOS amplifiers have been designed to match an inductive antenna of practical radio receivers. The circuit schematic of the bipolar version is given in figure 10 [2], [9]. The input transistor Q1 uses a compromised collector current of 50  $\mu\text{A}$  to realize the best noise matching in a wide frequency band. The emitter degeneration technique is applied to the active load of the input stage and to the current mirror of the output stage. This technique is invaluable to limit the extra noise contributions of the active load and the current mirror. The circuit schematic of CMOS version is shown in figure 11 [9]. The input transistor dimension is numerically derived from the optimal noise matching conditions. Since the input stage has a relatively high constant gain up to high frequencies, the noise contribution of the second and third stages are negligible. The noise performance of

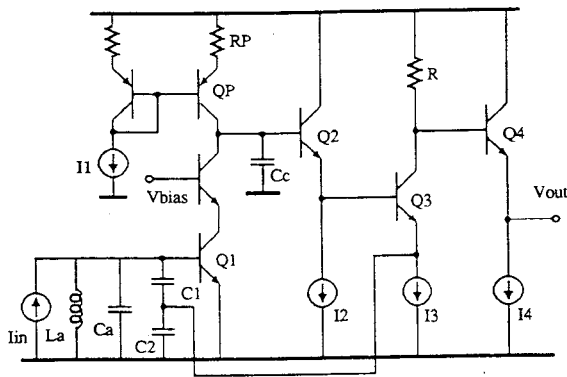


Fig. 10. Circuit schematic of inductive antenna amplifier in bipolar technology.

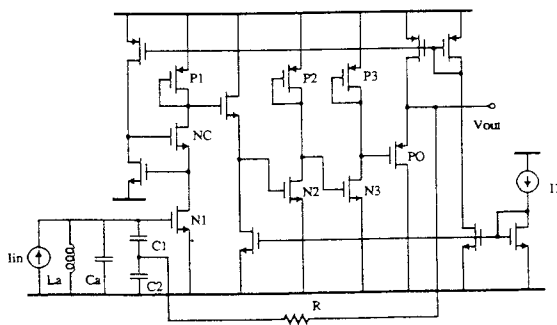


Fig. 11. Circuit schematic of inductive antenna amplifier in CMOS technology.

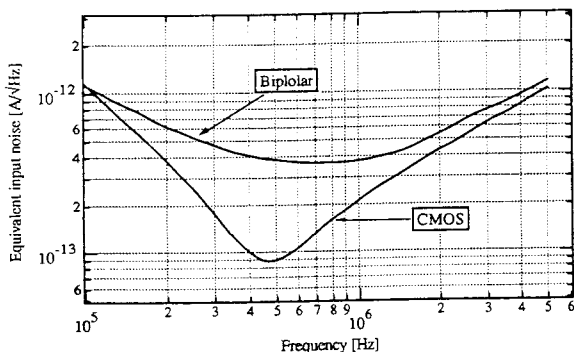


Fig. 12. Noise performance of bipolar and CMOS inductive antenna amplifiers.

both amplifiers is shown in figure 12. It is clear that the CMOS amplifier shows a lower noise level than the bipolar one, especially around the resonant frequency. It is important to realize that in spite of the much higher  $1/f$  noise, CMOS amplifiers show lower noise density even at the lower frequency end due to the optimal design of the input device.

### 6. Conclusions

The capability of bipolar and CMOS technologies for low-noise monolithic amplifier design is described. Based on the basic noise models of BJT and MOS transistors, noise matching conditions are derived for all three possible types of source impedance, i.e., resistive, capacitive and inductive. For each type of source impedance, comparisons are made between the best noise performance obtainable by using bipolar and CMOS technologies. It is shown that for a resistive source, both bipolar and CMOS amplifiers can easily be designed of which the noise performance is dominated by the source resistance itself.

On the other hand, for a capacitive or an inductive source, low-noise design requires much more effort because the source itself does not generate any noise and the impedance varies with frequencies. In the case of a bipolar approach, the best noise performance requires a BJT input transistor with a minimal base resistance, maximal current gain  $\beta$  and an optimal collector bias current. The basic limitation to low-noise performance of bipolar amplifiers for reactive sources is the existence of the base shot noise. This base shot noise prevents noise matching from being realized in a wide frequency band.

This limitation can be eliminated by using a CMOS approach due to its inherent low input current noise property. However, as a CMOS technology shows much higher  $1/f$  noise than a bipolar one, low-noise design in a CMOS technology must take into account the  $1/f$  noise as well. It is shown that for a given reactive signal source, a CMOS approach enables the best noise matching to be obtained in a wide frequency band by proper choice of the input transistor dimensions. This fact leads to the important conclusion that better noise performance can be obtained by a CMOS approach rather than a bipolar one.

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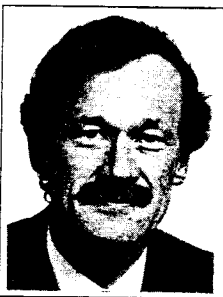
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