7. DESIGN PROJECT-FALL 2009

7.1 Objective

The objective of this experiment is to design, simulate, evaluate experimentally, and document a low-noise electronic amplifier circuit in which the output port is totally electrically isolated from the input. The equivalent input noise of the amplifier is to be minimized, viz. the noise performance of the amplifier is to be optimized with respect to the output noise.

7.2 Specifications

The specifications for the amplifier are:

- DC Power Supplies: ± 15 V and +5 V
- Small-Signal Midband Voltage Gain: 40 dB
- Minimum Output Signal for which the THD is to be 0.2% or less $5\sqrt{2}$ V peak, viz. an rms value of 5 V. The THD is to be measured for a input which is a sine wave with a frequency of 2 kHz. The value of the input is that which makes the output 5 V rms.
- Lower Half-Power Frequency: 20 Hz or less
- Upper Half-Power Frequency: 20 kHz or greater
- Source Resistance: $5.1\,\mathrm{k}\Omega$
- Load Resistance: $12 \,\mathrm{k}\Omega$
- \bullet Noise voltage over the band 20 Hz to 20 kHz $\,$ optimal, viz. lowest noise that can be obtained at the output port
- Devices. The devices are restricted to those available for this course, viz. Transistors: 2N4401 NPN BJT, 2N3904 NPN BJT, 2N4403 PNP BJT, 2N3906 PNP BJT, 2N5457 N Channel JFET Isolators: 4N25 Op Amps 741, TL071, OP-27

7.3 Simulation

The initial design should be verified with a SPICE simulation. This simulation must precede the circuit assembly.

Should the designer elect to employ a BJT as the first stage, the default values for IS, BF, RB, VA, CJC, CJE, and TF for the BJT transistor are not to be used for the simulation. Instead, use the values obtained from curve tracer measurements or manufacturers' data sheets. The value of the base spreading resistance measured in a previous experiment is to be used as RB. (In determining the optimum collector current use an average or typical value that was measured for the transistor.)

A noise simulation of the circuit should be made which predicts the signal-to-noise ratio corresponding to an output signal level of 5 V rms and noise figure of the amplifier.

The SPICE analyses should include .OP (to verify the biasing), .AC (to verify the frequency response specifications and phase margin specifications), .TRAN (to examine the clipping and slew rate performance), .FOUR (to verify the distortion specification), and .NOISE (to verify the noise specifications).

7.4 Experimental Measurements

Assemble the designed circuit on a solderless breadboard with a $12 \,\mathrm{k}\Omega$ load resistor. Use a power supply decoupling network.

Use the laboratory equipment to measure and record the circuit:

- mid-band voltage gain
- -3 dB bandwidth
- positive and negative slew rates
- distortion @ f = 2 kHz and output signal 5 V rms
- quiescent operating point
- output DC offset with input grounded
- equivalent input noise voltage
- signal-to-noise ratio (where output signal is 5 V rms
- noise figure (spot noise figure @ f = 2 kHz and the total noise figure)

The noise measurements are made with the source grounded. The other measurements are made with the function generator or the signal analyzer as the source.

7.5 Recommendations

The recommended topology used for the amplifier is three devices or stages. The first device or stage is to be a discrete BJT such as the 2N4401 NPN BJT. The second is an electrooptical isolator which provides total electrical isolation between the input and output ports. The third may be either discrete or an op amp. The attached SPICE simulation does not meet the design specifications. It is provided as a possible template for a design. But the designers are free to be creative.

The attached SPICE simulation was made with student or evaluation version 16.2 of Cadence SPICE. It was chosen because it has a built in part for the 4N25 electro-optical isolator. National Instruments Multisim is also available; it has electro-optical isolators but not this one.

A specification sheet for the 4N25 is attached.

7.6 Laboratory Report

The laboratory report should simply, succinctly, and lucidly summarize the design philosophy, present the appropriate calculations, and compare the theoretical, simulation, and experimental results.

The design project will weighted as three lab reports and will graded somewhat more critically than the previous reports. Although the design project grade will in part depend on the write-up, the major criterion will be whether or not the circuit meets the design criteria.

7.7 Due Date

Friday, December 4, 2009 A. D. @ 5 pm Eastern Standard Time





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Date: October 20, 2009

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Date: October 20, 2009



** Profile: "SCHEMATIC1-CE Sweep" [Z:\Red Ruby\brewdoc\NOISEf09\Z_DP_f09_opt\Cadence\ce summer 2008-psp... Date/Time run: 10/20/09 18:53:12 Temperature: 27.0

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Time: 19:03:56

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Isolation Techniques Using Optical Couplers

Prepared by: Francis Christian

INTRODUCTION

The optical coupler is a venerable device that offers the design engineer new freedoms in designing circuits and systems. Problems such as ground loop isolation, common mode noise rejection, power supply transformations, and many more problems can be solved or simplified with the use of an optical coupler.

Operation is based on the principle of detecting emitted light. The input to the coupler is connected to a light emitter and the output is a photodector, the two elements being separated by a transparent insulator and housed in a light–excluding package. There are many types of optical couplers; for example, the light source could be an incandescent lamp or a light emitting diode (LED). Also, the detector could be photovoltaic cell, photoconductive cell, photodiode, phototransistor, or a light–sensitive SCR. By various combinations of emitters and detectors, a number of different types of optical couplers could be assembled.

Once an emitter and detector have been assembled as a coupler, the optical portion is permanently established so that device use is only electronic in nature. This eliminates the need for the circuit designer to have knowledge of optics. However, for effective application, he must know something of the electrical characteristics, capabilities, and limitations of the emitter and detector.

COUPLER CHARACTERISTICS

The 4N25 is an optical coupler consisting of a gallium arsenide (GaAs) LED and a silicon phototransistor. (For more information on LEDs and phototransistors, see References 1 and 2.)

The coupler's characteristics are given in the following sequence: LED characteristics, phototransistor characteristics, coupled characteristics, and switching characteristics. Table 1 shows all four for the 4N25 series.

INPUT

For most applications the basic LED parameters IF and VF are all that are needed to define the input. Figure 1 shows these forward characteristics, providing the necessary information to design the LED drive circuit. Most circuit applications will require a current limiting resistor in series with the LED input. The circuit in Figure 2 is a typical drive circuit.

The current limiting resistor can be calculated from the following equation:

$$\mathsf{R} = \frac{\mathsf{V}_{\mathsf{IN}} - \mathsf{V}_{\mathsf{F}}}{\mathsf{I}_{\mathsf{F}}},$$



 V_F = diode forward voltage I_F = diode forward current



Figure 1. Input Diode Forward Characteristic







LED CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
*Reverse Leakage Current ($V_R = 3.0 V, R_L = 1.0 M ohms$)	IR	—	0.05	100	μΑ
*Forward Voltage (I _F = 50 mA)	۷ _F	—	1.2	1.5	Volts
Capacitance ($V_R = 0 V, f = 1.0 MHz$)	С	—	150	—	pF

PHOTOTRANSISTOR CHARACTERISTICS (T_A = 25°C and I_F = 0 unless otherwise noted)

Characteristic		Symbol	Min	Тур	Max	Unit	
*Collector–Emitter Dark Current (V _{CE} = 10 V, Base Open)	4N25, 4N26, 4N27 4N28	ICEO	—	3.5 —	50 100	nA	
*Collector–Base Dark Current (V _{CB} = 10 V, Emitter Open)		Ісво	—	—	20	nA	
*Collector–Base Breakdown Voltage ($I_C = 100 \ \mu A, I_E = 0$)		V(BR)CBO	70	—	—	Volts	
*Collector–Emitter Breakdown Voltage (I _C = 1.0 mA, I _B = 0)		V(BR)CEO	30	—	—	Volts	
*Emitter–Collector Breakdown Voltage (I _E = 100 μA, I _B = 0)		V(BR)ECO	7.0	—	—	Volts	
DC Current Gain (V _{CE} = 5.0 V, I _C = 500 μA)		hFE	—	250	—	—	

COUPLED CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Тур	Max	Unit
*Collector Output Current ⁽¹⁾	4N25, 4N26	۱ _C	2.0	5.0	—	mA
$(V_{CE} = 10 \text{ V}, I_{F} = 10 \text{ mA}, I_{B} = 0)$	4N27, 4N28		1.0	3.0	—	
*Isolation Voltage ⁽²⁾	4N25	VISO	2500	—	—	Volts
	4N26, 4N27		1500	-	-	
	4N28		500	—	—	
Isolation Resistance ⁽²⁾ (V = 500 V)		-	—	10 ¹¹	—	Ohms
*Collector–Emitter Saturation ($I_C = 2.0 \text{ mA}, I_F = 50 \text{ mA}$)		V _{CE(sat)}	—	0.2	0.5	Volts
Isolation Capacitance ⁽²⁾ (V = 0, f = 1.0 MHz)		—	—	1.3	—	pF
Bandwidth ⁽³⁾ (I _C = 2.0 mA, R _L = 100 ohms, Figure 11)		-	—	300	—	kHz
SWITCHING CHARACTERISTICS				_		
Delay Time	4N25 4N26	+ .		0.07		110

Delay fille	(I _C = 10 mA, V _{CC} = 10 V)	4N27, 4N28	۰a	_	0.10	_	μο
Rise Time	Figures 6 and 8	4N25, 4N26 4N27, 4N28	tr	—	0.8 2.0	—	μs
Storage Time	(I _C = 10 mA, V _{CC} = 10 V)	4N25, 4N26 4N27, 4N28	t _s	—	4.0 2.0	—	μs
Fall Time	Figures 7 and 8	4N25, 4N26 4N27, 4N28	t _f	—	7.0 3.0	—	μs

* Indicates JEDEC Registered Data 1. Pulse Test: Pulse Width = 300 μ s, Duty Cycle \leq 2.0%.

2. For this test LED pins 1 and 2 are common and Photo Transistor pins 4, 5 and 6 are common.

3. IF adjusted to yield IC = 2.0 mA and IC = 2.0 mAp p at 10 kHz.

OUTPUT

The output of the coupler is the phototransistor. The basic parameters of interest are the collector current I_C and collector emitter voltage, V_{CE}. Figure 3 is a curve of V_{CE(sat)} versus I_C for two different drive levels.

COUPLING

To fully characterize the coupler, a new parameter, the dc current transfer ratio or coupling efficiency (η) must be defined. This is the ratio of the transistor collector current to diode current I_C/I_F. Figures 4A and 4B show the typical dc current transfer functions for the couplers at V_{CE} = 10 volts. Note that η varies with I_F and V_{CE}.



Once the required output collector current I_C is known, the input diode current can be calculated by

$$I_F = I_C/\eta$$
,

where IF is the forward diode current IC is the collector current η is the coupling efficiency or transfer ratio.









Figure 4B. DC Current Transfer Ratio

RESPONSE TIME

The switching times for the couplers are shown in Figures 5A and 5B. The speed is fairly slow compared to switching transistors, but is typical of phototransistors because of the large base–collector area. The switching time or bandwidth of the coupler is a function of the load resistor R_L because of the R_LC_O time constant where C_O is the parallel combination of the device and load capacitances. Figure 6 is a curve of frequency response versus R_L.



Figure 5A. Switching Times





Figure 5B. Switching Times



Figure 6. Frequency Response



Figure 7. Pulse Mode Circuit

Figure 8. Linear Mode Circuit



Figure 9. Circuit Connections for Using the 4N26 as a Diode–Diode Coupler OPERATING MODE

The two basic modes of operation are pulsed and linear. In the pulsed mode of operation, the LED will be switched on or off. The output will also be pulses either in phase or 180° out of phase with the input depending on where the output is taken. The output will be 180° out of phase if the collector is used and in phase if the emitter is used for the output.

In the linear mode of operation, the input is biased at a dc operating point and then the input is changed about this dc point. The output signal will have an ac and dc component in the signal.

Figures 7 and 8 show typical circuits for the two modes of operation.

THE 4N26 AS A DIODE-DIODE COUPLER

The 4N26, which is a diode–transistor coupler, can be used as a diode–diode coupler. To do this the output is taken between the collector and base instead of the collector and emitter. The circuits in Figure 9 show the connections to use the coupler in the diode–diode mode.

The advantage of using the 4N26 as a diode–diode coupler is increased speed. For example, the pulse rise time for adiode–transistor coupler is in the order of 2 to 5 μ s, where the diode–diode coupler is 50 to 100 ns. The one disadvantage with the diode–diode coupler is that the output current is much lower than the diode–transistor coupler. This is because the base current is being used as signal current and the β multiplication of the transistor is omitted. Figure 10 is a graph of IB versus IF using the coupler in the diode–diode mode.



Figure 10. IB versus IF Curve for Using the 4N26 as a Diode–Diode Coupler



Figure 11. Coupler–Driven SCR

APPLICATIONS

The following circuits are presented to give the designer ideas of how the 4N26 can be used. The circuits have been bread-boarded and tested, but the values of the circuit components have not been selected for optimum performance over all temperatures.

Figure 11 shows a coupler driving a silicon controlled rectifier (SCR). The SCR is used to control an inductive load, and the SCR is driven by a coupler. The SCR used is a sensitive gate device that requires only 1 mA of gate current and the coupler has a minimum current transfer ratio of 0.2 so the input current to the coupler, IF, need only be 5 mA. The 1 k resistor connected to the gate of the SCR is used to hold off the SCR. The 1N4005 diode is used to supress the self-induced voltage when the SCR turns off.

Figure 12 is a circuit that couples a high voltage load to a low voltage logic circuit. To ensure that the voltage to the MTTL



Figure 12. Opto Coupler in a Load to Logic Translation

flip-flop exceeds the logic-one level, the coupler output current must be at least 10 mA. To guarantee 10 mA of output current, the input current to the LED must be 50 mA. The current limiting resistor R can be calculated from the equation

 $R = \frac{V - V_F}{0.05}$. If the power supply voltage, V, is much greater

than VF, the equation for R reduces to $R = \frac{V}{0.05}$.

The circuit of Figure 13 shows a coupler driving an operational amplifier. In this application an ac signal is passed through the coupler and then amplified by the op amp. To pass an ac signal through the coupler with minimum distortion, it is necessary to bias the LED with a dc current. The ac signal is summed with the dc current so the output voltage of the coupler will have an ac and a dc component. Since the op amp is capacitively coupled to the coupler, only the ac signal will appear at the output.



Figure 13. Coupling an AC Signal to an Operational Amplifier

The circuit of Figure 14 shows the 4N26 being used as a diode–diode coupler, the output being taken from the collector–base diode. In this mode of operation, the emitter is left open, the load resistor is connected between the base and ground, and the collector is tied to the positive voltage supply. Using the coupler in this way reduces the switching time from 2 to 3 μ s to 100 ns.



Figure 14. Using the 4N26 as a Diode–Diode Coupler

The circuit of Figure 15 is a standard two-transistor one-shot, with one transistor being the output transistor of the coupler. The trigger to the one-shot is the LED input to the coupler. A pulse of 3 μ s in duration and 15 mA will trigger the circuit. The output pulse width (PW_O) is equal to 0.7 RC + PW₁ + 6 μ s where PW₁ is the input pulse width and 6 μ s is the turn-off delay of the coupler. The amplitude of the output pulse is a function of the power supply voltage of the output side and independent of the input.



Figure 15. Pulse Stretcher

The circuit of Figure 16 is basically a Schmitt trigger. One of the Schmitt trigger transistors is the output transistor of a coupler. The input to the Schmitt trigger is the LED of the coupler. When the base voltage of the coupler's transistor exceeds V_e+V_{be} the output transistor of the coupler will switch on. This

will cause Q2 to conduct and the output will be in a high state. When the input to the LED is removed, the coupler's output transistor will shut off and the output voltage will be in a low state. Because of the high impedance in the base of the coupler transistor, the turn–off delay is about $6\mu s$.

AN571A



Figure 16. Optically Coupled Schmitt Trigger





The high base impedance (100 k ohms) represents a compromise between sensitivity (input drive required) and frequency response. A low value base resistor would improve speed but would also increase the drive requirements.

The circuit in Figure 17 can be used as an optically coupled R–S flip–flop. The circuit uses two 4N26 couplers cross coupled to produce two stable states. To change the output from a low state to a high state requires a positive 2 V pulse at the set input. The minimum width of the set pulse is 3 μ s. To switch the output back to the low state needs only a pulse on the reset input. The reset–operation is similar to the set operation.

Motorola integrated voltage regulators provide an input for the express purpose of shutting the regulator off. For large systems, various subsystems may be placed in a stand-by mode to conserve power until actually needed. Or the power may be turned OFF in response to occurrences such as overheating, over-voltage, shorted output, etc.

With the use of the 4N26 optically coupler, the regulator can be shut down while the controlling signal is isolated from the regulator. The circuit of Figure 18 shows a positive regulator connected to an optical coupler.

To ensure that the drive to the regulator shut down control is 1 mA, (the required current), it is necessary to drive the LED in the coupler with 5 mA of current, an adequate level for logic circuits.



Figure 18. Optical Coupler Controlling the Shut Down of MC1569 Voltage Regulator



Figure 19. Simple Pulse Amplifier

The circuit in Figure 19 is a simple pulse amplifier using positive, ac feedback into the base of the 4N26. The advantage of the feedback is in faster switching time. Without the feedback, the pulse rise time is about 2.0 μ s, but with the positive feedback, the pulse rise time is about 0.5 μ s. Figure 17A shows the input and output wave–forms of the pulse amplifier.

REFERENCES

- 1. "Theory and Characteristics of Phototransistors," Motorola Application Note AN440.
- 2. "Motorola Switching Transistor Handbook."
- Deboo, G.J. and C.N. Burrous, Integrated Circuits and Semiconductor Devices Theory and Application. New York: McGraw–Hill, 1971.

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