

Mohit Pathak

Address:

Mohit Pathak
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Education:

08/2007 – current

Ph.D (candidate) in Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA

08/2007

MS in Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA

05/2004

B.Tech in Computer Science and Engineering
Indian Institute of Technology, Kharagpur, India

Skills:

Programming Languages:

C++, C, Matlab

Tools:

Cadence P&R tools (Encounter), Synopsys Tools
Sonnet, Ansys

Research Experience:

- Member of a team that developed a 64-core processor-memory stack in a 3D IC using 130nm technology and sent for fabrication in March 2010
- Experience in analysis and developing a tool flow for 3D integrated circuits using existing commercial 2D physical design tools
- Experience in various physical design algorithms like partitioning, placement, global routing, timing analysis and optimization
- Experience with tools like Ansys to perform finite element analysis (stress in 3D ICs)
- Experience with existing commercial tools from Cadence and Synopsys for physical design automation of integrated circuits.

Work Experience:

05/2004 - 06/2005

Member Technical Staff,
Magma Design Automation, Bangalore, India

- Managed pad placement and design for integrated circuits

Publications:

Journal:

- Jacob Minz, Eric Wong, **Mohit Pathak**, and Sung Kyu Lim, "Placement and Routing for 3D System-On-Package Designs," *IEEE Transactions on Components and Packaging Technologies*, Vol. 29, No. 3, pp. 644-657, 2006.
- **Mohit Pathak** and Sung Kyu Lim, "Performance and Thermal-aware Steiner Routing for 3D Stacked ICs", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 28, No. 9, pp. 1373-1386, 2009.
- **Mohit Pathak** and Sung Kyu Lim, "Fast Layout Generation of RF Embedded Passive Circuits Using Mathematical Programming", submitted to *IEEE Transactions on Components and Packaging Technologies*

Conference:

- Ramprasad Ravichandran, Jacob Minz, **Mohit Pathak**, Siddharth Easwar, and Sung Kyu Lim, "Physical Layout Automation for System-On-Packages," *IEEE Electronic Components and Technology Conference (ECTC)*, pp. 41-48, 2004.
- Jacob Minz, **Mohit Pathak**, and Sung Kyu Lim, "Net and Pin Distribution for 3D Package Global Routing," *Design, Automation and Test in Europe (DATE)*, pp. 1410-1411, 2004
- **Mohit Pathak**, Souvik Mukherjee, Madhavan Swaminathan, Ege Engin, and Sung Kyu Lim, "Placement and Routing of RF Embedded Passive Designs In LCP Substrate", *IEEE International Conference on Computer Design (ICCD)*, pp. 273-279, 2007.
- **Mohit Pathak**, Satya Vadlamudi, Josh Beavers, and Sung Kyu Lim, "Automatic Layout Generation of RF Embedded Passive Designs", *IEEE Electrical Performance of Electronic Packaging (EPEP)*, pp. 115-118, 2007.
- **Mohit Pathak** and Sung Kyu Lim, "Thermal-aware Steiner Routing for 3D Stacked ICs," *IEEE International Conference on Computer-Aided Design (ICCAD)*, pp. 205-211, 2007.
- Young-Joon Lee, **Mohit Pathak**, Chang Liu, Moongon Jung, and Sung Kyu Lim, "Design and Timing Optimization of a 3D Stacked Microprocessor", *ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, 2010
- **Mohit Pathak**, Young-Joon Lee, Thomas Moon, and Sung Kyu Lim, "Through Silicon Via Management during 3D Physical Design: When to Add and How Many?", *IEEE International Conference on Computer-Aided Design (ICCAD)*, 2010.
- Michael B. Healy, **Mohit Pathak**, S.K. Lim et.al. , "Design and Analysis of 3D-MAPS: A Many-Core 3D Processor with Stacked Memory", *IEEE Custom Integrated Circuits Conference (CICC)*, 2010.

- Dean Lewis, **Mohit Pathak**, Hsien-Hsin Lee et.al. , "Design and Test of 3D-MAPS, a 3D Die-Stack Many-Core Processor", *IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits*, 2010.
- Jiwoo Pak, **Mohit Pathak**, Sung Kyu Lim and David Z. Pan, "Modeling of Electromigration in Through-Silicon-Via Based 3D IC", *IEEE Electronic Components and Technology Conference (ECTC)*, 2011
- **Mohit Pathak**, Jiwoo Pak, David Z. Pan and Sung Kyu Lim, "Electromigration Modeling and Full-chip Reliability Analysis for TSV-based 3D ICs", submitted to *ACM Design Automation Conference (DAC)*, 2011.

References available on request