Modeling Multi Output Filtering Effects in PCMOS

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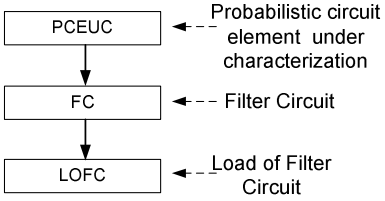
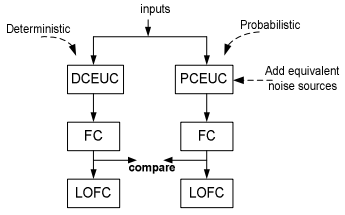
Abstract:

• To quickly and accurately predict the error-rates of noise based Probabilistic CMOS (PCMOS) Circuits.
• Cascade Math Model [4,5] predicts the error-rates of cascaded blocks of circuits if the error-rates of unique blocks are known.
• Previously, two stage model [6] was used for obtaining error-rates of unique circuit elements (blocks).
•The results from the two stage model work well for linear circuits like Ripple Carry Adder, Carry-Select Adder, etc., but do not work properly for two dimensional circuits like Wallace Tree Multiplier.
• We observe different filtering effects for different paths in a circuit because different paths present different delays.
•The two stage model [6] does not account for different filtering effects for different paths in a circuit.
• In this paper, we present a new model – Three Stage Model – which accounts for different filtering for different paths.
• We show that using the proposed three stage model, the cascade math model can accurately predict the error-rates of a Wallace Tree Multiplier.

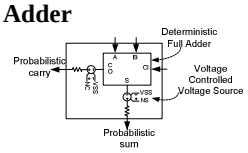
A New Model for Characterizing PCEs (Three Stage Model)



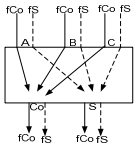
Characterization Procedure for PCEs



Probabilistic Full Adder

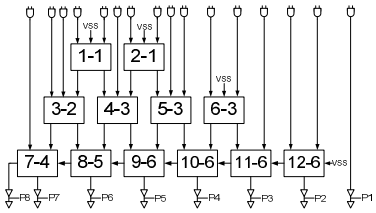


A Probabilistic Full Adder used in a Probabilistic Wallace Tree Multiplier

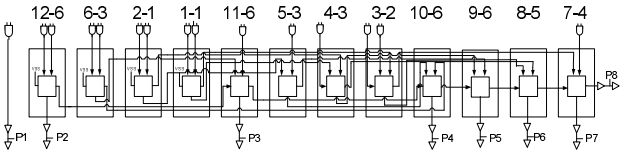


Full Adder of a Wallace Tree Multiplier for Cascade Math Model [4,5]

Wallace Tree Multiplier

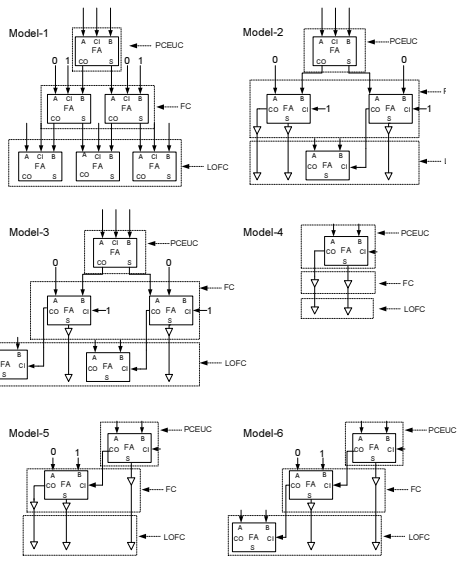


A 4x4 Wallace Tree Multiplier



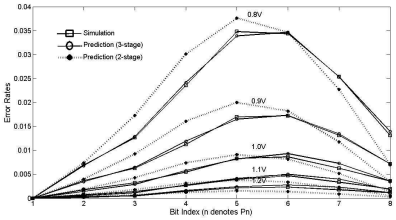
Cascade Structure of a 4x4 Wallace Tree Multiplier

Three Stage Models of Unique Full Adders in a Wallace Tree Multiplier

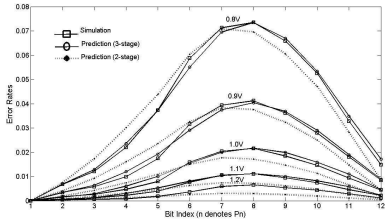


Three Stage Models of Full Adders of a Wallace Tree Multiplier

Simulation Results



4x4 Wallace Tree Multiplier Error-Rates



6x6 Wallace Tree Multiplier Error-Rates

References

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[3] Lau et al., "A general mathematical model of probabilistic ripple-carry adders," DATE, 8-12 Mar'10, Dresden, Germany, pp. 1100-1105.
[4] Lau et al., "Error rate prediction for probabilistic circuits with more general structures", SASIMI2010, 18-19 October, 2010, Taipei, Taiwan, pp. 220-225.
[5] Bhanu et al., " A more precise model of noise based PCMOS errors," Proceedings of 2010 DELTA, pp. 99-102.