## EXAMINATION NO. 2

NAME $\qquad$ SCORE $\qquad$
INSTRUCTIONS: This exam is closed book with one sheet of notes permitted. The exam consists of 4 questions for a total of 100 points. Please show your work leading to your answers so that maximum partial credit may be given where appropriate. Be sure to turn in your exam with the problems in numerical order, firmly attached together.
Problem 1-( 25 points)
A CMOS op amp is shown. All W/L values of all transistors are $10 \mu \mathrm{~m} / 1 \mu \mathrm{~m}$. Assume that $K_{N}{ }^{\prime}=$ $110 \mu \mathrm{~A} / \mathrm{V}^{2}, K_{P}{ }^{\prime}=50 \mu \mathrm{~A} / \mathrm{V}^{2}, V_{T N}$ $=0.7 \mathrm{~V}, V_{T P}=-0.7 \mathrm{~V}, \lambda_{N}=$ $0.04 \mathrm{~V}^{-1}$, and $\lambda_{P}=0.05 \mathrm{~V}^{-1}$. Find the low frequency differential voltage gain, $v_{\text {out }} / v_{\text {in }}$, the gainbandwidth, $G B$, the slew rate, $S R$, and the power dissipation, $P_{\text {diss }}$ if $V_{D D}=2 \mathrm{~V}$.

are $10 \mu \mathrm{~m} / 1 \mu \mathrm{~m}$
Fig. S03E1P1

## Problem 2-(25 points)

A two-stage, Miller compensated op amp has the following values: $g_{m I}=100 \mu \mathrm{~S}, g_{m I I}=$ $1000 \mu \mathrm{~S}, C_{c}=2 \mathrm{pF}$, and $C_{L}=10 \mathrm{pF}$.
a.) What value of nulling resistor, $R_{z}$, will cancel the output pole?
b.) If the output capacitance of the first stage is $C_{I}=1 \mathrm{pF}$, what is the phase margin if $R_{z}$ is $5 \mathrm{k} \Omega$ and the RHP zero still cancels the output pole.
c.) In part b.) if $C_{L}$ is increased to 20 pF and $R_{z}=5 \mathrm{k} \Omega$, what is the new phase margin?

## Problem 3-( 25 points)

For the CMOS op amp shown, assume the model parameters for the transistors are $K_{N}{ }^{\prime}=$ $110 \mu \mathrm{~A} / \mathrm{V}^{2}, K_{P}{ }^{\prime}=50 \mu \mathrm{~A} / \mathrm{V}^{2}, V_{T N}$ $=0.7 \mathrm{~V}, \quad V_{T P}=-0.7 \mathrm{~V}, \lambda_{N}=$ $0.04 \mathrm{~V}^{-1}$, and $\lambda_{P}=0.05 \mathrm{~V}^{-1}$. Let all transistor lengths be $1 \mu \mathrm{~m}$ and design the widths of every transistor and the dc currents $I_{5}$ and $I_{7}$ to satisfy the following specifications:

Slew rate $=10 \mathrm{~V} / \mu \mathrm{s}$
$+\mathrm{ICMR}=0.8 \mathrm{~V}$

$-\mathrm{ICMR}=0 \mathrm{~V}$
$\mathrm{GB}=10 \mathrm{MHz}$
Phase margin $=60^{\circ}\left(g_{m I I}=10 g_{m I}\right.$ and $\left.V_{S G 4}=V_{S G 6}\right)$

## Problem 4-( 25 points)

The device parameters for the operational amplifier shown below are given in the table. Ignore the body effect of the MOS transistor and the internal capacitances of all the transistors.
a. What resistance R in the emitter of Q 9 is required to set the first stage bias currents in the emitters of Q3 and Q4 at $10 \mu \mathrm{~A}$ each?
b. Calculate the overall voltage gain of the amplifier, by calculating the effective transconductances of the differential input stage and the $2^{\text {nd }}$ gain stage, and their effective output resistances.
c. Calculate the value of the miller capacitance Cc required to obtain a gain-bandwidth of 2 MHz for this op-amp.
d. Calculate the phase margin of this op-amp.

| Parameter | NPN | PNP |
| :--- | :---: | :---: |
| Beta | 200 | 50 |
| Early voltage | 130 | 50 |
|  | MOS |  |
| lambda | $0.01 \mathrm{~V}^{-1}$ |  |
| $\mu$ Cox | $30 \mu \mathrm{~A} / \mathrm{V}^{2}$ |  |
| VTO | 0.8 V |  |



Extra Sheet

